where

$$\frac{dQ_j(V_x)}{dV_x} = C_j(V_x) = \frac{A \cdot C_{j0}}{\sqrt{1 + \frac{V_x}{\phi_0}}} = A \cdot \sqrt{\frac{q\,\varepsilon_{Si}\,N_A}{2(\phi_0 + V_x)}} \tag{9.18}$$

according to (3.104), and

$$\phi_0 = \frac{kT}{q} \ln\left(\frac{N_D \cdot N_A}{n_i^2}\right) \tag{9.19}$$

$$C_{j0} = \sqrt{\frac{q\,\varepsilon_{Si}\,N_A\,N_D}{2(N_A + N_D)\,\phi_0}} \approx \sqrt{\frac{q\,\varepsilon_{Si}\,N_A}{2\,\phi_0}} \tag{9.20}$$

Also note that the subthreshold current in deep-submicron transistors can significantly exceed the reverse conduction current, especially for $V_{DS} = V_{DD}$. In long-channel transistors, the magnitude of the subthreshold current can be comparable to that of the reverse leakage current. The reverse conduction current in turn has two main components, the constant reverse saturation current I_0, and the generation current I_{gen} which originates in the depletion region and is a function of the applied bias voltage V_x.

To estimate the actual charge leakage time from the soft node, we have to solve the differential equation given in (9.17), taking into account the voltage-dependent capacitance components and the nonlinear leakage currents. For a quick estimate of the worst-case leakage behavior, on the other hand, the problem can be further simplified.

Assume that the *minimum* combined soft-node capacitance is given as

$$C_{x,min} = C_{gb} + C_{poly} + C_{metal} + C_{db,min} \tag{9.21}$$

where $C_{db,min}$ represents the minimum junction capacitance, obtained under the bias condition $V_x = V_{max}$. Now we define the *worst-case holding time* (t_{hold}) as the shortest time required for the soft-node voltage to drop from its initial logic-high value to the logic threshold voltage due to leakage. Once the soft-node voltage reaches the logic threshold, the logic stage being driven by this node will lose its previously held state.

$$t_{hold} = \frac{\Delta Q_{critical,min}}{I_{leakage,max}} \tag{9.22}$$

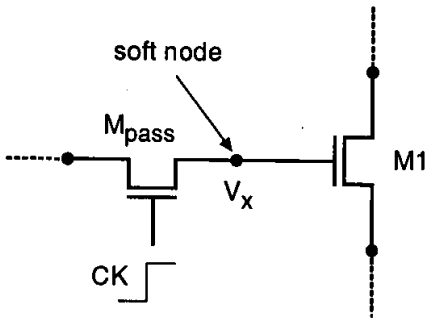
where

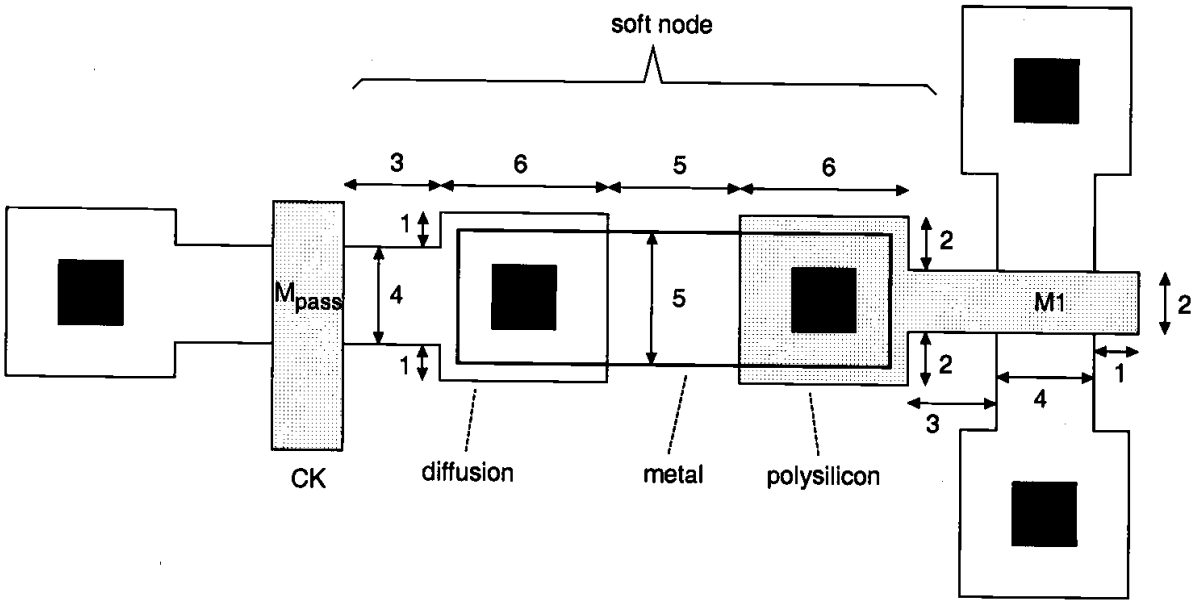
$$\Delta Q_{critical,min} = C_{x,min}\left(V_{max} - \frac{V_{DD}}{2}\right) \tag{9.23}$$

The calculation of the worst-case leakage time can be simplified with this approximation, as will be shown in the following example.

Example 9.2.

Consider the soft-node structure shown below, which consists of the drain (or source, depending on current direction) terminal of the pass transistor, connected to the polysilicon gate of an nMOS driver transistor via a metal interconnect.





We will assume that the power supply voltage used in this circuit is $V_{DD} = 5$ V, and that the soft node has initially been charged up to its maximum voltage, V_{max}. In order to estimate the worst-case holding time, the total soft-node capacitance must be calculated first. The simplified mask layout of the structure is shown in the following. All dimensions are given in micrometers. The critical material parameters to be used in this example are listed below.

$$V_{T0} = 0.8 \text{ V}$$
$$\gamma = 0.4 \text{ V}^{1/2}$$
$$|2\phi_F| = 0.6 \text{ V}$$

$$C_{ox} = 0.065 \text{ fF}/\mu\text{m}^2$$
$$C'_{metal} = 0.036 \text{ fF}/\mu\text{m}^2$$
$$C'_{poly} = 0.055 \text{ fF}/\mu\text{m}^2$$
$$C_{j0} = 0.095 \text{ fF}/\mu\text{m}^2$$
$$C_{j0sw} = 0.2 \text{ fF}/\mu\text{m}$$

First, we calculate the oxide-related (constant) parasitic capacitance components associated with the soft node.

$$\begin{aligned} C_{gb} &= C_{ox} \cdot W \cdot L_{mask} \\ &= 0.065 \text{ fF}/\mu\text{m}^2 \cdot (4\ \mu\text{m} \times 2\ \mu\text{m}) \\ &= 0.52 \text{ fF} \end{aligned}$$

$$\begin{aligned} C_{metal} &= 0.036 \text{ fF}/\mu\text{m}^2 \cdot (5\ \mu\text{m} \times 5\ \mu\text{m}) \\ &= 0.90 \text{ fF} \end{aligned}$$

$$\begin{aligned} C_{poly} &= 0.055 \text{ fF}/\mu\text{m}^2 \cdot (36\ \mu\text{m}^2 + 8\ \mu\text{m}^2) \\ &= 2.42 \text{ fF} \end{aligned}$$

Now, we have to calculate the parasitic junction capacitance associated with the drain-substrate pn-junction of the pass transistor. Using the zero-bias unit capacitance values given here, we obtain

$$\begin{aligned} C_{db,max} &= C_{bottom} + C_{sidewall} \\ &= A_{bottom} \cdot C_{j0} + P_{sidewall} \cdot C_{j0sw} \\ &= (36\ \mu\text{m}^2 + 12\ \mu\text{m}^2) \cdot 0.095 \text{ fF}/\mu\text{m}^2 + 30\ \mu\text{m} \cdot 0.2 \text{ fF}/\mu\text{m} \\ &= 4.56 \text{ fF} + 6.0 \text{ fF} \\ &= 10.56 \text{ fF} \end{aligned}$$

The minimum value of the drain junction capacitance is achieved when the junction is biased (in reverse) with its maximum possible voltage, V_{max}. In order to calculate the minimum capacitance value, we first find V_{max} using (9.5), as follows.

$$V_{max} = 5.0 - 0.8 - 0.4\left(\sqrt{0.6 + V_{max}} - \sqrt{0.6}\right)$$

$$\Rightarrow V_{max} = 3.68 \text{ V}$$

Now, the minimum value of the drain junction capacitance can be calculated.

$$C_{db,min} = \frac{C_{bottom}}{\sqrt{1+\frac{V_{x,max}}{\phi_0}}} + \frac{C_{sidewall}}{\sqrt{1+\frac{V_{x,max}}{\phi_{0sw}}}}$$
$$= \frac{4.56\ \text{fF}}{\sqrt{1+\frac{3.68}{0.88}}} + \frac{6.0\ \text{fF}}{\sqrt{1+\frac{3.68}{0.95}}} = 4.71\ \text{fF}$$

The minimum value of the total soft-node capacitance is found by using (9.21).

$$C_{x,min} = C_{gb} + C_{metal} + C_{poly} + C_{db,min}$$
$$= 0.52\ \text{fF} + 0.90\ \text{fF} + 2.42\ \text{fF} + 4.71\ \text{fF}$$
$$= 8.55\ \text{fF}$$

The amount of the critical charge drop in the soft node, which will eventually cause a change of logic state, is

$$\Delta Q_{critical} = C_{x,min} \cdot \left(V_{x,max} - \frac{V_{DD}}{2} \right)$$
$$= 8.55\ \text{fF} \cdot (3.68\ \text{V} - 2.5\ \text{V})$$
$$= 10.09\ \text{fC}$$

assuming that the logic threshold voltage of the next gate is (V_{DD}/2). In this example, the maximum leakage current responsible for charge depletion is given from the MOS characteristics (cf. equation (3.92) in Chapter 3) and the junction diode characteristics as

$$I_{leakage} = I_{subthreshold} + I_{reverse} = 0.85\ \text{pA}$$

Finally, we calculate the worst-case (minimum) hold time for the soft node using the expression (9.22).

$$t_{hold,min} = \frac{\Delta Q_{critical}}{I_{leakage,max}}$$
$$= \frac{10.09\ \text{fC}}{0.85\ \text{pA}} = \underline{\underline{11.87\ \text{ms}}}$$

It is interesting to note that even with a very small soft-node capacitance of 8.55 fF, the worst-case hold time for this structure is relatively long, especially compared with the signal propagation delays encountered in nMOS or CMOS logic gates. This example proves the feasibility of the dynamic charge storage concept and shows that a logic state can be safely preserved in a soft node for long time periods.