CHAPTER 9

DYNAMIC LOGIC CIRCUITS

9.1. Introduction

A wide range of static combinational and sequential logic circuits was introduced in the previous chapters. Static logic circuits allow versatile implementation of logic functions based on static, or steady-state, behavior of simple nMOS or CMOS structures. In other words, all valid output levels in static gates are associated with steady-state operating points of the circuit in question. Hence, a typical static logic gate generates its output corresponding to the applied input voltages after a certain time delay, and it can preserve its output level (or state) as long as the power supply is provided. This approach, however, may require a large number of transistors to implement a function, and may cause a considerable time delay.

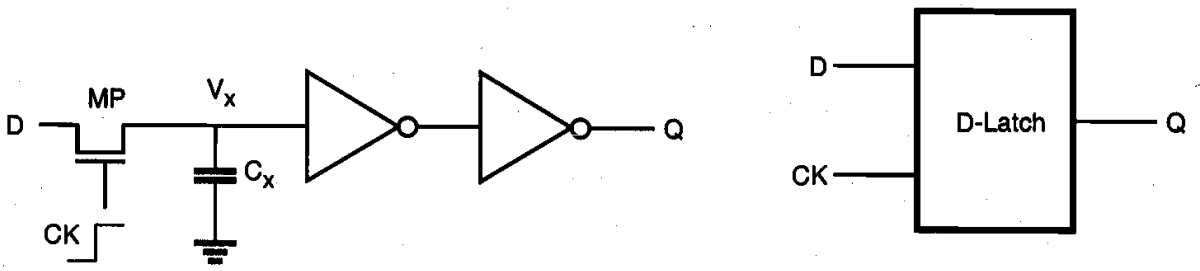
In high-density, high-performance digital implementations where reduction of circuit delay and silicon area is a major objective, *dynamic logic circuits* offer several significant advantages over static logic circuits. The operation of all dynamic logic gates depends on temporary (transient) storage of charge in parasitic node capacitances, instead of relying on steady-state circuit behavior. This operational property necessitates periodic updating of internal node voltage levels, since stored charge in a capacitor cannot be retained indefinitely. Consequently, dynamic logic circuits require periodic clock signals in order to control charge refreshing. The capability of temporarily storing a state, i.e., a voltage level, at a capacitive node allows us to implement very simple

sequential circuits with memory functions. Also, the use of common clock signals throughout the system enables us to *synchronize* the operations of various circuit blocks. As a result, dynamic circuit techniques lend themselves well to synchronous logic design. Finally, the dynamic logic implementation of complex functions generally requires a smaller silicon area than does the static logic implementation. As for the power consumption which increases with the parasitic capacitances, the dynamic circuit implementation in a smaller area will, in many cases, consume less power than the static counterpart, despite its use of clock signals.

The following example presents the operation of a dynamic D-latch circuit, which essentially consists of two inverters connected in cascade. This simple circuit illustrates most of the basic operational concepts involved in dynamic circuit design.

Example 9.1.

Consider the dynamic D-latch circuit shown below. The circuit consists of two cascaded inverters and one nMOS pass transistor driving the input of the primary inverter stage.



We will see that the parasitic input capacitance C_x of the primary inverter stage plays an important role in the dynamic operation of this circuit. The input pass transistor is being driven by the external periodic clock signal, as follows:

- When the clock is high (CK = 1), the pass transistor turns on. The capacitor C_x is either charged up, or charged down through the pass transistor MP, depending on the input (D) voltage level. The output (Q) assumes the same logic level as the input.

- When the clock is low (CK = 0), the pass transistor MP turns off, and the capacitor C_x is isolated from the input D. Since there is no current path from the intermediate node X to either V_{DD} or ground, the amount of charge stored in C_x during the previous cycle determines the output voltage level Q.

It can easily be seen that this circuit performs the function of a simple D-latch. In fact, the transistor count can be reduced by removing the last inverter stage if the latch output can be inverted. This option will be elaborated on in Section 9.2. The "hold" operation during the inactive clock cycle is accomplished by temporarily storing charge in the parasitic capacitance C_x. Correct operation of the circuit critically depends on how long

a sufficient amount of charge can be retained at node X, before the output state changes due to charge leakage. Therefore, the capacitive intermediate node X is also called a *soft node*. The nature of the soft node makes the dynamic circuits more vulnerable to the so-called single-event upsets (SEUs) caused by α-particle or cosmic ray hits in integrated circuits.

In the following, we will examine the circuit operation in more detail. Assume that the dynamic D-latch circuit is being operated with a power supply voltage of $V_{DD} = 5$ V, and that the VTC of both inverters are identical, with

$$V_{OL} = 0 \text{ V}$$
$$V_{IL} = 2.1 \text{ V}$$
$$V_{IH} = 2.9 \text{ V}$$
$$V_{OH} = 5.0 \text{ V}$$

Furthermore, the threshold voltage of the pass transistor MP is given as $V_{T,n} = 0.8$ V. During the active clock phase (CK = 1), assume that the input is equal to logic "1," i.e., $V_{in} = V_{OH} = 5$ V. The pass transistor MP is conducting during this phase, and the parasitic intermediate node capacitance C_x is charged up to a logic-high level. We recall that the nMOS pass transistor is a poor conductor for logic "1," and its output voltage V_x will be *lower than* V_{OH}, by one threshold voltage: $V_x = 5.0 - 0.8 = 4.2$ V. Still, this voltage is clearly higher than the V_{IH} of the first inverter, thus, the output voltage of the first inverter will be very close to $V_{OL} = 0$ V. Consequently, the output level Q of the secondary inverter becomes a logic "1," $V_Q = V_{DD}$.

Next, the clock signal goes to zero, and the pass transistor turns off. Initially, the logic-high level at node X is preserved through charge storage in C_x. Thus, the output level Q also remains at logic "1." However, the voltage V_x eventually starts to drop from its original level of 4.2 V because of charge leakage from the soft node. It can easily be seen that in order to keep the output node Q at logic "1," the voltage level at the intermediate node X cannot be allowed to drop lower than $V_{IH} = 2.9$ V (once V_x falls *below* this level, the input of the first inverter cannot be interpreted as a logic "1"). Thus, the inactive clock phase during which the clock signal is equal to zero can, at most, be as long as it takes for the intermediate voltage V_x to drop from 4.2 V to 2.9 V, due to charge leakage. To avoid an erroneous output, the charge stored in C_x must be restored, or refreshed, to its original level before V_x reaches 2.9 V.

This example shows that the simple dynamic-charge storage principle employed in the D-latch circuit is quite feasible for preserving an output state during the inactive clock phase, assuming that the leakage currents responsible for draining the capacitance C_x are relatively small. In the following, we will examine the charge-up and charge-down events for the soft-node capacitance C_x in greater detail.

9.2. Basic Principles of Pass Transistor Circuits

The fundamental building block of nMOS dynamic logic circuits, consisting of an nMOS pass transistor driving the gate of another nMOS transistor, is shown in Fig. 9.1. As

already discussed in Example 9.1, the pass transistor MP is driven by the periodic clock signal and acts as an access switch to either charge up or charge down the parasitic capacitance C_x, depending on the input signal V_{in}. Thus, the two possible operations when the clock signal is active (CK = 1) are the logic "1" transfer (charging up the capacitance C_x to a logic-high level) and the logic "0" transfer (charging down the capacitance C_x to a logic-low level). In either case, the output of the depletion-load nMOS inverter obviously assumes a logic-low or a logic-high level, depending on the voltage V_x.

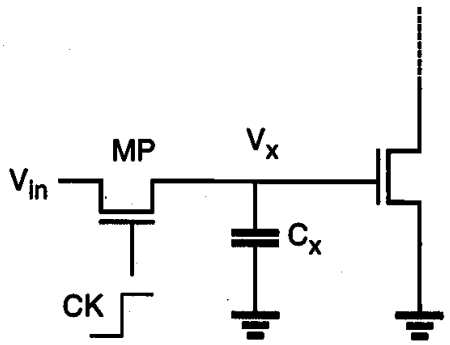


Figure 9.1. The basic building block for nMOS dynamic logic, which consists of an nMOS pass transistor driving the gate of another nMOS transistor.

Notice that the pass transistor MP provides the only current path to the intermediate capacitive node (soft node) X. When the clock signal becomes inactive (CK = 0), the pass transistor ceases to conduct and the charge stored in the parasitic capacitor C_x continues to determine the output level of the inverter. In the following, we will first examine the charge-up event.

Logic "1" Transfer

Assume that the soft node voltage is equal to 0 initially, i.e., $V_x(t = 0) = 0$ V. A logic "1" level is applied to the input terminal, which corresponds to $V_{in} = V_{OH} = V_{DD}$. Now, the clock signal at the gate of the pass transistor goes from 0 to V_{DD} at $t = 0$. It can be seen that the pass transistor MP starts to conduct as soon as the clock signal becomes active and that MP will operate in saturation throughout this cycle since $V_{DS} = V_{GS}$. Consequently, $V_{DS} > V_{GS} - V_{T,n}$. The circuit to be analyzed for the logic "1" transfer event can be simplified into an equivalent circuit as shown in Fig. 9.2.

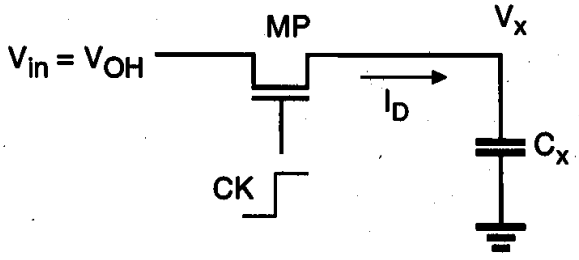


Figure 9.2. Equivalent circuit for the logic "1" transfer event.

The pass transistor MP operating in the saturation region starts to charge up the capacitor C_x, thus,

$$C_x \frac{dV_x}{dt} = \frac{k_n}{2}\left(V_{DD} - V_x - V_{T,n}\right)^2 \tag{9.1}$$

Note that the threshold voltage of the pass transistor is actually subject to substrate bias effect and therefore, depends on the voltage level V_x. To simplify our analysis, we will neglect the substrate bias effect at this point. Integrating (9.1), we obtain

$$\int_0^t dt = \frac{2C_x}{k_n}\int_0^{V_x} \frac{dV_x}{\left(V_{DD} - V_x - V_{T,n}\right)^2}$$

$$= \frac{2C_x}{k_n}\left(\frac{1}{\left(V_{DD} - V_x - V_{T,n}\right)}\right)\Bigg|_0^{V_x} \tag{9.2}$$

$$t = \frac{2C_x}{k_n}\left[\left(\frac{1}{V_{DD} - V_x - V_{T,n}}\right) - \left(\frac{1}{V_{DD} - V_{T,n}}\right)\right] \tag{9.3}$$

This equation can be solved for $V_x(t)$, as follows.

$$V_x(t) = \left(V_{DD} - V_{T,n}\right)\frac{\left(\frac{k_n\left(V_{DD} - V_{T,n}\right)}{2C_x}\right)t}{1 + \left(\frac{k_n\left(V_{DD} - V_{T,n}\right)}{2C_x}\right)t} \tag{9.4}$$

The variation of the node voltage V_x according to (9.4) is plotted as a function of time in Fig. 9.3. The voltage rises from its initial value of 0 V and approaches a limit value for large t, but it cannot exceed its limit value of $V_{max} = (V_{DD} - V_{T,n})$. The pass transistor will turn off when $V_x = V_{max}$, since at this point, its gate-to-source voltage will be equal to its threshold voltage. Therefore, the voltage at node X can never attain the full power supply voltage level of V_{DD} during the logic "1" transfer. The actual value of the maximum possible voltage V_{max} at node X can be found by taking into account the substrate bias effect for MP.

$$V_{max} = V_x\big|_{t\to\infty} = V_{DD} - V_{T,n}$$

$$= V_{DD} - V_{T0,n} - \gamma\left(\sqrt{|2\phi_F| + V_{max}} - \sqrt{|2\phi_F|}\right) \tag{9.5}$$

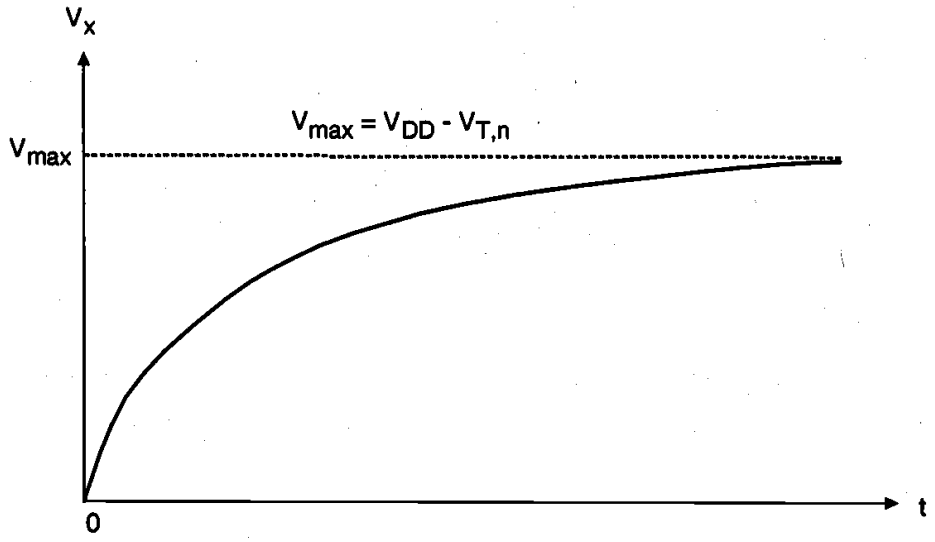


Figure 9.3. Variation of V_x as a function of time during logic "1" transfer.

Thus, the voltage V_x which is obtained at node X following a logic "1" transfer can be considerably lower than V_{DD}. Also note that the rise time of the voltage V_x will be *underestimated* if the zero-bias threshold voltage V_{T0} is used in (9.3). In that case, the actual charge-up time will be longer than predicted by (9.3), because the drain current of the nMOS transistor is decreased due to the substrate bias effect.

The fact that the node voltage V_x has an upper limit of $V_{max} = (V_{DD} - V_{T,n})$ has a significant implication for circuit design. As an example, consider the following case in which a logic "1" at the input node ($V_{in} = V_{DD}$) is being transferred through a chain of cascaded pass transistors (Fig. 9.4). For simple analysis, we assume that initially all internal node voltages, V_1 through V_4, are zero. The first pass transistor M1 operates in saturation with $V_{DS1} > V_{GS1} - V_{T,n1}$. Therefore, the voltage at node 1 cannot exceed the limit value $V_{max1} = (V_{DD} - V_{T,n1})$. Now, assuming that the pass transistors in this circuit are identical, the second pass transistor M2 operates at the *saturation boundary*. As a result, the voltage at node 2 will be equal to $V_{max2} = (V_{DD} - V_{T,n2})$. It can easily be seen that with $V_{T,n1} = V_{T,n2} = V_{T,n3} = \ldots$, the node voltage at the end of the pass transistor chain will become one threshold voltage lower than V_{DD}, regardless of the number of pass transistors in the chain. It can be observed that the steady-state internal node voltages in this circuit are always one threshold voltage below V_{DD}, regardless of the initial voltages.

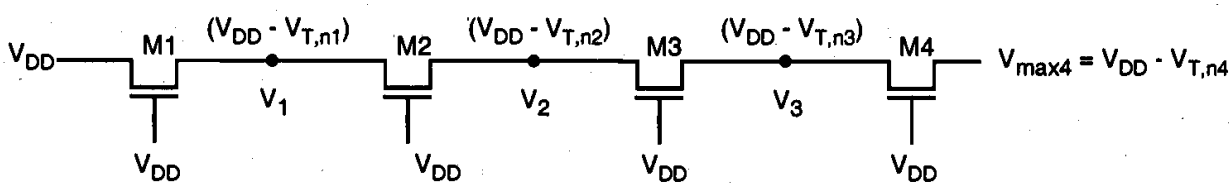


Figure 9.4. Node voltages in a pass-transistor chain during the logic "1" transfer.

Now consider a different case in which the output of each pass transistor drives the gate of another pass transistor, as depicted in Fig. 9.5.

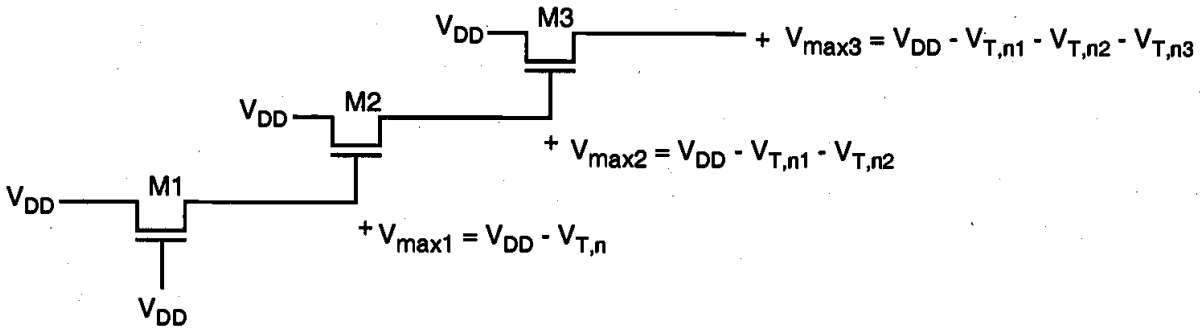


Figure 9.5. Node voltages during the logic "1" transfer, when each pass transistor is driving another pass transistor.

Here, the output of the first pass transistor M1 can reach the limit $V_{max1} = (V_{DD} - V_{T,n1})$. This voltage drives the gate of the second pass transistor, which also operates in the saturation region. Its gate-to-source voltage cannot exceed $V_{Tn,2}$, hence, the upper limit for V_2 is found as $V_{max2} = V_{DD} - V_{T,n1} - V_{T,n2}$. It can be seen that in this case, each stage causes a significant loss of voltage level. The amount of voltage drop at each stage can be approximated more realistically by taking into account the corresponding substrate bias effect, which is different in all stages.

$$V_{T,n1} = V_{T0,n} - \gamma\left(\sqrt{|2\phi_F| + V_{max1}} - \sqrt{|2\phi_F|}\right)$$

$$V_{T,n2} = V_{T0,n} - \gamma\left(\sqrt{|2\phi_F| + V_{max2}} - \sqrt{|2\phi_F|}\right) \qquad (9.6)$$

$$\vdots$$

The preceding analysis helped us to examine important characteristics of the logic "1" transfer event. Next, we will examine the charge-down event, which is also called a logic "0" transfer.

Logic "0" Transfer

Assume that the soft-node voltage V_x is equal to a logic "1" level initially, i.e., $V_x(t = 0) = V_{max} = (V_{DD} - V_{T,n})$. A logic "0" level is applied to the input terminal, which corresponds to $V_{in} = 0$ V. Now, the clock signal at the gate of the pass transistor goes from 0 to V_{DD} at $t = 0$. The pass transistor MP starts to conduct as soon as the clock signal becomes active, and the direction of drain current flow through MP will be opposite to that during the charge-up (logic "1" transfer) event. This means that the intermediate node X will now correspond to the drain terminal of MP and that the input node will correspond to its source terminal. With $V_{GS} = V_{DD}$ and $V_{DS} = V_{max}$, it can be seen that the pass transistor operates in the linear region throughout this cycle, since $V_{DS} < V_{GS} - V_{T,n}$.

The circuit to be analyzed for the logic "0" transfer event can be simplified into an equivalent circuit as shown in Fig. 9.6. As in the logic "1" transfer case, the depletion-load nMOS inverter does not affect this event.

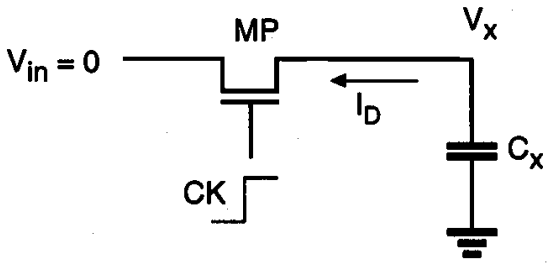


Figure 9.6. Equivalent circuit for the logic "0" transfer event.

The pass transistor MP operating in the linear region discharges the parasitic capacitor C_x, as follows:

$$-C_x \frac{dV_x}{dt} = \frac{k_n}{2}\left(2\left(V_{DD} - V_{T,n}\right)V_x - V_x^2\right) \tag{9.7}$$

$$dt = -\frac{2C_x}{k_n} \cdot \frac{dV_x}{2\left(V_{DD} - V_{T,n}\right)V_x - V_x^2} \tag{9.8}$$

Note that the source voltage of the nMOS pass transistor is equal to 0 V during this event; hence, there is no substrate bias effect for MP ($V_{T,n} = V_{T0,n}$). But the initial condition $V_x(t=0) = (V_{DD} - V_{T,n})$ contains the threshold voltage *with* substrate bias effect, because the voltage V_x is set during the preceding logic "1" transfer event. To simplify the expressions, we will use $V_{T,n}$ in the following. Integrating both sides of (9.8) yields

$$\int_0^t dt = -\frac{2C_x}{k_n}\int_{V_{DD}-V_{T,n}}^{V_x}\left(\frac{\frac{1}{2\left(V_{DD}-V_{T,n}\right)}}{2\left(V_{DD}-V_{T,n}\right)-V_x} + \frac{\frac{1}{2\left(V_{DD}-V_{T,n}\right)}}{V_x}\right)dV_x \tag{9.9}$$

$$t = \frac{C_x}{k_n\left(V_{DD}-V_{T,n}\right)}\left[\ln\left(\frac{2\left(V_{DD}-V_{T,n}\right)-V_x}{V_x}\right)\right]\Bigg|_{V_{DD}-V_{T,n}}^{V_x} \tag{9.10}$$

Finally, the fall-time expression for the node voltage V_x can be obtained as

$$t = \frac{C_x}{k_n\left(V_{DD}-V_{T,n}\right)}\ln\left(\frac{2\left(V_{DD}-V_{T,n}\right)-V_x}{V_x}\right) \tag{9.11}$$

The variation of the node voltage V_x according to (9.11) is plotted as a function of time in Fig. 9.7. It is seen that the voltage drops from its logic-high level of V_{max} to 0 V. Hence, unlike the charge-up case, the applied input voltage level (logic 0) can be transferred to the soft node without any modification during this event.

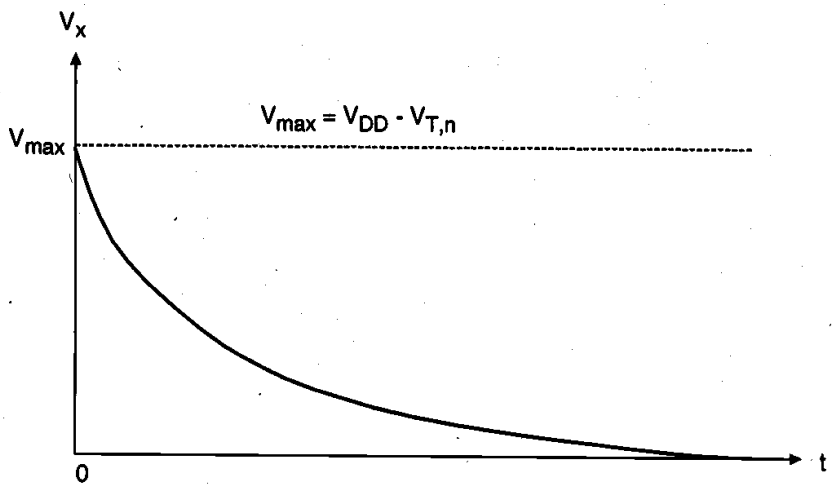


Figure 9.7. Variation of V_x as a function of time during logic "0" transfer.

The fall time (τ_{fall}) for the soft-node voltage V_x can be calculated from (9.11) as follows. First, define the two time points $t_{90\%}$ and $t_{10\%}$ as the times at which the node voltage is equal to 0.9 V_{max} and 0.1 V_{max}, respectively. These two time points can easily be found by using (9.11).

$$t_{90\%} = \frac{C_x}{k_n\left(V_{DD}-V_{T,n}\right)}\ln\left(\frac{(2-0.9)\left(V_{DD}-V_{T,n}\right)}{0.9\left(V_{DD}-V_{T,n}\right)}\right)$$
$$= \frac{C_x}{k_n\left(V_{DD}-V_{T,n}\right)}\ln\left(\frac{1.1}{0.9}\right) \tag{9.12}$$

$$t_{10\%} = \frac{C_x}{k_n\left(V_{DD}-V_{T,n}\right)}\ln\left(\frac{1.9}{0.1}\right) \tag{9.13}$$

The fall time of the soft-node voltage V_x is by definition the difference between $t_{10\%}$ and $t_{90\%}$, which is found as

$$\tau_{fall} = t_{10\%} - t_{90\%}$$
$$= \frac{C_x}{k_n\left(V_{DD}-V_{T,n}\right)}\left[\ln(19)-\ln(1.22)\right]$$
$$= 2.74\frac{C_x}{k_n\left(V_{DD}-V_{T,n}\right)} \tag{9.14}$$

Until this point, we have examined the transient charge-up and charge-down events which are responsible for logic "1" transfer and logic "0" transfer during the active clock phase, i.e., when CK = 1. Now we will turn our attention to the storage of logic levels at the soft node X during the inactive clock cycle, i.e., when CK = 0.

Charge Storage and Charge Leakage

As already discussed qualitatively in the preceding section, the preservation of a correct logic level at the soft node during the inactive clock phase depends on preserving a sufficient amount of charge in C_x, despite the leakage currents. To analyze the events during the inactive clock phase in more detail, consider the scenario shown in Fig. 9.8 below. We will assume that a logic-high voltage level has been transferred to the soft node during the active clock phase and that now both the input voltage V_{in} and the clock are equal to 0 V. The charge stored in C_x will gradually leak away, primarily due to the leakage currents associated with the pass transistor. The gate current of the inverter driver transistor is negligible for all practical purposes.

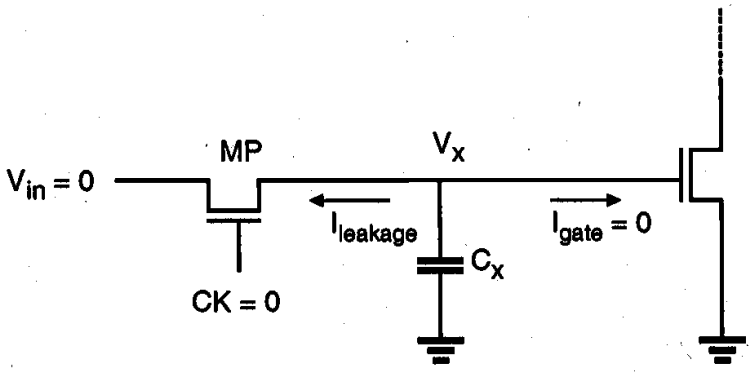


Figure 9.8. Charge leakage from the soft node.

Figure 9.9 shows a simplified cross-section of the nMOS pass transistor, together with the lumped node capacitance C_x. We see that the leakage current responsible for draining the soft-node capacitance over time has two main components, namely, the subthreshold channel current and the reverse conduction current of the drain-substrate junction.

$$I_{leakage} = I_{subthreshold(MP)} + I_{reverse(MP)} \tag{9.15}$$

Note that a certain portion of the total soft-node capacitance C_x is due to the reverse biased drain-substrate junction, which is also a function of the soft-node voltage V_x. Other components of C_x, which are primarily due to oxide-related parasitics, can be considered constants. In our analysis, these constant capacitance components will be represented by C_{in} (Fig. 9.10). Thus, we have to express the total charge stored in the soft node as the sum of two main components, as follows.

$$Q = Q_j(V_x) + Q_{in} \quad \text{where} \quad Q_{in} = C_{in} \cdot V_x$$

$$C_{in} = C_{gb} + C_{poly} + C_{metal} \tag{9.16}$$

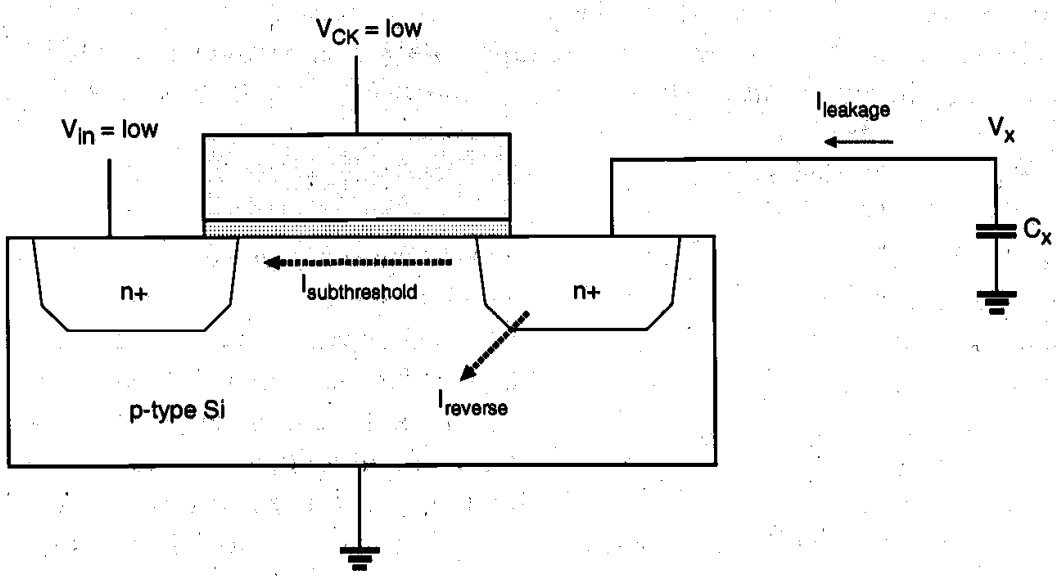


Figure 9.9. Simplified cross-section of the nMOS pass transistor, showing the leakage current components responsible for draining the soft-node capacitance C_x.

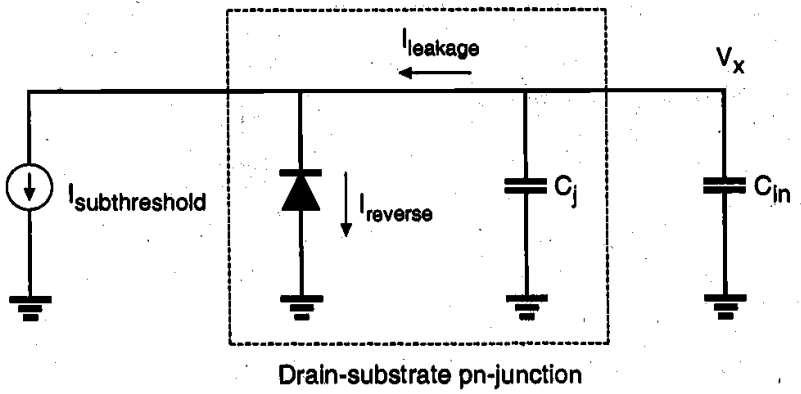


Figure 9.10. Equivalent circuit used for analyzing the charge leakage process.

The total leakage current can be expressed as the time derivative of the total soft-node charge Q.

$$\begin{aligned} I_{leakage} &= \frac{dQ}{dt} \\ &= \frac{dQ_j(V_x)}{dt} + \frac{dQ_{in}}{dt} \\ &= \frac{dQ_j(V_x)}{dV_x}\frac{dV_x}{dt} + C_{in}\frac{dV_x}{dt} \end{aligned} \tag{9.17}$$