```vhdl
1
2     ----------------------------Multiplexer (3 Bit) - chooses between Ea and Eb--------------------
3
4     library IEEE;
5     use IEEE.STD_LOGIC_1164.ALL;
6     use IEEE.NUMERIC_STD.ALL;
7
8     entity MUX is
9         Port ( Ea : in  UNSIGNED (2 downto 0);
10               Eb : in  UNSIGNED (2 downto 0);
11               Sign : in STD_LOGIC := '0';
12               ErTemp : out  UNSIGNED (2 downto 0));
13    end MUX;
14
15    architecture Behavioral of MUX is
16
17    begin
18    with Sign select
19       ErTemp <= Ea when '0',
20                 Eb when others;
21    end Behavioral;
22
23
```