```
1  ----------------------------------------------------------------------------------------------
2  ------------------------- COMPONENTS USED IN MAIN ARCHITECTURE-------------------------------
3  ----------------------------------------------------------------------------------------------
4
5  ------------------------- 1) INTEGER ADDER SUBTRACTOR----------------------------------------
6
7  library IEEE;
8  use IEEE.STD_LOGIC_1164.ALL;
9  use IEEE.NUMERIC_STD.ALL;
10
11 entity AdderSubtractor is
12     generic (N : natural := 7); --This is 8 bit adder-subtractor by default
13     Port ( InpA : in  UNSIGNED (N downto 0);
14            InpB : in  UNSIGNED (N downto 0);
15             Opr : in STD_LOGIC := '0'; -- '0' means Add(Default) , '1' means Subtract
16            Sum : out  Unsigned (N downto 0);
17            Error : out STD_LOGIC);
18 end AdderSubtractor;
19
20 architecture Behavioral of AdderSubtractor is
21
22 begin
23    process(Opr)
24    variable sum_ans : UNSIGNED (N downto 0);
25    variable carry_ans : UNSIGNED (N+1 downto 0);
26    variable InpBnew : UNSIGNED (N downto 0);
27    begin
28       carry_ans(0) := Opr;
29
30       for i in 0 to N loop
31          InpBnew(i) := InpB(i) xor Opr;
32          sum_ans(i) := (InpA(i) xor InpBnew(i)) xor carry_ans(i);
33          carry_ans(i+1) := (InpA(i) and InpBnew(i)) or (InpA(i) and carry_ans(i)) or (InpBnew(i) and carry_ans(i));
34       end loop;
35
36       Error <= (carry_ans(N) xor carry_ans(N+1)) or Carry_ans(N);
37       Sum <= sum_ans;
38
39    end process;
40
41 end Behavioral;
```