```
1
2   -------Contol Logic (Determines the final Sign of output and Add-subtract operation that need to be done)----
3
4   library IEEE;
5   use IEEE.STD_LOGIC_1164.ALL;
6
7   entity ControlLogic is
8       Port ( Sa : in  STD_LOGIC; --Sign of FP no. a
9              Sb : in  STD_LOGIC; --Sign of FP no. b
10             AS : in  STD_LOGIC; --The Operation Desired by the user
11             S4 : in  STD_LOGIC; --Sign of the mantissa difference
12             S3 : in  STD_LOGIC; --Sign of Exponent Difference
13             Sr : out  STD_LOGIC; --Sign of Final Result
14             AddSub : out  STD_LOGIC); --Operation signal to the mantissa adder or subtractor
15  end ControlLogic;
16
17  architecture Behavioral of ControlLogic is
18
19  begin
20
21     AddSub <= Sa xor Sb xor AS;
22     Sr <= (S4 and (not Sa)) or (Sa and (not S4) and (not S3)) or (AS and (not Sb) and S4) or (Sb and (not AS) and S3);
23
24  end Behavioral;
25
26
```