DLD Lab-05

Adders

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EL227 – Digital Logic Design-Lab

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Contents

1. Objectives:

To become familiar with the operation of adders

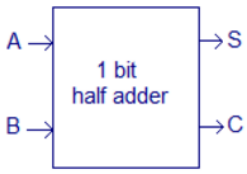
2. Equipment Required:

- DEV-2765E Trainer Board/ Multisim 14.2 /Logic.ly
- 7486 quad 2-input XOR gate IC
- 7404 Hex Inverter gate IC
- 7408 quad 2-input AND gate IC
- 7432 quad 2-input OR gate IC

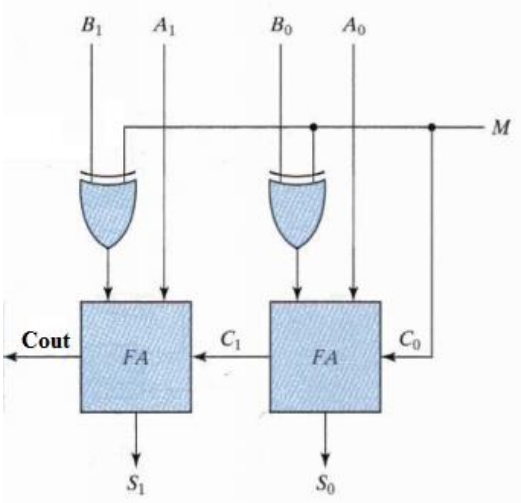
3. Description:

In this lab, we will learn the functionality of adders and subtractors through implementation. First of all we have to design a half adder, and then using two half adders implement a full adder.

Half adder have two binary inputs and two binary outputs. The Input variables designates the augend and addend bits; the output variables produce the sum and carry. Let suppose we assign symbols *A* and *B* to the two inputs and S (for sum) and C (for *carry)* to the outputs, the block diagram of half adder is shown in the figure below:



The addition and subtraction operations can be combined into one circuit with XOR gate for each full adder. The mode input M controls the operation. When M = 0, the circuit is an adder, and when M = 1, the circuit becomes a subtractor. Each XOR gate receives input M and one of the inputs of B. when M = 0, we have B$\oplus$0 = B. the full adder receive the value of B, the input carry is 0, and the circuit performs A plus B. when M = 1, we have B$\oplus$1= B' and C0 = 1. The B inputs are complemented and a 1 is added through the input carry.



4. Adder

Adder is a combinational circuit which perform addition of number (binary number)

In many computers and other kinds of processors adders are used in Arithmetic Logic Unit (ALU). calculate addresses, increment, decrement operation etc.

Basic types of Adder

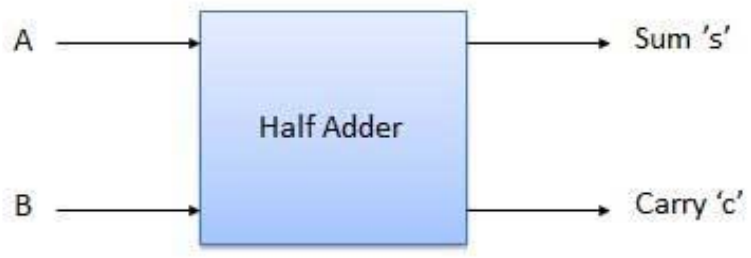
Half Adder

Full Adder

5. Half Adder

The half adder accepts two binary digits on its inputs and produce two binary digits outputs, a sum bit and a carry bit. In other words it is a combinational circuit which performs arithmetic addition of two one bit numbers It does not take carry from previous sum

Block Diagram



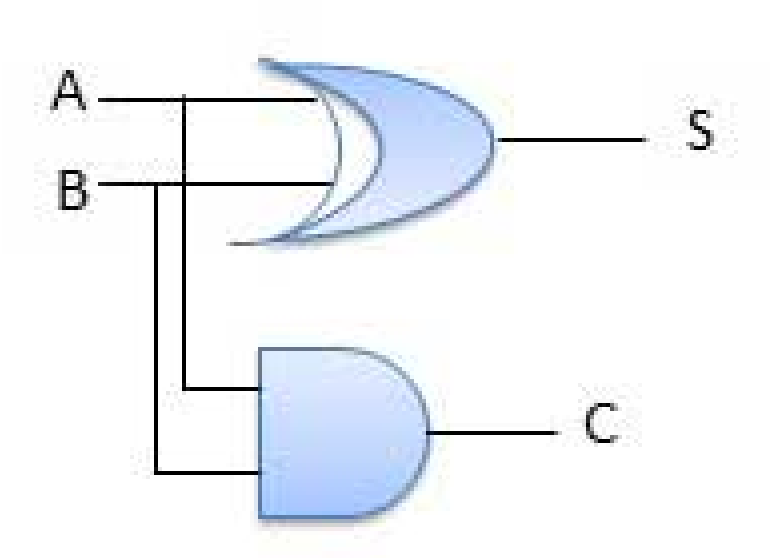
Truth Table

Inputs		Output
A	B	S C
0	0	0 0
0	1	1 0
1	0	1 0
1	1	0 1

6. Half Adder Circuit Diagram

S (Sum) **=** **= A'.B + A.B'**

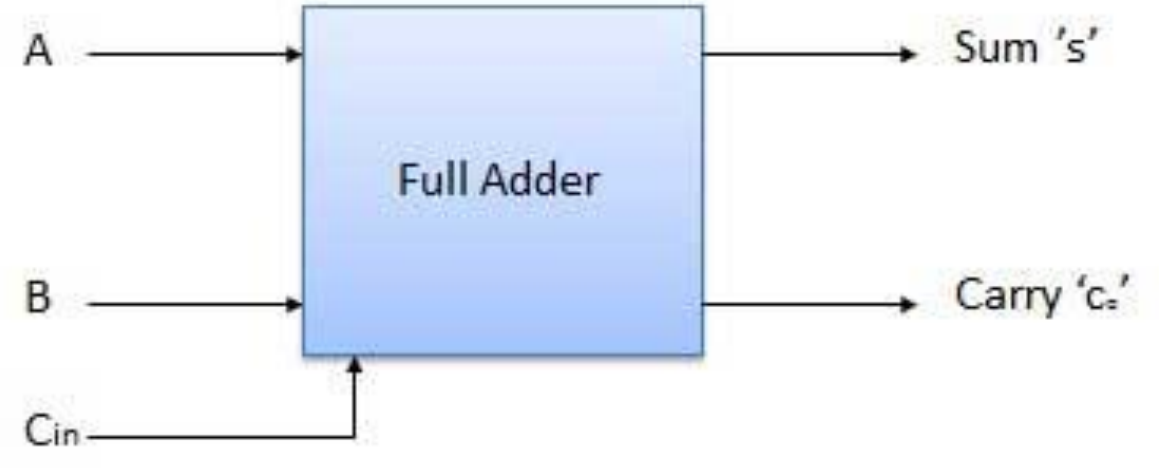
C (carry) **=** **A.B**



Inputs		Output	
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

7. Full Adder

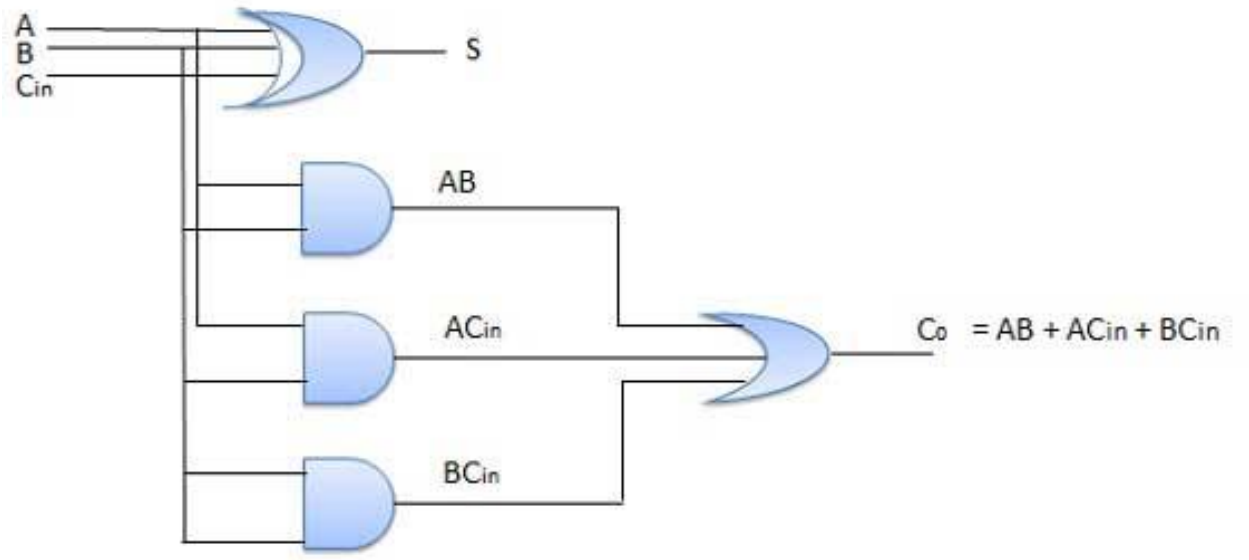
- The full adder accepts two inputs bits and an input carry and generates a sum output and an output carry.
- It can add two one-bit numbers A and B, and carry c.
- Full adder is developed to overcome the drawback of Half Adder circuit.



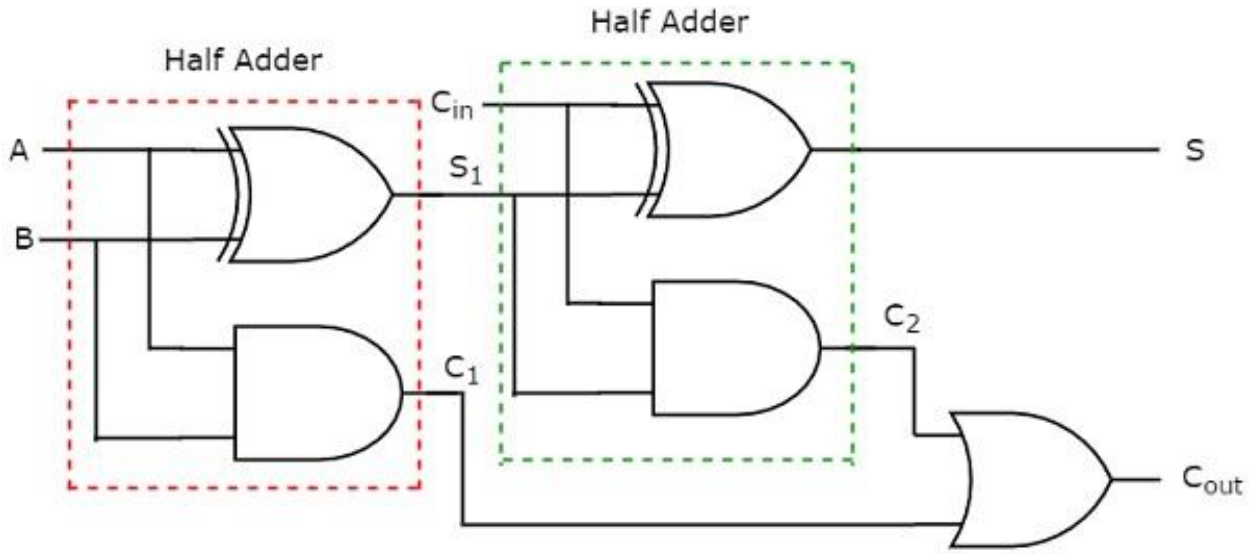
Inputs			Output	
A	B	Cin	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

8. Full Adder Circuit Diagram

- S (Sum) = $A \oplus B \oplus C$
- C (carry) = A.B + A.Cin + B.Cin

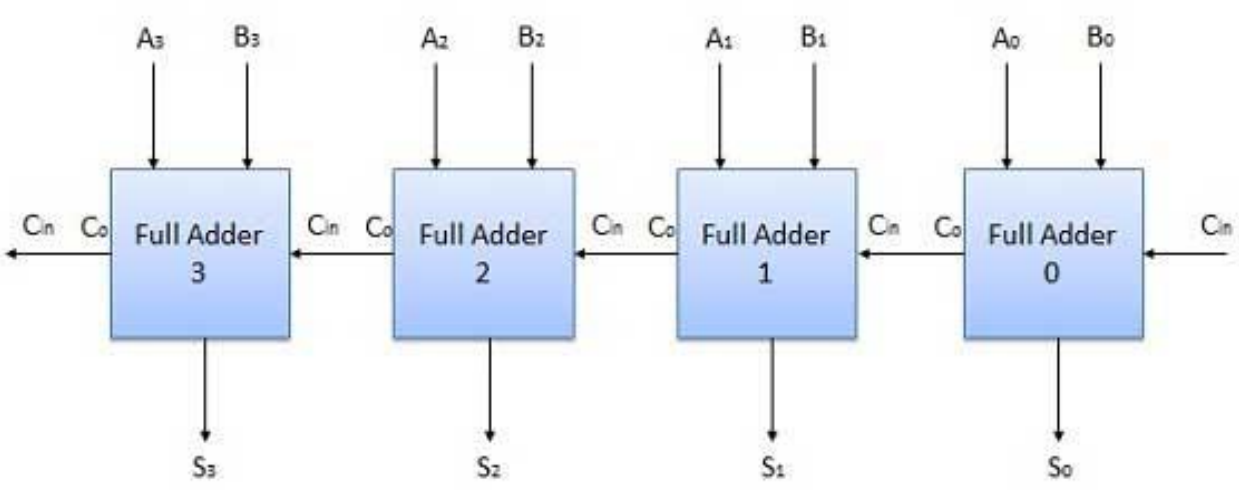


9. Full Adder Using Two Half Adder

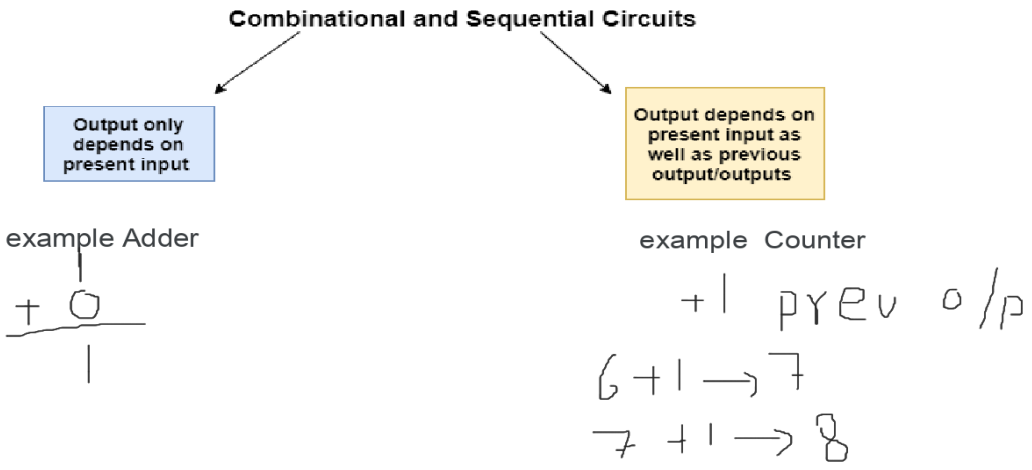


10. Four Bit Parallel Adder /Ripple Adder

- A = $A_3A_2A_1A_0$ assume A = 10111 , B = 11011
- B = $B_3B_2B_1B_0$



11. Combinational Vs Sequential Circuit



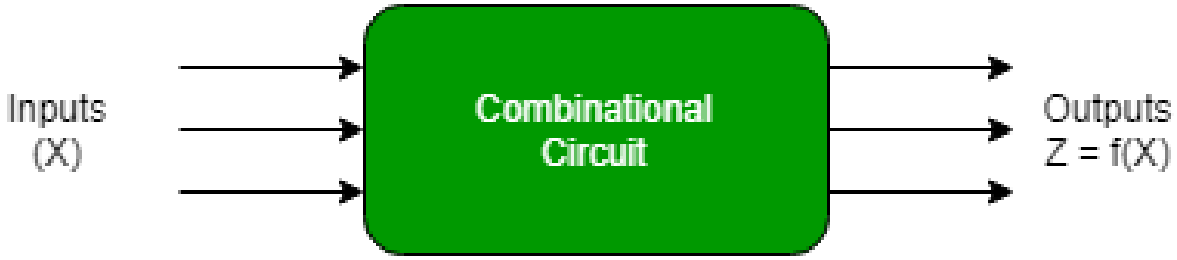


Figure: Combinational Circuits

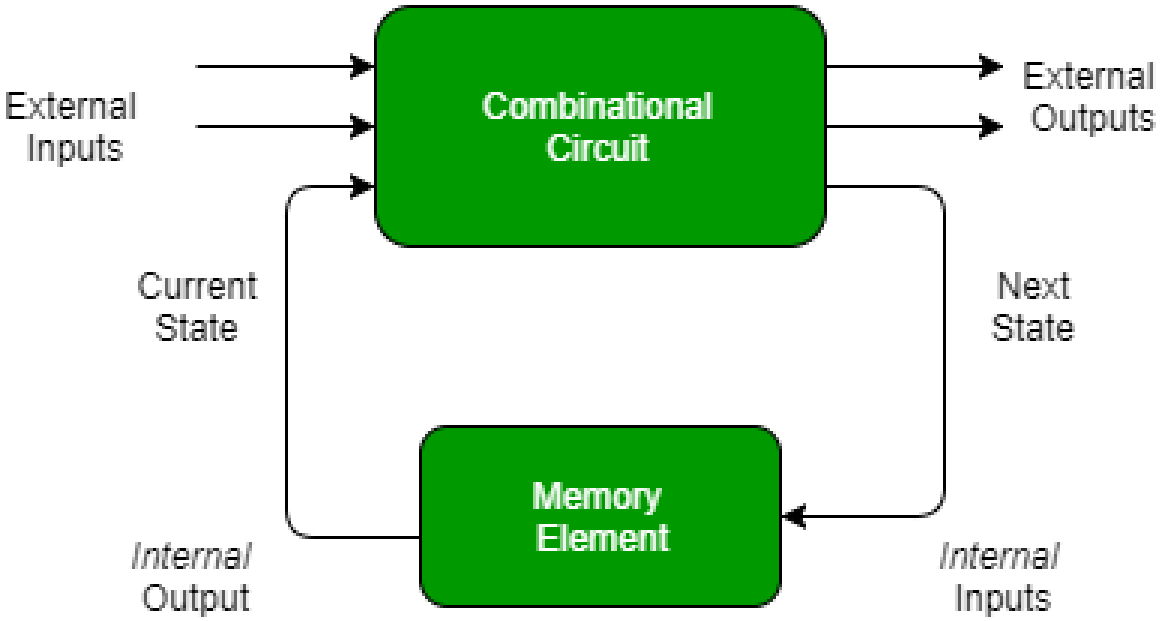


Figure: Sequential Circuit

12. Lab Task

- Implement Half adder and Full Adder Using Universal Gate
    - e.g
    - Design Truth Table
    - Design Logical Expression
    - Draw Circuit Diagram from Logical Expression
    - Implementation on logic.ly
- Implement Four Bit Parallel Adder /Ripple Adder (Using Basic and Universal Gate)
    - e.g
    - Design Truth Table
    - Design Logical Expression
    - Draw Circuit Diagram from Logical Expression
    - Implementation on logic.ly