DLD Lab-09

Multiplexer & De Multiplexer

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EL227 – Digital Logic Design-Lab

SEMESTER SPRING 2021

FEBRUARY 9, 2022

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Contents

1. Objectives:

- Design and implement the circuitry for a 4 to 1 Multiplexer.
- Test the functionality of a 1x4 DE multiplexer using the IC-74LS139
- Test the functionality of a 8x1 multiplexer using the IC-74LS151
- Test the functionality of a 4x1 multiplexer using the IC-74LS153Gaining a close insight into the functioning and properties of multiplexer (MUX) circuits
- Developing skills in the design and testing of combinational logic circuits.

2. Equipment Required:

- DEV-2765E Trainer Board/ Multisim 14.2 /Logic.ly
- 74LS04 Hex Inverter
- 74LS08 And gate
- 74LS32 OR gate
- 74LS151 (8-to-1 Multiplexer)
- 74LS153 (dual 4-to-1 Multiplexer)

3. Background Theory

A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs the information to a single output line. The selection of a particular input line is controlled by a set of input variables, called selection input. Normally, there are 2^n input lines and n selection inputs whose bit combination determines which input is selected.
A de multiplexer is doing the opposite function of multiplexer. It takes input on a single input line and the select lines determines one of the 2^n output lines and the input contents is visible on that particular output.

The multiplexer is a device that has multiple inputs and single line output. The select lines determine which input is connected to the output in other words
Multiplexer is a combinational circuit that has maximum of 2^n data inputs, 'n' selection lines and single output line.
Multiplexer is also called as Mux.

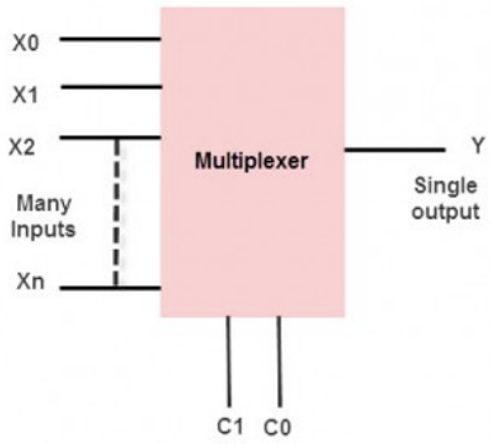
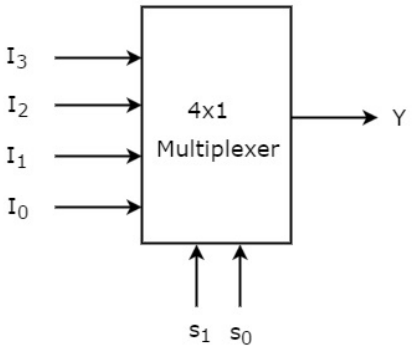


Figure 1

4. 4x1 Mux Contd.

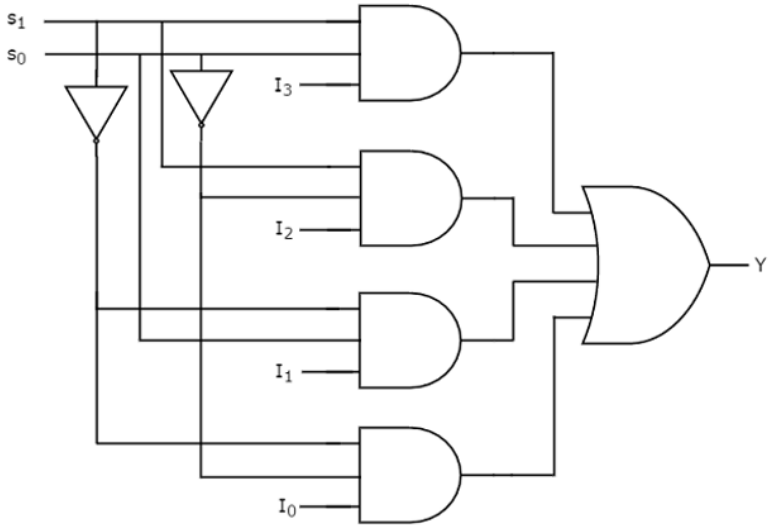
4x1 Multiplexer has four data inputs I_3, I_2, I_1 & I_0, two selection lines s_1 & s_0 and one output Y. The **block diagram** of 4x1 Multiplexer is shown in the following figure.

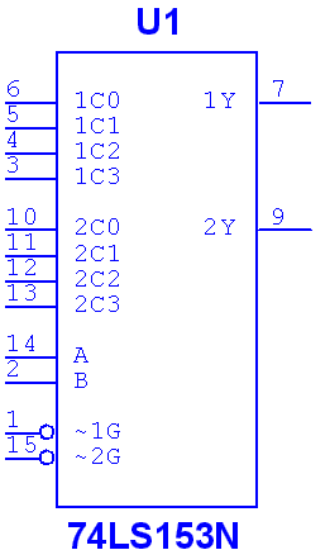


Selection Lines		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

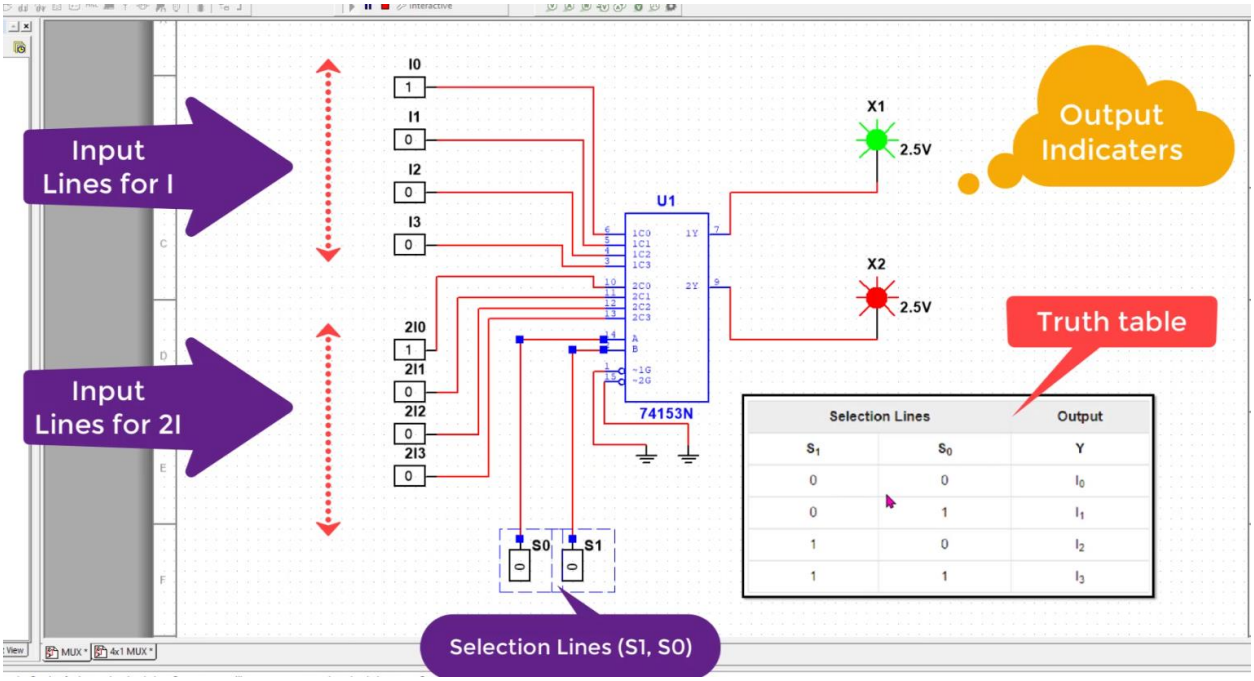
$Y=S_1'S_0'I_0+S_1'S_0I_1+S_1S_0'I_2+S_1S_0I_3$

We can implement this Boolean function using Inverters, AND gates & OR gate. The **circuit diagram** of 4x1 multiplexer is shown in the following figure.

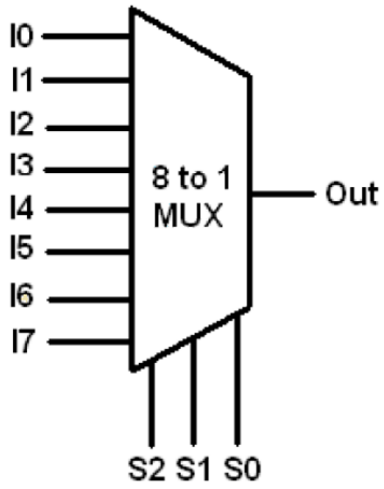




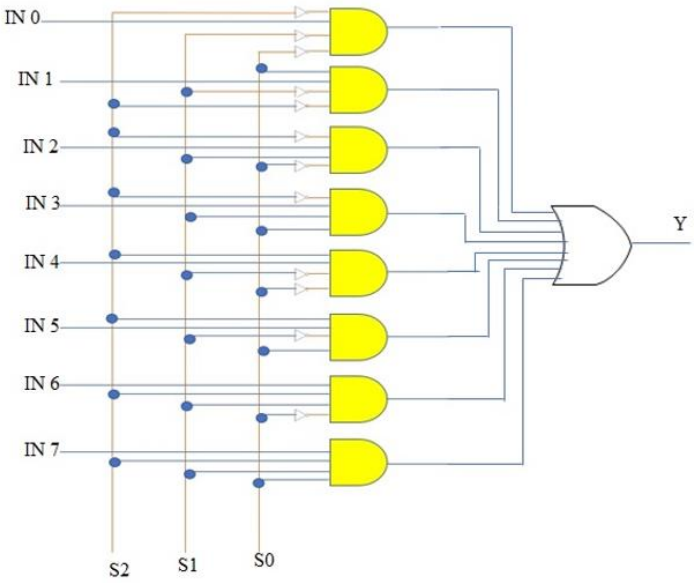
5. 4x1 Mux(74LS153 Testing in Multisim)



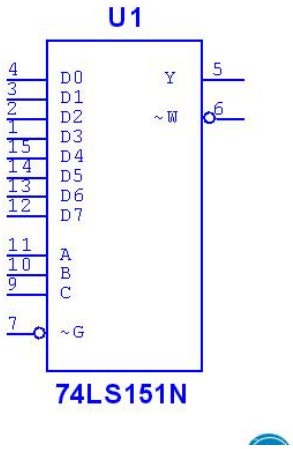
6. 8x1 Mux



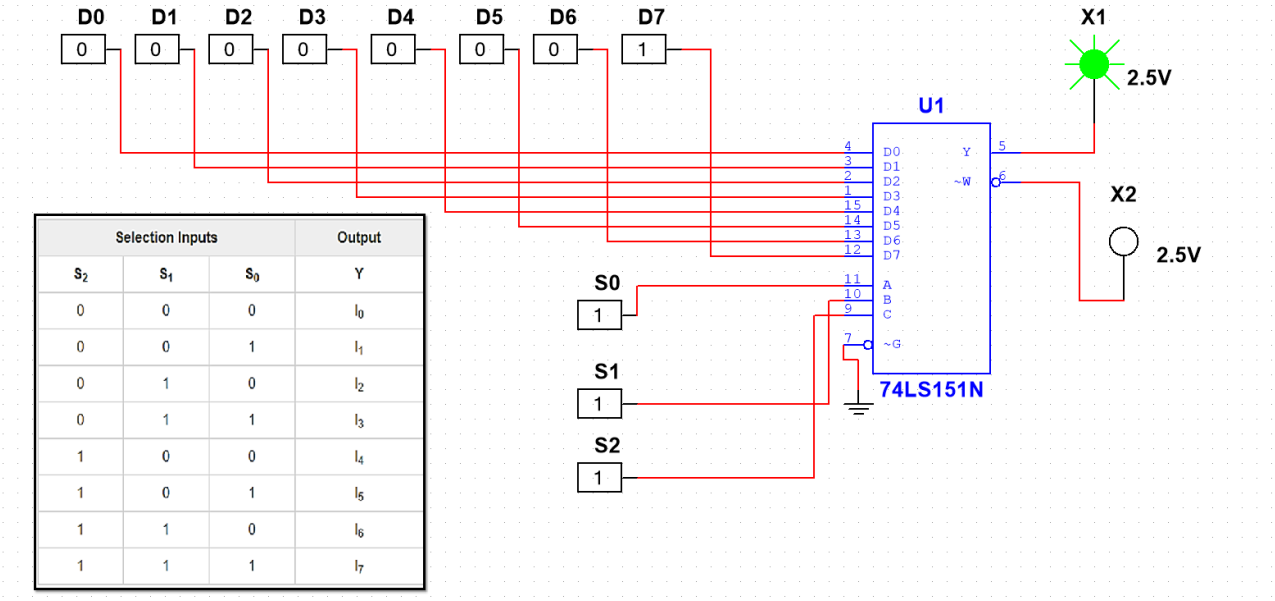
Selection Inputs			Output
S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7



$$Y = S2'\,S2'\,S0'\,I0 + S2'\,S1'\,S0\,I1 + S2'\,S1\,S0'\,I2 + S2'\,S1\,S0\,I3 + S2\,S1'\,S0'\,I4 + S2\,S1'\,S0\,I5 + S2\,S1\,S0'\,I6 + S2\,S1\,S0\,I7$$



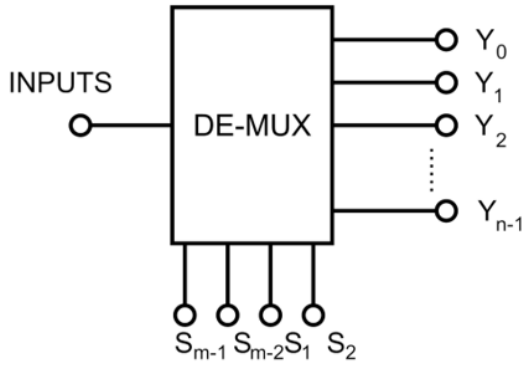
7. 8x1 Mux(74LS151 Testing in Multisim)



Selection Inputs			Output
S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

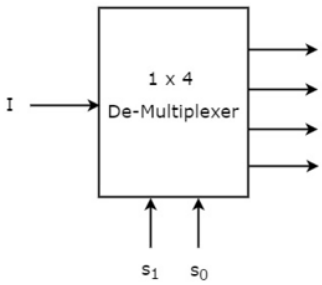
8. DE Multiplexer

The function of De multiplexer is in contrast to multiplexer function. It takes information from one line and distributes it to a given number of output lines. For this reason, the demultiplexer is also known as a data distributor. It has single input, 'n' selection lines and maximum of 2^n outputs. The input will be connected to one of these outputs based on the values of selection lines.



9. 1x4 De Multiplexer

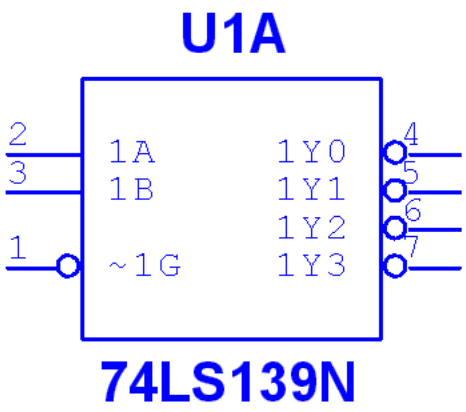
1x4 De-Multiplexer has one input I, two selection lines, s_1 & s_0 and four outputs Y_3, Y_2, Y_1 &Y_0. The **block diagram** of 1x4 De-Multiplexer is shown in the following figure.

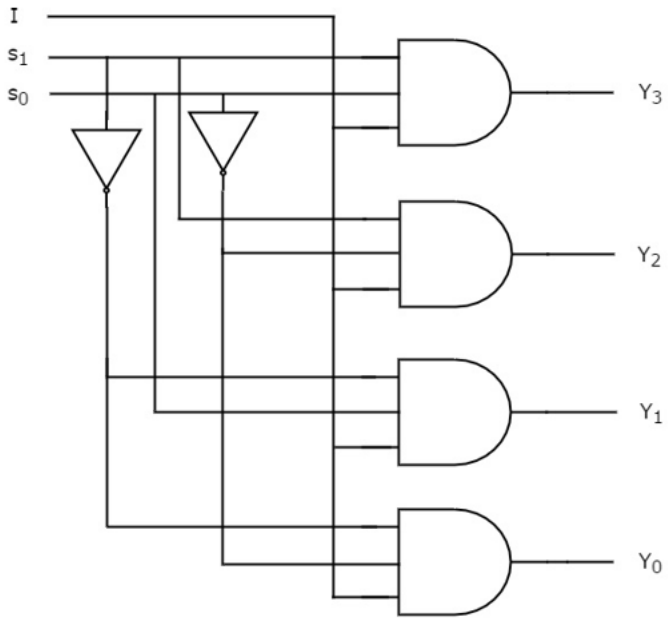


Selection Inputs		Outputs			
S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	I
0	1	0	0	I	0
1	0	0	I	0	0
1	1	I	0	0	0

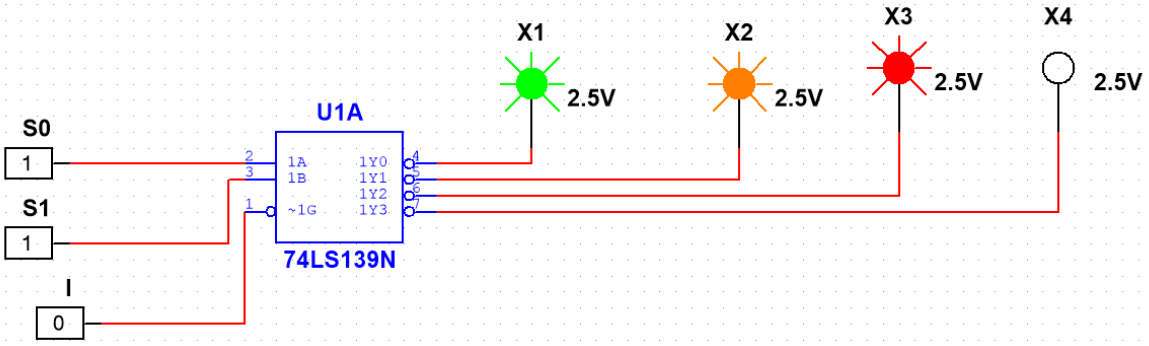
From the Truth table, we can directly write the **Boolean functions** for each output as

$Y_3=s_1s_0I$
$Y_2=s_1s_0'I$
$Y_1=s_1's_0I$
$Y_0=s_1's_0'I$





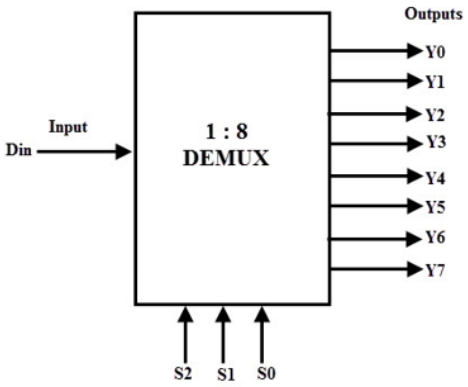
10. 1x4 De-Mux(74LS139 Testing in Multisim)



Selection Inputs		Outputs			
S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	I
0	1	0	0	I	0
1	0	0	I	0	0
1	1	I	0	0	0

11. 1x8 De Multiplexer

1x8 De-Multiplexer has one input I, three selection lines, s_2, s_1 & s_0 and seven outputs $Y_7, Y_6, Y_5, Y_4, Y_3, Y_2, Y_1$ & Y_0. The **block diagram** of 1x8 De-Multiplexer is shown in the following figure.



Selection Inputs			Outputs							
s_2	s_1	s_0	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0	I
0	0	1	0	0	0	0	0	0	I	0
0	1	0	0	0	0	0	0	I	0	0
0	1	1	0	0	0	0	I	0	0	0
1	0	0	0	0	0	I	0	0	0	0
1	0	1	0	0	I	0	0	0	0	0
1	1	0	0	I	0	0	0	0	0	0
1	1	1	I	0	0	0	0	0	0	0