



DLD Lab-14 Registers



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1. Objectives:

- Getting familiar with the design of sequential circuits on the register transfer level
- Gaining experience in using functions of shift registers for performing register transfer operations
- Gaining a close insight into the functioning and properties of the universal shift register,
- Developing skills in the composition and testing of sequential logic circuits

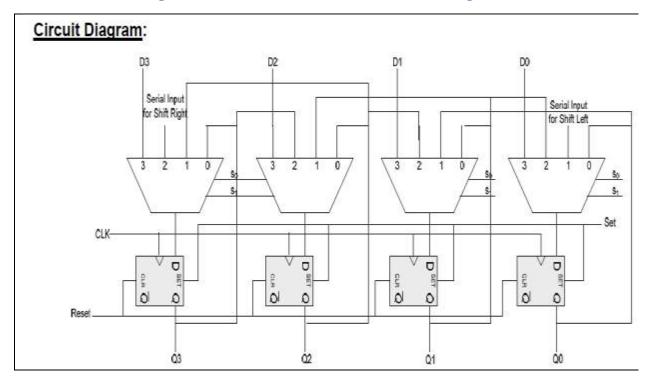
2. Equipment Required:

- ETS-5000 Trainer Board / Multisim 14.2 /Logic.ly
- 74194 4-bit Universal Shift Register
- Jumper wires

3. Background Theory

A register is used to store n-bits of information, where n is number of flipflops. A register is consists of a set of flip-flops, together with gates that perform data processing tasks. The flip-flops hold data, and the gates determine the new or transformed data to be transferred into the flip-flops. The registers have two types, one simple register and other register with parallel load. The register with parallel load is the register in which we can easily store the value of our own choice. This ability of register is controlled by a control input, if control input is 1 then the data which we want to enter is store on the register, and when the value is 0 then the data which store in the register remain store in the register. Another type of register is known as shift register. The shift register is capable of shifting its stored bits laterally in one or both direction. The logical configuration of a shift register consists of a chain of flip-flops in cascade, with the output of one flip-flop connected to the input of the next flip-flop. All flip-flops receive a common clock pulse, which activates the shift from each stage to the next.

4. Circuit Diagram of Four Bit Universal Shift Register:



5. Universal Shift Register IC:

Pin Configuration of 74194

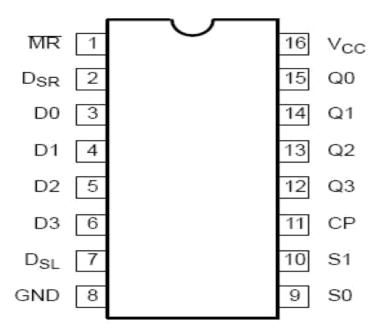


Figure 12.2 Pin Configurations 74194

6. Characteristics Table for Universal Shift Register IC Operation:

S1	S0	Operation
0	0	No change
0	1	Shift Right
1	0	Shift Left
1	1	Parallel Load

7. Parallel Load Operation:

S1	S0	D0D1D2D3	Q0Q1Q2Q3

8. Shift Left Operation:

S1	S0	D_sl	Q0 Q1 Q2 Q3

9. Shift Right Operation:

S1	S0	D_sr	Q0 Q1 Q2 Q3

10. No change Operation:

S1	S0	Q0Q1Q2Q3

11. Procedure

- 12. Connect the trainer with the power supply
- 13. For clock, connect function generator with the power supply. Keep frequency knob on minimum, press the button for function of square wave and keep the frequency range on minimum, rotate the amplitude knob to max and get the output from it. Connect the red elegator clip with the CP pin of the IC and ground the black elegator clip.
- 14. Mount the IC 74LS194 on the trainer board
- 15. Supply the VCC and GND to the pin 16 and 8 respectively
- 16. Wire the pins of IC, refer to the pin configuration.
- 17. Drive the D's, Dsr, Dsl, S0 & S1 inputs with input switches on the trainer board and CP input from the clock on the trainer board. Connect output Q's to LEDs.
- 18. Connect the Mater Reset (MR) to input switch. When low will reset the register
- 19. Apply different combinations on S1, S0 and verify the corresponding function. Observe and record the output on the LEDs.