



---

# **DLD Lab-02**

## **Logic Gates**

---



**Instructor: Mazhar Iqbal**

**EL227 – Digital Logic Design-Lab**

**SEMESTER SPRING 2023**

FEBRUARY 9, 2022

NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES, FAST- PESHAWAR CAMPUS  
Department Of Computer Science

## Contents

1. Lab Title: .....	2
2. Objectives: .....	2
3. Equipment Required: .....	2
4. Background Theory .....	2
5. GATES, THEIR IC PIN CONFIGURATION & TRUTH TABLES:.....	2
6. Test the functionality of 2-Input AND Gate.....	7
7. Test the functionality of 2-Input OR Gate.....	7
8. Test the functionality of 2-Input NAND Gate.....	7
9. Test the functionality of 2-Input NOR Gate.....	7
10. Test the functionality of 2-Input NOR Gate using OR and NOT gates.....	7
11. Test the functionality of 2-Input NAND Gate using AND and NOT gates.....	7
12. Test the functionality of 2-Input OR Gate using NOR and NOT gates.....	7
13. Test the functionality of 2-Input AND Gate using NAND and NOT gates.....	7
14. Test the functionality of 3-Input NAND Gate. ....	7
15. Test the functionality of 3-Input NAND Gate using 2-Input NAND gates. ....	7

## 1. Lab Title:

Logic Gates (AND, OR, NOT, NAND, NOR, XOR, XNOR)

## 2. Objectives:

- To become familiar with the operation of Basic Gates (AND, OR, NOT, NAND, NOR, XOR, XNOR) using ICs.
- To become familiar how to determine the truth tables for logic gates

## 3. Equipment Required:

- ETS-5000 Digital Training System/ Multisim 14.2 /Logic.ly
- 7400 quad 2-input NAND gate IC
- 7402 quad 2-input NOR gate IC
- 7404 hex NOT (Inverter) gate IC
- 7408 quad 2-input AND gate IC
- 7432 quad 2-input OR gate IC
- 7486 quad 2-input XOR gate IC
- 4077 quad 2-input XNOR gate IC

## 4. Background Theory

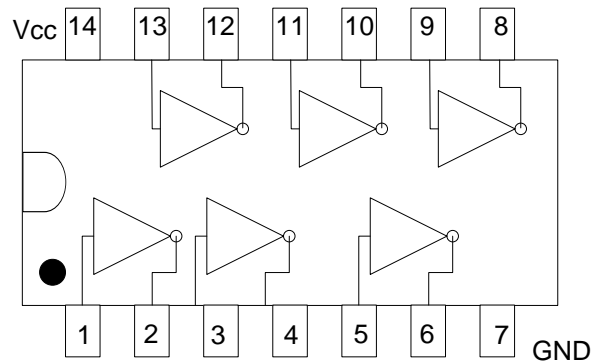
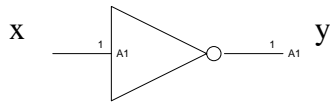
Logic deals with only two normal conditions: logic TRUE or logic FALSE. In Boolean logic, TRUE is often represented by the term HIGH or the number 1 and FALSE is represented by the term LOW or the number 0. HIGH and LOW (1 or 0) are logic terms; they do not indicate whether the voltage is higher or lower. In positive logic the more positive voltage is TRUE and the less positive voltage is FALSE i.e  $+2.5V = \text{HIGH}$  and  $+0.5V = \text{LOW}$ . With the negative logic this definition is reversed.

The basic logic gates and their symbols are summarized in the following pages. The truth table with all possible input combination is given and the output is left empty to you as an exercise. All possible combination of inputs involve counting in binary from 0 to  $2^n - 1$  where n is the number of inputs.

In this experiment you will look at the truth tables for several arrangements of simple gates.

## 5. GATES, THEIR IC PIN CONFIGURATION & TRUTH TABLES:

### NOT Gate

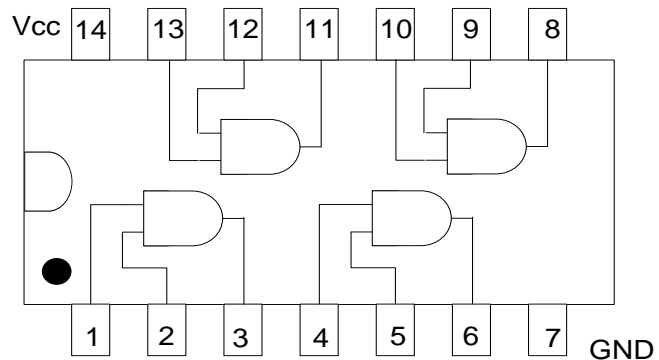
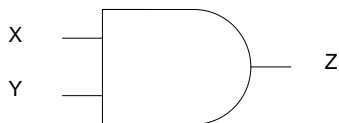


NOT Gate (Hex Inverter) 7404

### Truth Table

Input (x)	Output (y)
0	
1	

### 2-Input AND Gate

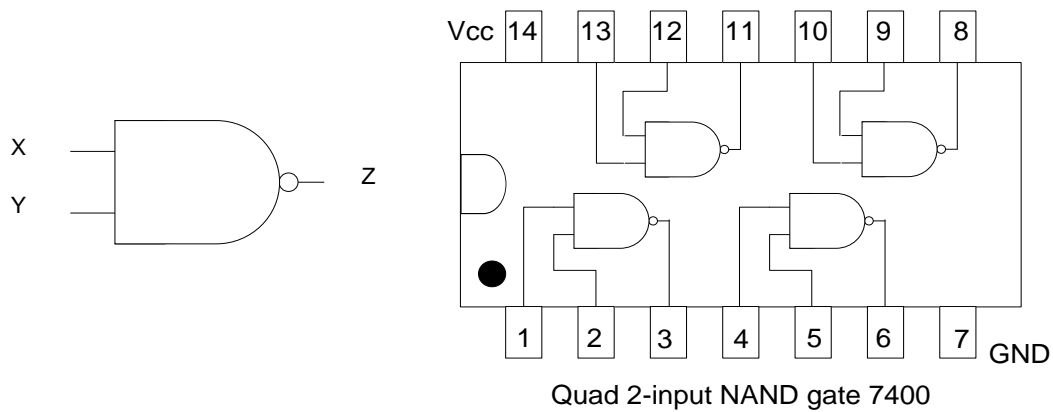


Quad 2-input AND gate 7408

### Truth Table

Input		Output
X	Y	Z
0	0	
0	1	
1	0	
1	1	

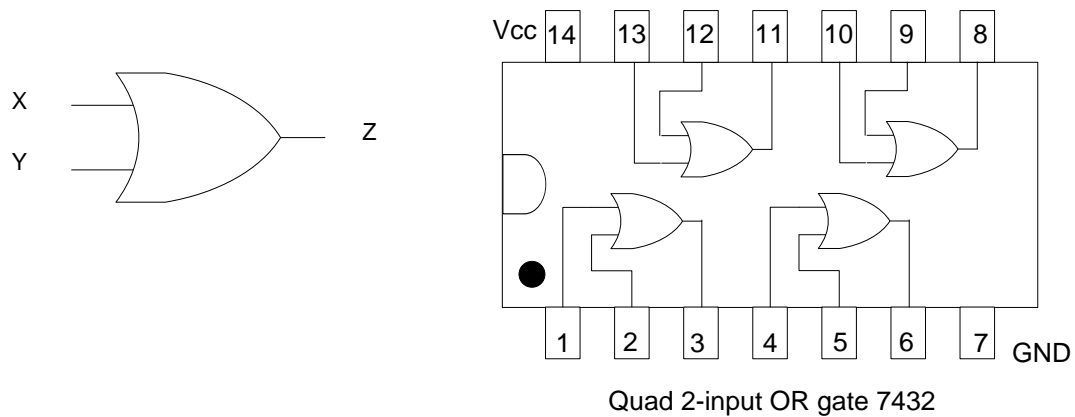
### 2-Input NAND Gate



**Truth Table**

Input		Output
X	Y	Z
0	0	
0	1	
1	0	
1	1	

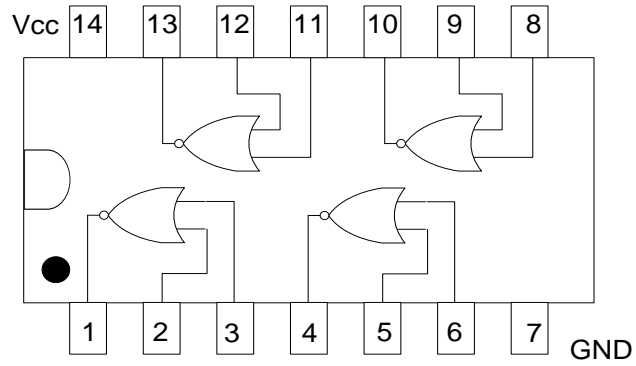
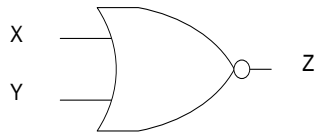
**2-Input OR Gate**



**Truth Table**

Input		Output
X	Y	Z
0	0	
0	1	
1	0	
1	1	

**2-Input NOR Gate**

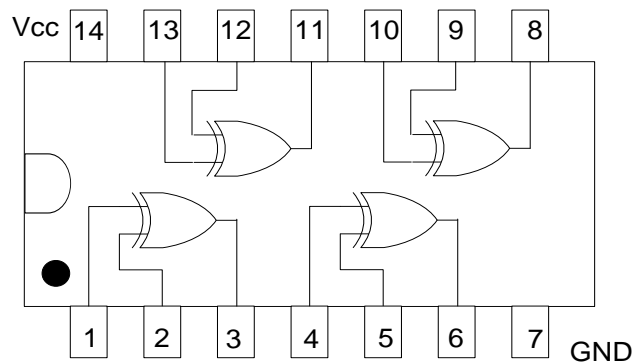
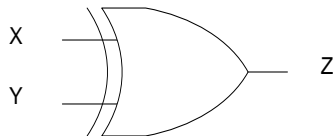


Quad 2-input NOR gate 7402

### Truth Table

Input		Output
X	Y	Z
0	0	
0	1	
1	0	
1	1	

### 2-Input X-OR Gate

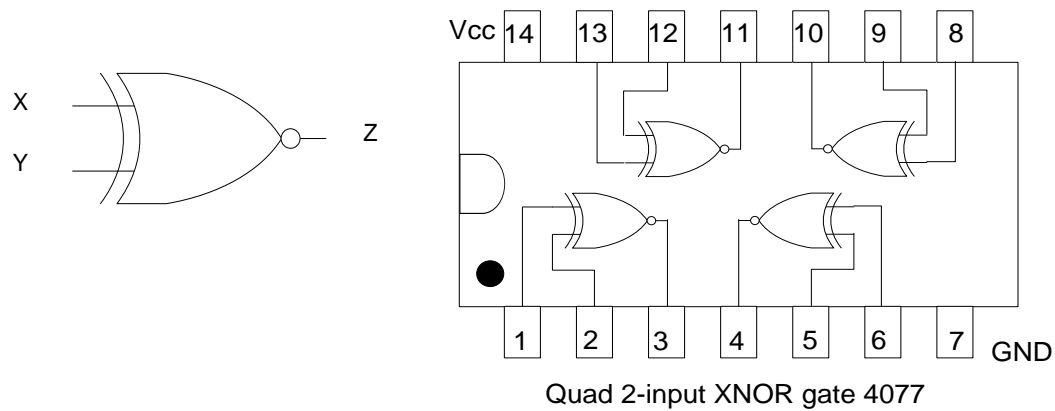


Quad 2-input X-OR gate 7486

### Truth Table

Input		Output
X	Y	Z
0	0	
0	1	
1	0	
1	1	

### 2-Input X-NOR Gate



### ***Truth Table***

Input		Output
X	Y	Z
0	0	
0	1	
1	0	
1	1	

### ***Procedure***

1. Connect the trainer board with the power supply
2. Mount the first IC 7408 (AND gate) on the board.
3. Connect pin 14 to +5 V and pin 7 to GND.
4. Wire the circuit according to the diagram by consulting the corresponding gate ICs data sheet.
5. Apply all the combinations of inputs and observe the output on the LED to verify the truth tables of the gates.

6. Test the functionality of 2-Input AND Gate.
7. Test the functionality of 2-Input OR Gate.
8. Test the functionality of 2-Input NAND Gate.
9. Test the functionality of 2-Input NOR Gate.
10. Test the functionality of 2-Input NOR Gate using OR and NOT gates.
11. Test the functionality of 2-Input NAND Gate using AND and NOT gates.
12. Test the functionality of 2-Input OR Gate using NOR and NOT gates.
13. Test the functionality of 2-Input AND Gate using NAND and NOT gates.
14. Test the functionality of 3-Input NAND Gate.
15. Test the functionality of 3-Input NAND Gate using 2-Input NAND gates.