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# **DLD Lab-11**

## **Latches**

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**EL227 – Digital Logic Design-Lab**

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## 1. Objectives:

- Getting familiar with characteristic tables and characteristic functions of latches and flip-flops
- Gaining a close insight into the functioning and properties of basic static memory circuits
- Developing skills in the composition and testing of sequential logic circuits.

## 2. Equipment Required:

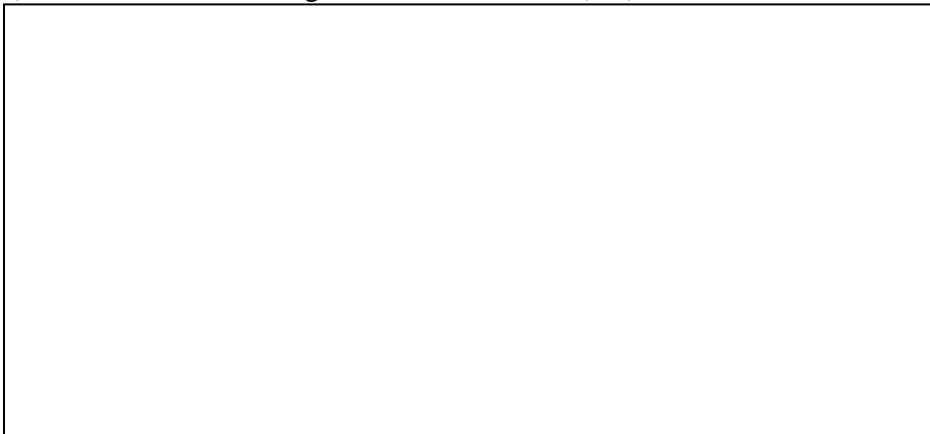
- DEV-2765E Trainer Board/ Multisim 14.2 /Logic.ly
- 7400 NAND Gate IC
- 7402 NOR Gate IC
- 7474 Dual +ve edge triggered D-Flip Flop

## 3. Background Theory

The elements used to store binary information in sequential circuits are called latches and flip-flops. A storage element can maintain a binary state as long as power is delivered to the circuit until directed by an input signal to switch states. The major differences among the various types of latches and flip-flops are the number of inputs they possess and the manner inputs affect the binary state. The most basic storage elements are latches, which uses feedback to lock onto and hold data, from which flip-flops are usually constructed. Although latches are most often used within flip-flops, they can also be used with more complex clocking methods to implement sequential circuits directly.

### • LATCHES

a) Draw the circuit diagram of a *NOR* latch (SR) below:



- b) Construct the circuit on the breadboard and fill the following truth table according to the outputs your circuit gives.

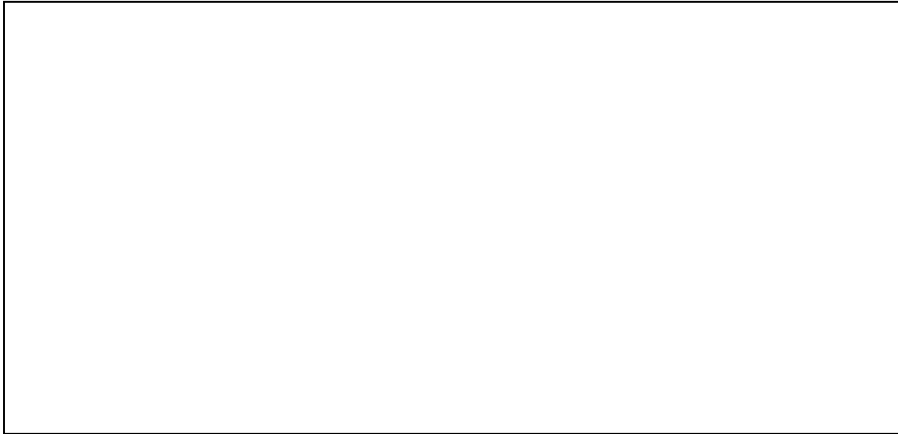
<b>S</b>	<b>R</b>	<b>Next State of Q</b>
0	1	
1	1	
1	0	
0	0	

- c) Draw the circuit diagram of a *NAND* latch (SR) below:

- d) Construct the circuit on the breadboard and fill the following truth table according to the outputs your circuit gives.

<b>S</b>	<b>R</b>	<b>Next State of Q</b>
0	1	
1	1	
1	0	
0	0	

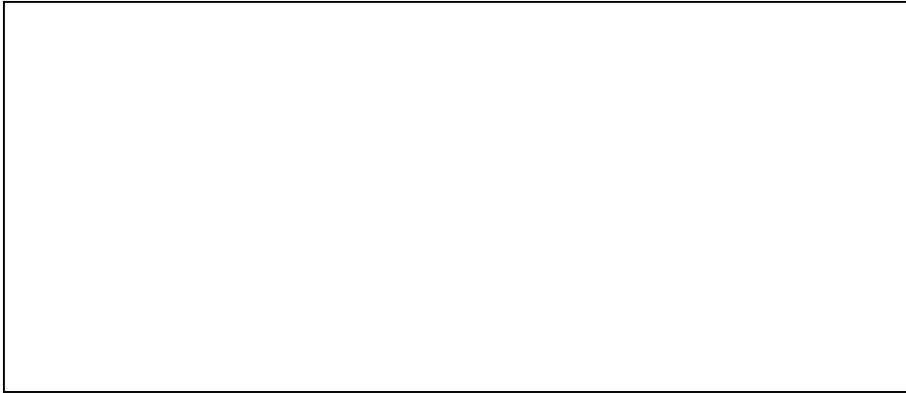
- e) Draw the circuit diagram of a *SR* latch with a control input below. (Modify the circuit you implemented in part 'a')



- f) Construct the circuit on the breadboard and fill the following truth table according to the outputs your circuit gives.

C	S	R	Next State of Q
0	x	x	
1	0	1	
1	0	0	
1	1	0	
1	1	1	

- g) Draw the circuit diagram of a *D* latch. (Modify the circuit you implemented in part 'c')



- h) Construct the circuit on the breadboard and fill the following truth table according to the outputs your circuit gives.

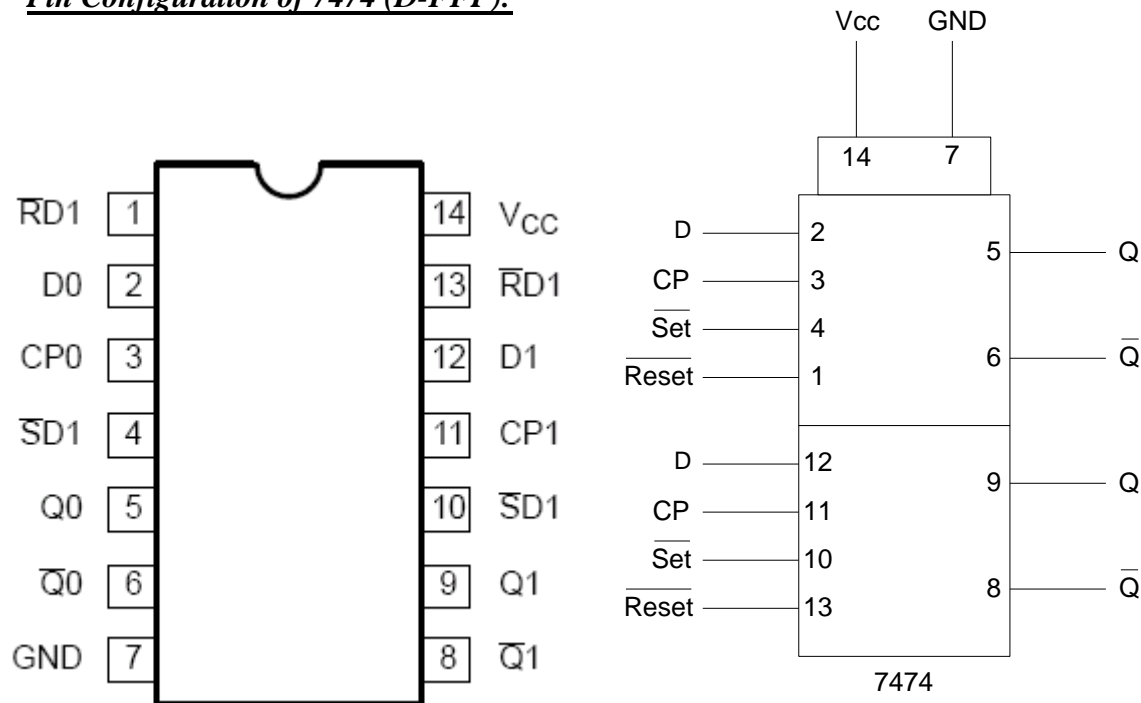
C	D	Next State of Q
0	x	
1	0	
1	1	

### **Flip Flops**

A flip-flop is usually constructed by combining two same or different types of latches. Flip-flop circuits are constructed in such a way as to make them operate properly when they are a part of a sequential circuit that employs a single clock. Note that the problem with the latch is that as soon as an input changes, shortly thereafter the corresponding output changes to match it. This is what allows a change on a latch output to produce additional changes at other latch outputs while the clock pulse is at logic 1. The key to the proper operation of flip-flops is to prevent them from being transparent. In a flip-flop, before an output can change, the path from its inputs to its outputs is broken. So a flip-flop cannot “see” the change of its output or of the outputs of other, like flip-flops at its input during the same clock pulse. Thus, the new state of a flip-flop depends only on the immediately preceding state, and the flip-flops do not go through multiple changes of state. The edge triggered D flip flop avoids the problem of the RS invalid output states by not allowing the invalid states. The JK flip flop is a clocked RS flip flop with additional logic to replace the RS invalid output states with a new mode called toggle. Toggle causes the flip flop to change to the state opposite to its present state.

## 4. D-Flip Flop

### Pin Configuration of 7474 (D-FFP):



### Description of PINS

The 7474 is a dual positive edge-triggered D-type flip-flop featuring individual data, clock, set, and reset inputs; also true and complementary outputs. Set (SD) and reset (RD) are asynchronous active low inputs and operate independently of the clock input. When set and reset are inactive (high), data at the D input is transferred to the Q and Q outputs on the low-to-high transition of the clock

### **Function Table:**

INPUTS				OUTPUTS		OPERATING MODE
SD	RD	CP	D	Q	$\sim Q$	

0	1	X	X	1	0	Asynchronous set
1	0	X	X	0	1	Asynchronous reset
0	0	X	X	1	1	Undetermined*
1	1	↑	1	1	0	Load “1”
1	1	↑	0	0	1	Load “0”
1	1	1	X	NC	NC	Hold

### **Procedure**

1. Connect the trainer with the power supply
2. Mount the IC 74LS74 on the trainer board
3. Supply the VCC and GND to the pin 16 and 8 respectively
4. Connect only one of the two flip-flops available on the IC. The pin configuration and characteristic table (function table) for this IC is given above.
5. Drive the D input with input switch on the trainer board and CP input from the clock on the trainer board. Connect output Q<sub>0</sub> & ~ Q<sub>0</sub> with LED.
6. Be sure to connect the set (SD) and reset (RD) inputs to a logical 1.
7. Using the different input combinations and verify the D flip-flop characteristic table.
8. Observe and record the output on the LED.