DLD Lab-08

Encoder & Decoder

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EL227 – Digital Logic Design-Lab

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Contents

1. Objectives:

- Practicing the implementation of logic functions using MSI level functional blocks
- Gaining experience with MSI level functional blocks/components whose outputs are active low
- Gaining a close insight into the functioning and properties of decoder circuits
- Developing skills in the design and testing of combinational logic circuits.

2. Equipment Required:

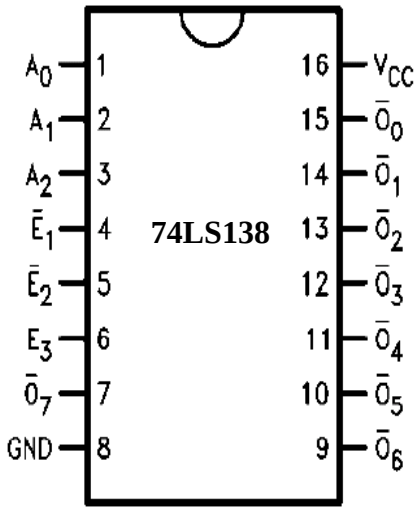
- DEV-2765E Trainer Board/ Multisim 14.2 /Logic.ly
- 74LS138 (3-to-8 Decoder)
- 74LS148 (8-bit Priority Binary Encoder)

3. Background Theory

Decoder is used to convert code in to set of signals. Decoder is a multiple input, multiple output logic circuit that converts coded input into decoded output, where the input and output codes are different. The input code generally has fewer bits than the output, and there is one-to-one mapping, each input code word produces a different output signal. The most commonly used input code is an n-bit binary code, where an n-bit word represents one of 2^n different coded values, i.e n-to-2^n decoder or binary decoder.

Encoder is a logic circuit that has fewer output bits than the input code. The encoder takes 2^n inputs bits and generates n-bit output. Only one of the inputs can be 1, and the corresponding binary will display on the output bits. But when more than one input bits become 1 at the same time then what should be the output then? So we give priority to inputs and the input with high priority will freeze the output with its binary value. Such an encoder is called *priority encoder*.

Pin Configuration of 74LS138 (3-to-8 Decoder)



Proper value at the enable lines (E1=0, E2=0, E3=1) will enable the decoder, all other combination of enable lines will keep the output lines high. These multiple enable lines are for building large decoders.

TRUTH TABLE:

Inputs						**Outputs**							
E_1	**E_2**	**E_3**	**A_0**	**A_1**	**A_2**	**O_0**	**O_1**	**O_2**	**O_3**	**O_4**	**O_5**	**O_6**	**O_7**
1	X	X	X	X	X								
X	1	X	X	X	X								
X	X	0	X	X	X								
0	0	1	0	0	0								
0	0	1	1	0	0								
0	0	1	0	1	0								
0	0	1	1	1	0								
0	0	1	0	0	1								
0	0	1	1	0	1								
0	0	1	0	1	1								
0	0	1	1	1	1								

1. Procedure

2. Connect the trainer with the power supply
3. Install the IC 74LS138 on the trainer board
4. IC 74138 is a 3 to 8 decoder. Wire according to the diagram.
5. Use the logic switches for input and connect output O0 O1 ……O7 to the LEDs
6. Supply the VCC and GND to the pin 16 and 8 respectively
7. Test all the possible combination of input and fill out the table

8. Encoders

Encoders and Decoders are combinational logic circuits.
An encoder is a device which transforms the data into some bits known only to it and the decoder is a device which transforms those coded bits to generate the original data again.
Encoding and Decoding is done for the safe transmission of data.
To encode something is to convert an unambiguous piece of information into a form of code that is not so clearly understood.
To decode is to perform the reverse operation: converting a code back into an unambiguous form.
The Main Difference between a decoder and encoder is that a decoder has binary code as an input while an encoder has binary code as an output.

9. Decoder

A decoder is a logic circuit that accepts a set of inputs that represents a binary number and activates only the output that corresponds to the input number.
In other words, a decoder circuit looks at its inputs, determines which binary number is present there, and activates the one output that corresponds to the number, all other outputs remain inactive.
A decoder is a circuit that changes a code into a set of signals.
In its general form, a decoder has N input lines to handle N bits and from one to 2^N output lines to indicate the presence of one or more N-bit combinations.
An AND gate can be used as the basic decoding element because it produces a high output only when all inputs are high.

BLOCK DIAGRAM OF DECODER

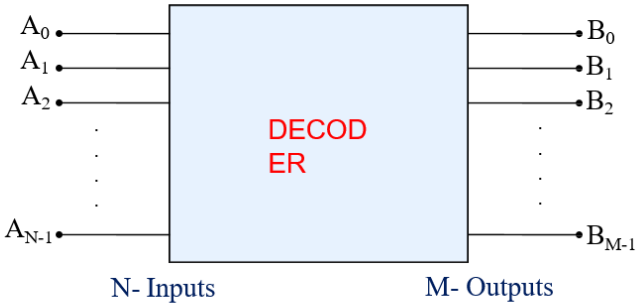


Fig. 1

Only one output is High for each input

10. 2 to 4 Line Decoder

- Block diagram of 2 to 4 decoder is shown in fig. 2
- A and B are the inputs. (No. of inputs =2)
- No. of possible input combinations: $2^2=4$
- No. of Outputs : $2^2=4$, they are indicated by D_0, D_1, D_2 and D_3
- From the Truth Table it is clear that each output is "1" for only specific combination of inputs.

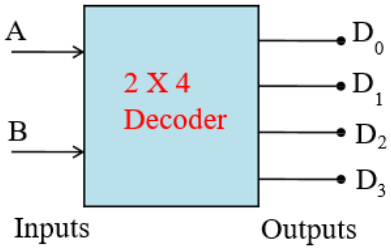


Fig. 2

TRUTH TABLE

INPUTS		OUTPUTS			
A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Truth Table

INPUTS		OUTPUTS			
A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

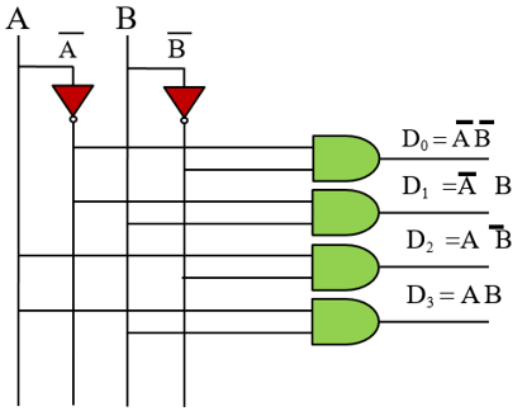
BOOLEAN EXPRESSION

From Truth Table

$$D_0 = \overline{A}\,\overline{B} \qquad D_1 = \overline{A}B$$

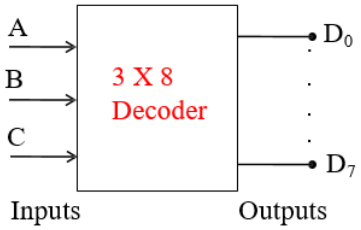
$$D_2 = A\,\overline{B} \qquad D_3 = AB$$

LOGIC DIAGRAM



11. 3 to 8 Line Decoder

- Block diagram of 3 to 8 decoder is shown in fig. 4
- A , B and C are the inputs. (No. of inputs =3)
- No. of possible input combinations: 23=8
- No. of Outputs : 23=8, they are indicated by D0 to D7
- From the Truth Table it is clear that each output is "1" for only specific combination of inputs.



12. 3 to 8 Line Decoder Truth Table

INPUTS			OUTPUTS								
A	B	C	D0	D1	D2	D3	D4	D5	D6	D7	
0	0	0	1	0	0	0	0	0	0	0	$D_0 = A\,B\,C$
0	0	1	0	1	0	0	0	0	0	0	$D_1 = A\,B\,C$
0	1	0	0	0	1	0	0	0	0	0	$D_2 = A\,B\,C$
0	1	1	0	0	0	1	0	0	0	0	$D_3 = A\,B\,C$
1	0	0	0	0	0	0	1	0	0	0	$D_4 = A\,B\,C$
1	0	1	0	0	0	0	0	1	0	0	$D_5 = A\,B\,C$
1	1	0	0	0	0	0	0	0	1	0	$D_6 = A\,B\,C$
1	1	1	0	0	0	0	0	0	0	1	$D_7 = A\,B\,C$

13. Circuit Diagram of 3 to 8 Line Decoder

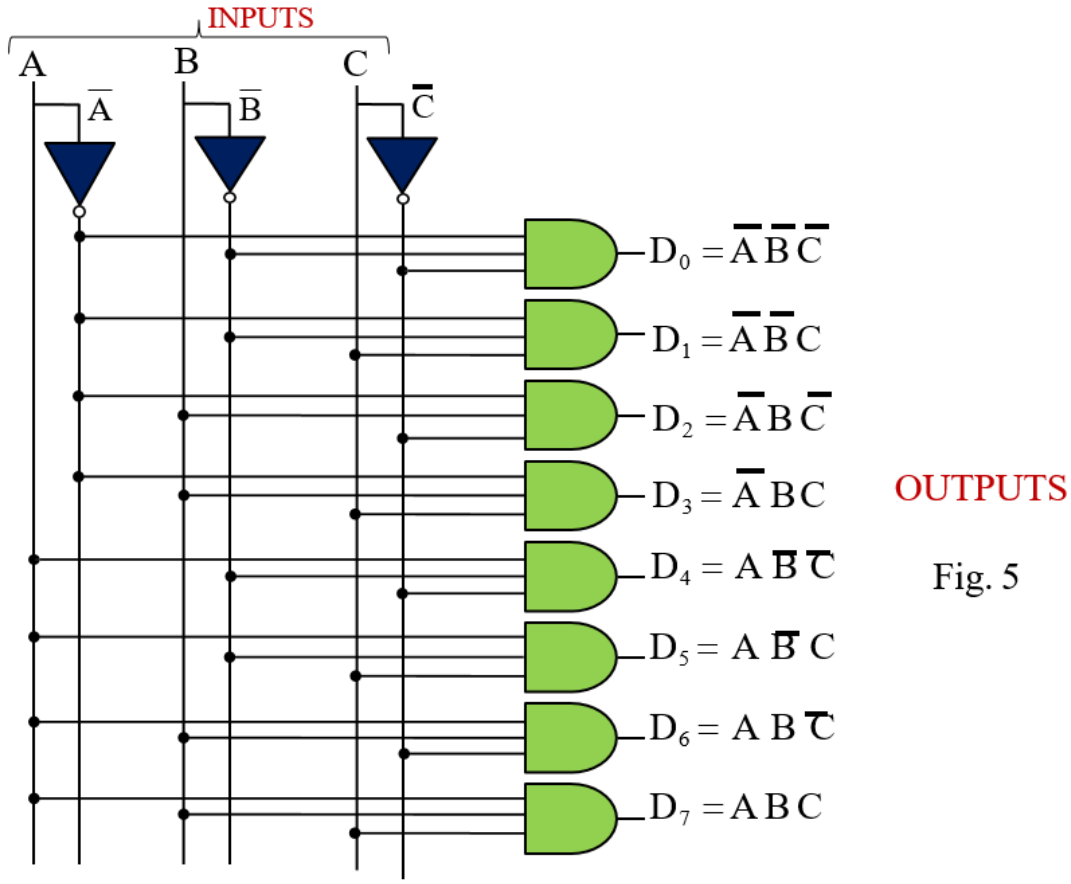
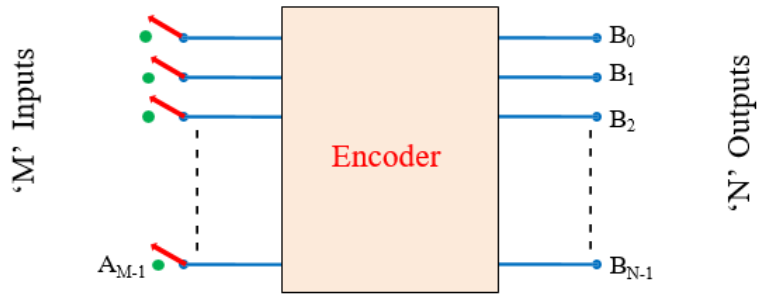


Fig. 5

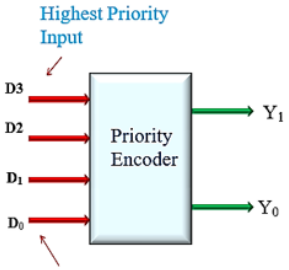
14. ENCODER

- An Encoder is a combinational logic circuit.
- It performs the inverse operation of Decoder.
- The opposite process of decoding is known as Encoding.
- An Encoder converts an active input signal into a coded output signal.
- Block diagram of Encoder is shown in Fig.10. It has 'M' inputs and 'N' outputs.
- An Encoder has 'M' input lines, only one of which is activated at a given time, and produces an N-bit output code, depending on which input is activated.



- Encoders are used to translate the rotary or linear motion into a digital signal.
- The difference between Decoder and Encoder is that Decoder has Binary Code as an input while Encoder has Binary Code as an output.
- Encoder is an Electronics device that converts the analog signal to digital signal such as BCD Code.
- Types of Encoders

i. Priority Encoder
ii. Decimal to BCD Encoder
iii. Octal to Binary Encoder
iv. Hexadecimal to Binary Encoder



Block Diagram of Priority Encoder

- As the name indicates, the priority is given to inputs line.
- If two or more input lines are high at the same time i.e 1 at the same time, then the input line with high priority shall be considered.

- From the truth table:
- We see that when all inputs are 0, our V bit or the valid bit is zero and outputs are not used.
- The x's in the table show the don't care condition, i.e, it may either be 0 or 1. Here, D3 has highest priority, therefore, whatever be the other inputs, when D3 is high, output has to be 11.
- And D0 has the lowest priority, therefore the output would be 00 only when D0 is high and the other input lines are low.
- Similarly, D2 has higher priority over D1 and D0 but lower than D3 therefore the output would be 010 only when D2 is high and D3 are low (D0 & D1 are don't care).

INPUTS				OUTPUTS		V
D_3	D_2	D_1	D_0	Y_1	Y_0	
0	0	0	0	x	x	0
0	0	0	1	0	0	1
0	0	1	x	0	1	1
0	1	x	x	1	0	1
1	x	x	x	1	1	1

Input				Output	
D_3	D_2	D_1	D_0	Y_1	Y_0
0	0	0	0	x	x
0	0	0	1	0	0
0	0	1	x	0	1
0	1	x	x	1	0
1	x	x	x	1	1

- There are four inputs D_0, D_1,D_2, D_3 and two outputs Y_1 and Y_2.
- D_3 has highest priority and D_0 is at lowest priority.
- If D_3=1 irrespective of other inputs then output Y_1Y_0=11.
- D_3 is at highest priority so other inputs are considered as don't care.

K-map for Y_1 and Y_0

D_3D_2 \ D_1D_0	00	01	11	10
00	X	0	0	0
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$Y_1 = D_2 + D_3$

D_3D_2 \ D_1D_0	00	01	11	10
00	X	0	1	1
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

$Y_0 = D_3 + \overline{D_2}\, D_1$

$Y_1 = D_2 + D_3$

$Y_0 = D_3 + \overline{D_2} D_1$

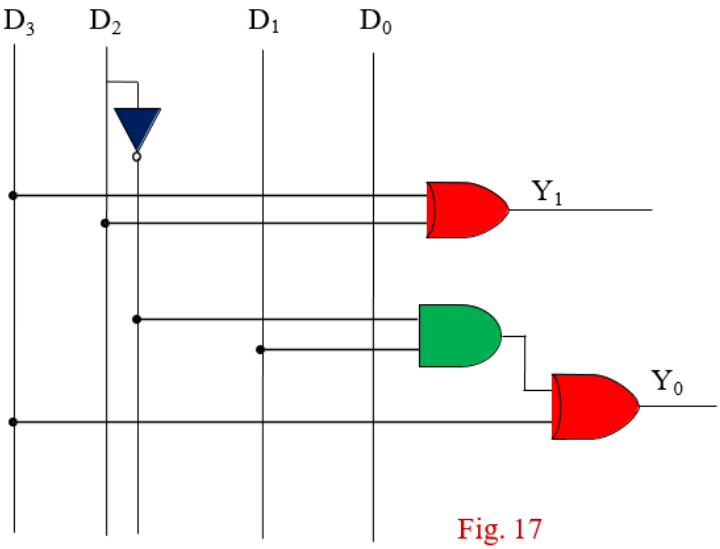


Fig. 17

15. DECIMAL TO BCD ENCODER:

- It has ten inputs corresponding to ten decimal digits (from 0 to 9) and four outputs (A,B,C,D) representing the BCD.
- The block diagram is shown in fig.18 and Truth table in fig.19

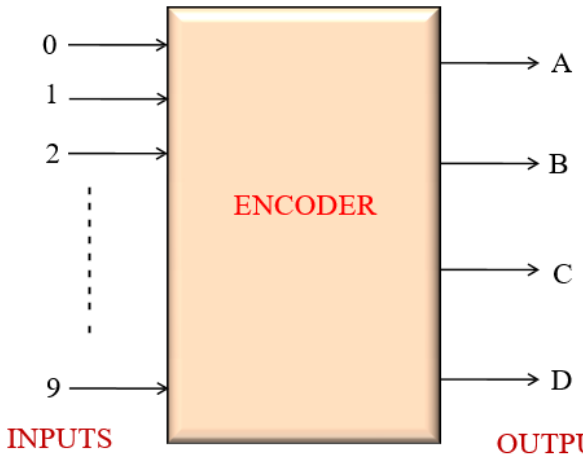


Fig. 18

INPUTS										BCD OUTPUTS			
0	1	2	3	4	5	6	7	8	9	A	B	C	D
1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	0	0	0	1	0	0
0	0	0	0	0	1	0	0	0	0	0	1	0	1
0	0	0	0	0	0	1	0	0	0	0	1	1	0
0	0	0	0	0	0	0	1	0	0	0	1	1	1
0	0	0	0	0	0	0	0	1	0	1	0	0	0
0	0	0	0	0	0	0	0	0	1	1	0	0	1

- From Truth Table it is clear that the output Ais HIGH when input is 8 OR 9 is HIGH

  Therefore A=8+9
- The output B is HIGH when 4 OR 5 OR 6 OR 7 is HIGH

  Therefore B=4+5+6+7
- The output C is HIGH when 2 OR 3 OR 6 OR 7 is HIGH

  Therefore C=2+3+6+7
- Similarly D=1+3+5+7+9

  Logic Diagram is shown in fig.20

16. DECIMAL TO BCD ENCODER Circuit Diagram:

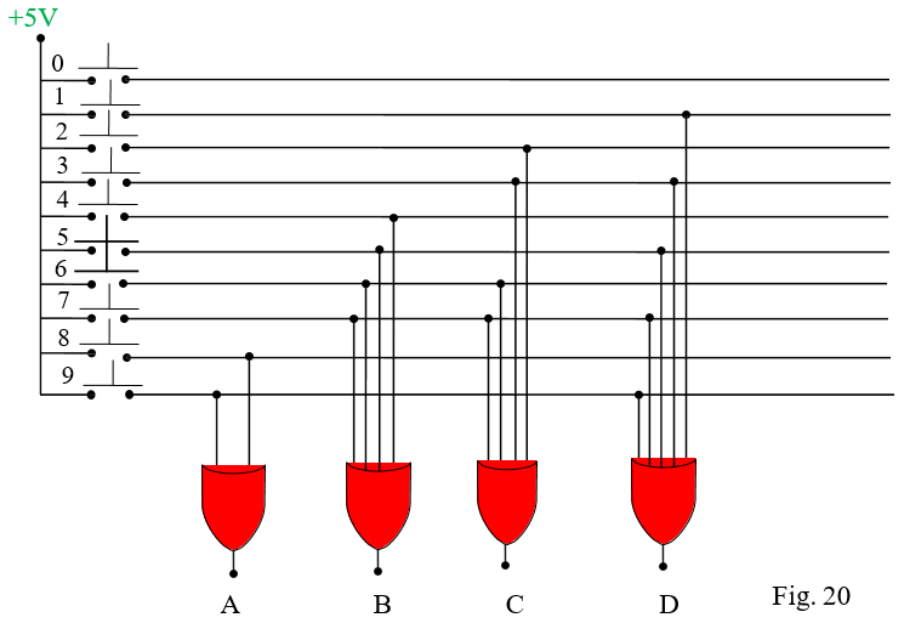
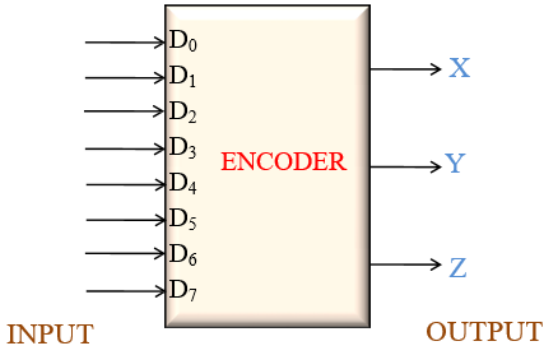


Fig. 20

17. OCTAL TO BINARY ENCODER

- Block Diagram of Octal to Binary Encoder is shown in Fig. 21
- It has eight inputs and three outputs.
- Only one input has one value at any given time.
- Each input corresponds to each octal digit and output corresponding Binary Code.



generates

INPUT								OUTPUT		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	X	Y	Z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

FROM TRUTH TABLE:

$$X = D_4 + D_5 + D_6 + D_7$$

$$Y = D_2 + D_3 + D_6 + D_7$$

$$Z = D_1 + D_3 + D_5 + D_7$$

- It is assume that only one input is HIGH at any given time. If two outputs are HIGH then undefined output will produced. For example D_3 and D_6 are HIGH, then output of Encoder will be 111.. This output neither equivalent code corresponding to D_3 nor to D_6
- To overcome this problem, priorities should be assigned to each input.
- Form the truth table it is clear that the output X becomes 1 if any of the digit D_4 or D_5 or D_6 or D_7 is 1.
- D_0 is considered as don't care because it is not shown in expression.
- If inputs are zero then output will be zero. Similarly if D_0 is one, the output will be zero.

18. Logic Diagram of Octal to Binary Encoder

$X = D_4 + D_5 + D_6 + D_7$ $Y = D_2 + D_3 + D_6 + D_7$ $Z = D_1 + D_3 + D_5 + D_7$

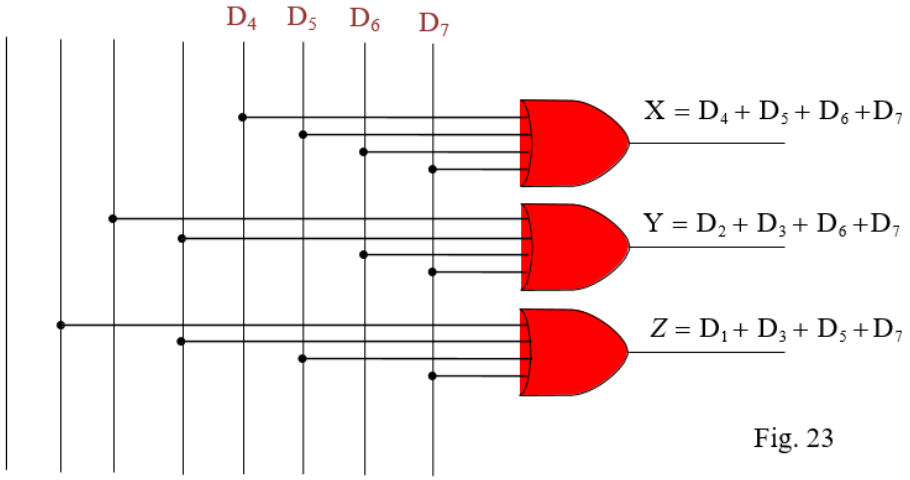


Fig. 23