ECE 550 Fall 2015
Homework 1
Due: 11:59PM September 11, 2015
Demo by: 11:59PM September 18, 2015

For this homework, you will be answering three pencil and paper questions, as well as writing VHDL. You should submit your answers to the pencil and paper questions, along with your VHDL code in a .tar, .tar.gz, or .zip format (no other formats will be accepted) to Sakai before the deadline. Your answers to the pencil and paper questions **must** be in .pdf format—no Word documents will be accepted. For drawings, you are encouraged to draw in computerized tool, but may draw by hand and scan the drawings into a pdf format, as long as they are clear and easily readable.

Within one week of the submission deadline, you must demo your VHDL code to a TA, who will ask each group member to explain various aspects of how it works. **All** group members are responsible for understanding the entire submissions.

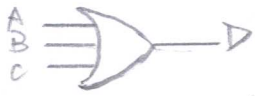
Group: Shengxin Qian
Xinquan Lin.

Shengxin_Qian

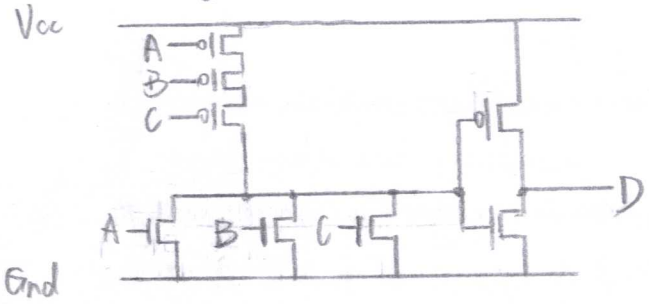
Question 1:
Draw the transistors required to form the following gates:

- A 3-input OR gate.

input: A, B, C, Output: D

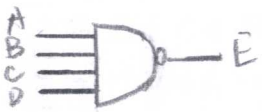


$D = A + B + C = \overline{\bar{A}\bar{B}\bar{C}}$



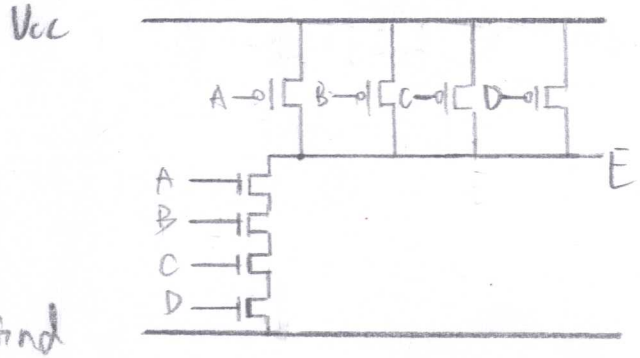
- A 4-input NAND gate.

NAND:



$E = \overline{ABCD}$

$= \bar{A} + \bar{B} + \bar{C} + \bar{D}$



Question 2:
Given the following truth-table:

A	B	C	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

1. Write the sum-of-products formula for the truth table
2. Simplify your formula as much as you can.
3. Draw the logic gates which correspond to your simplified formula.

1. $Out = \bar{A}B\cdot C + A\cdot\bar{B}\cdot C + A\cdot B\cdot C$

2. $Out = \bar{A}B\cdot C + A\cdot\bar{B}\cdot C + A\bar{B}\cdot C$

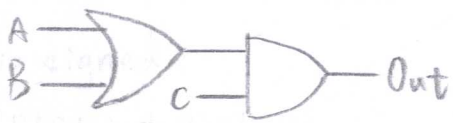
$= B\cdot C + A\cdot\bar{B}\cdot C$

$= C(B + A\bar{B})$

$= C[(1+A)B + A\bar{B}]$

$= C\cdot(A+B)$

3



Question 3:

1. Convert each of the following numbers to **8** bit signed 2's complement binary, then to hexadecimal (write both the binary and the hex):

	binary	hex
(a) 83	0101 0011	0x53
(b) -62	1100 0010	0xC2
(c) 0	0000 0000	0x00
(d) -116	1000 1100	0x8C
(e) 111	0110 1111	0x6F

2. Perform each of the following 8-bit additions (assume 2's complement representation). For each addition, give the result, and state whether or not the addition suffered from *overflow* (1) if the numbers are treated as signed numbers (2) if the numbers are treated as unsigned numbers. **Show your work!** (for this problem, show where you carried).

(a) 1010 0001 + 1101 1010 (-95)

(b) 01010111 + 01010111

(c) 0111 1101 + 01001001

(d) 0101 0101 + 1111 1110

(a) (1) signed:

1010,0001 + 1101,1010

= 0111,1011, overflow

(2) unsigned:

1010,0001 + 1101,1010

= 0111,1011, overflow

(b) (1) signed:

0101,0111 + 0101,0111

= 1010,1110, overflow

(2) unsigned

0101,0111 + 0101,0111

= 1010,1110, not overflow

(c) (1) signed

0111,1101 + 0100,1001

= 1100,0110, overflow

(2) unsigned

0111,1101 + 0100,1001

= 1100,0110, not overflow

(d) (1) signed

0101,0101 + 1111,1110

= 0101,0011, not overflow

2) unsigned

0101,0101 + 1111,1110

= 0101,0011, overflow