ECE 550 Fall 2015
Homework 1
Due: 11:59PM September 11, 2015
Demo by: 11:59PM September 18, 2015

For this homework, you will be answering three pencil and paper questions, as well as writing VHDL. You should submit your answers to the pencil and paper questions, along with your VHDL code in a .tar, .tar.gz, or .zip format (no other formats will be accepted) to Sakai before the deadline. Your answers to the pencil and paper questions **must** be in .pdf format—no Word documents will be accepted. For drawings, you are encouraged to draw in computerized tool, but may draw by hand and scan the drawings into a pdf format, as long as they are clear and easily readable.

Within one week of the submission deadline, you must demo your VHDL code to a TA, who will ask each group member to explain various aspects of how it works. **All** group members are responsible for understanding the entire submissions.

Question 1:
Draw the transistors required to form the following gates:

- A 3-input OR gate.

- A 4-input NAND gate.

Question 2:
Given the following truth-table:

A	B	C	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

1. Write the sum-of-products formula for the truth table
2. Simplify your formula as much as you can.
3. Draw the logic gates which correspond to your simplified formula.

Question 3:

1. Convert each of the following numbers to **8** bit signed 2's complement binary, then to hexadecimal (write both the binary and the hex):

   (a) 83

   (b) -62

   (c) 0

   (d) -116

   (e) 111

2. Perform each of the following 8-bit additions (assume 2's complement representation). For each addition, give the result, and state whether or not the addition suffered from *overflow* (1) if the numbers are treated as signed numbers (2) if the numbers are treated as unsigned numbers. **Show your work!** (for this problem, show where you carried).

   (a) 10100001 + 11011010

   (b) 01010111 + 01010111

   (c) 01111101 + 01001001

   (d) 01010101 + 11111110

Question 4:

For this question, you will be writing VHDL. The DE2 boards have a row of 18 switches, as well as a set of 8 7-segment LEDs. For this question, you will reads the 18 switches as a binary number, and displays it as a hexadecimal number on the 5 right-most (lowest numbered) LEDs.

You should note that the LED segments are "active low"—a value of 0 turns them on, and a value of 1 turns them off. The segments are numbered starting with 0 at the top, and increasing in a clockwise fashion around the outside segments. The horizontal middle segment is numbered 6.

You should use the following figure to show you how to lay out the segments for each hex digit: