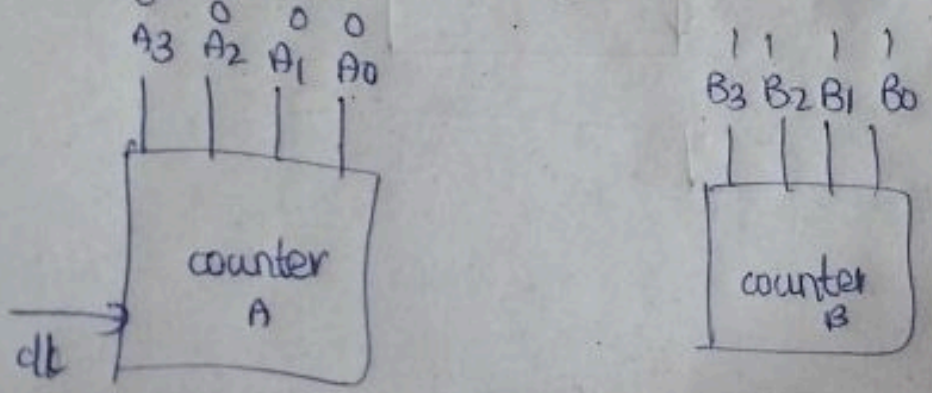
there are 2 counters, "counter A" being asynchronous up counter & "counter B" is an asynchronous down counter and at $T=0$, 0000 & 1111 are loaded respectively as shown. clock source (clk) available is 1MHz.

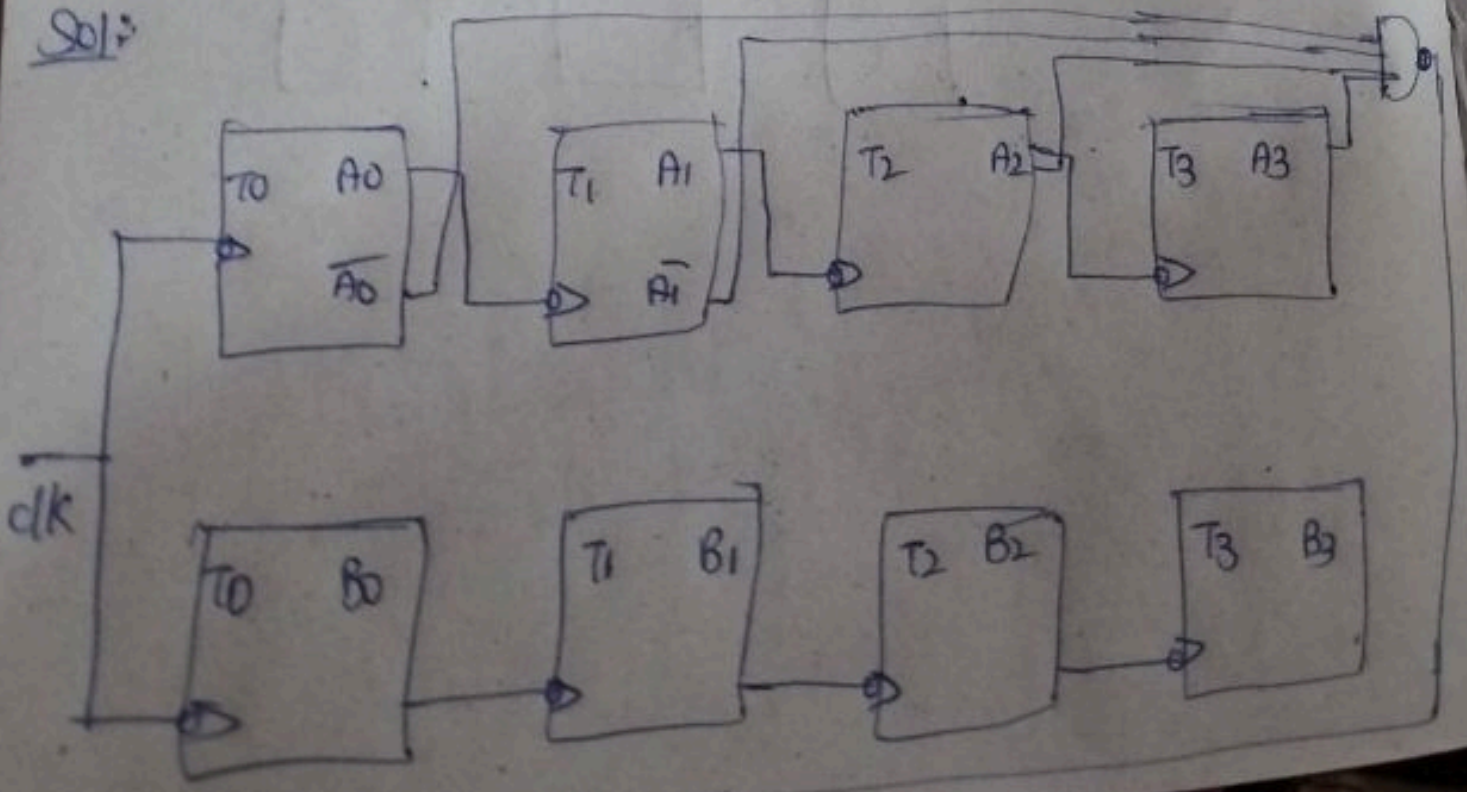
(1) complete the design such that counter B decrements by one value each time when decimal "12" appears at output of counter A (A_0 being LSB).

(2) what is the decimal value at o/ps of both counter A & counter B at $T=0.2$ milliseconds?

(3) what is the frequency of B_0 with respect to clk (1MHz)



Sol:



2A) Given freq = 1MHz

$T = 1\mu sec$

for $T = 0.2 msec = 0.2 \times 10^{-3}$

$$\text{pulses} = \frac{0.2 \times 10^{-3}}{1 \times 10^{-6}} = 200 \text{ pulses}$$

Decimal value for counter B

pulses = 200 − 12 = 188

and change occured at 16 pulses

16) 188 (11
16
28
16
12

decimal value = 3.

16) 200 (12
16
40
32
8

count-A

decimal = 7

8 clock pulses

counter B

pulses = 200 − 12 = 188

change occured at 16 pulses

(3) Frequency Bo is $\frac{f}{2} = \frac{1MHz}{2} = 0.5MHz$.