P4-NetFPGA Toolchain: Writing Stateful P4 Programs

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1 Abstract

The NetFPGA family of open source FPGA-based platforms is designed for the research community to do rapid hardware prototyping of high-performance networking applications at line rate. The latest NetFPGA platform, NetFPGA-SUME, has i/o capabilities allowing for 100Gbps operation.

The P4-NetFPGA toolchain has recently been developed to provide a seamless path for researchers, who may be unfamiliar with hardware description languages and FPGA details, to compile their P4 programs directly to the NetFPGA SUME platform. The intention is to make it very easy for anyone to try out their P4 programs at line rate.

In this demonstration, we will specifically showcase the toolchain and platform's ability to run stateful P4 data-plane programs. Demo attendees will be able to interact with the tables and registers on a data plane design in real time and see how performance is affected.

Within the networking community, there has been a lot of interest recently in defining apt abstractions for writing stateful data-plane programs. The Domino paper [1] from SIGCOMM 2016 proposed the idea of packet transactions and atoms. A packet transaction is a stateful packet processing code block that is executed atomically. An atom is the atomic packet processing unit supported by the target hardware. The authors showed that by using a small set of atoms they could implement a large range of different stateful programs in the data plane.

The P4-NetFPGA toolchain includes a library that supports a similar set of atoms to those defined in the Domino paper. This demonstration will show that by using these atoms, it is possible to write stateful P4 programs that run at line rate.

This opens up the possibility that researchers experimenting with higher level abstractions for writing stateful data-plane programs may now compile them to P4 and then on to the NetFPGA platform using the P4-NetFPGA toolchain as an intermediate step.

2 Presenters

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3 Other Notes

The P4-NetFPGA team will host a tutorial session at the P4 Developer Day. The proposed demo will be a working implementation of one of the tutorial assignments. We wish to use the demo and associated lightning talk as a means of advertising the new toolchain to the general workshop attendees. We plan to bring in physical machines as well as a NetFPGA-SUME board so that attendees can see the actual hardware running the P4 programs.

References

[1] Anirudh Sivaraman, Alvin Cheung, Mihai Budiu, Changhoon Kim, Mohammad Alizadeh, Hari Balakrishnan, George Varghese, Nick McKeown, and Steve Licking. Packet transactions: High-level programming for line-rate switches. In *Proceedings of the 2016 conference on ACM SIGCOMM 2016 Conference*, pages 15–28. ACM, 2016.