P4FPGA: Towards an Open Source P4 Backend for FPGA

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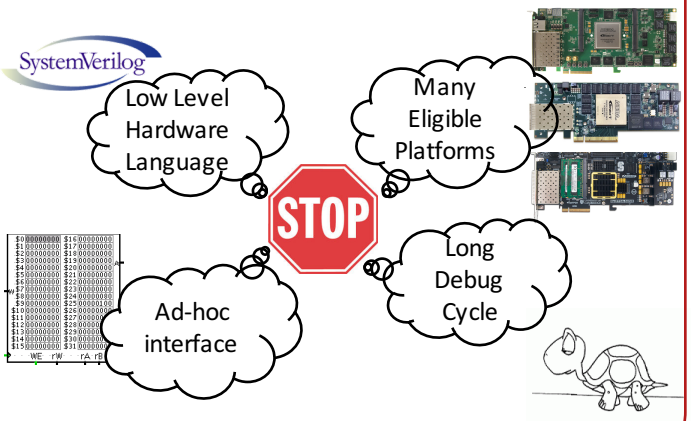
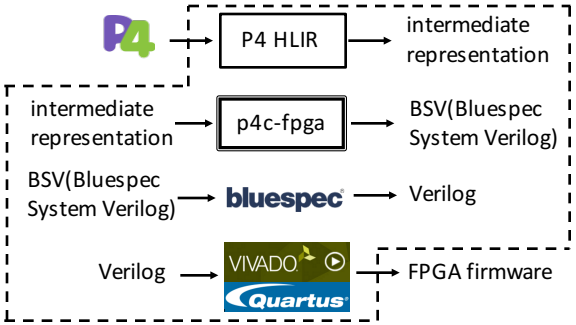
Motivation

Enable compilation of P4 to many FPGA platforms.



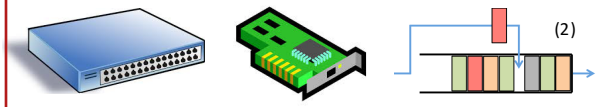
P4FPGA alleviates all of the above problems!

P4FPGA Pipeline



- P4FPGA complements existing software-based process
- Bluespec as implementation language
- Pipeline stages are driven by Makefile
- Integrated with Vivado and Quartus command line flow

Applications

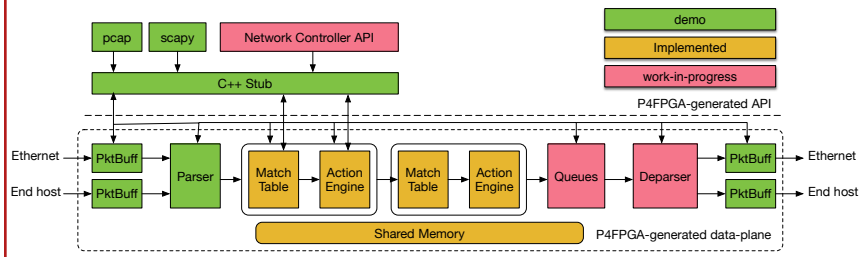


Switch/Router Intelligent-NIC Packet Scheduling

Status

We have implemented the following components:
- Packet Parser (Fixed parse graph from P4 program)
- Match Table (BCAM) (3)
- Packet Memory (Backed by Block RAM in FPGA)
- Tx/Rx Ring Buffer (Backed by Block RAM)
- Action Engine (Subset of primitives)
- Control and debug API through PCIe (Gen2)

Reference Architecture / Demo

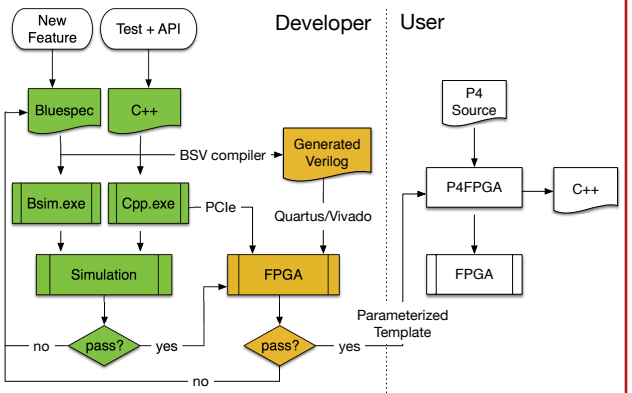


Host to FPGA communication (1)
- RPC-style function invocation
- Direct Memory Access (DMA)

```
// In C++
static MatchTable *device = 0;
device = new MatchTable(Ifc_MatchTable);
MatchEntry_t entry = { key: 0x80 };
device->add_entry(entry);
device->delete_entry(flowId);
```

```
// In Bluespec
interface MatchTable;
   interface Put#(MatchEntry_t) add_entry;
   interface Put#(FlowId_t) delete_entry;
   interface Put#(Tuple2#(FlowId_t, ActionEntry_t)) modify_entry;
endinterface
```

Extending P4FPGA



- Same bluespec and C++ for simulation and synthesis
- Automatic generation of Verilog from Bluespec
- Developer works in green flow for fast turn-around time

Contributions

- Compile P4 to multiple FPGA targets
- Open-source framework
- Full system and fast simulation
- RPC-style SW/HW communication
- Extensible for new data-plane features
- Modular and strong-typed language

To be released at p4fpga.org

Reference

(1) http://www.connectal.org/ (FPGA'15)
(2) Towards Programmable Packet Scheduling (HotNet'15)
(3) Modular SRAM-Based Binary Content-Addressable Memories (FCCM'15)