Target Architecture P4 Extension Compiled to Xilinx FPGA

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- Describe target data path in P4 “1.arch”
- … user describes elements in P4 “1.user”
- Compile to customized 100G hardware
- Demonstrated on Xilinx UltraScale FPGA

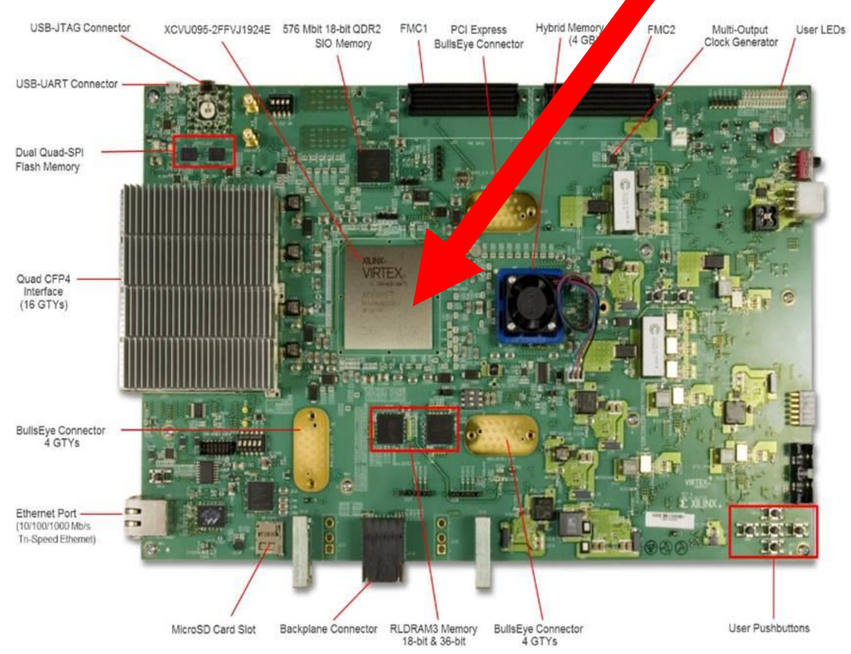
P4 1.arch

Front end

```
architecture_type IP_pipeline {
    // External interfaces to the architecture
    in packet instream;
    out packet outstream;

    // Two user-provided elements
    intern Parser parser;
    intern Processor processor;

    // One supplied element
    Deparser deparser;

    // Connectivity of the architecture
    connections {
        (instream, parser.packet_in),
        (parser.standard, processor.standard),
        (parser.ethernet, processor.ethernet),
        (parser.ipv4, processor.ipv4),
        (processor.standard, deparser.standard),
        (processor.ethernet, deparser.ethernet),
        (processor.ipv4, deparser.ipv4),
        (deparser.packet_out, outstream)
    }

    // One provided extern
    extern IPv4Checksum checksummer;

}
```

Xilinx Labs mapper

Xilinx SDNet



- Click-style architecture description
- Avoid vague “specifications in English”