Uniform Timestamping in P4

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Abstract

The ability to get precise timestamp reading at various stages in a packet processor pipeline is a critical requirement for carrying out any kind of analysis and comparison of the performance of hardware, software or a combination of the two. The P4 language currently does not have a *standardized* facility for reading time from hardware clocks. For the purposes of benchmarking, such a functionality is currently implemented in vendor-specific ways via the `extern` keyword, whereby an abstract, blackbox interface is defined for accessing the hardware clock. Among other variations, the granularity of timestamping differs from hardware to hardware making it difficult to faithfully compare the performance of different architectures. We wish to demonstrate the possibility of having a uniform API for accessing the hardware clock that would alleviate the problem of variation in the granularity of timestamping.

Demo Contents

We plan to adapt the Whippersnapper Benchmark Suite [1] to use the proposed extensions and to elaborate on the differences between the original methodology and the new approach. We would use a variety of Altera and Xilinx FPGA boards, for example, the NetFPGA SUME.

Keywords

timestamp, granularity, extern, benchmarking, P4, API.

References

[1] DANG, H. T., WANG, H., JEPSEN, T., BREBNER, G., KIM, C., REXFORD, J., SOUL, R., AND WEATHERSPOON, H. Whippersnapper: A p4 language benchmark suite. *ACM SIGCOMM SOSR* (2017).