

dRMT: Disaggregated Programmable Switching

We present dRMT (disaggregated Reconfigurable Match-action Table), a new architecture for programmable switches. dRMT overcomes two important restrictions of Reconfigurable Match-action Table (RMT), the predominant pipeline-based architecture for programmable switches: (1) RMT’s pipeline stages cannot share table memory, and (2) RMT is hard-wired to sequentially execute matches followed by actions in each stage. We show that these restrictions make it difficult, if not impossible, to execute packet processing programs efficiently on RMT.

dRMT resolves both issues by disaggregating the memory and processing resources of a programmable switch. dRMT moves table memories out of pipeline stages and into a centralized pool that is accessible through a crossbar. dRMT also replaces RMT’s match/action stages with a cluster of “match-action processors,” which can execute matches and actions in any order on incoming packets.

We show how to pre-schedule a dRMT system for a given P4 program at compile time to achieve deterministic throughput and latency. We also present a detailed hardware design for dRMT and analyze its implementation feasibility and cost. Our results show that dRMT achieves near-ideal hardware utilization and $1.04\text{--}1.71\times$ better throughput than RMT on real P4 programs, given similar hardware resources.