EE518 Analog IC-DESIGN LAB
Lab Project

Design a 2-Stage OP Amp in 180nm for low area design specification

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April 8, 2024

Contents

1 EXPERIMENT

Design a 2-stage Op-amp in 180 nm technology targeting low area

2 OBJECTIVE

To find W/L, gain-bandwidth product, output swing, ICMR, and compare the practical and theoretical results

3 General Specifications:

- VDD= 1.8V
- Reference current source (Iref) = 20 µA
- Slew rate = 1V/µs
- Phase margin$\geq$ 60
- Load Capacitance (CL) = 10pF
- ICMR = 0.6- 1.4 V

4 Low Area specifications:

- Gain $\geq$ 40dB
- GBW $\geq$ 10MHz
- Pdiss $\leq$1mW
- Lmax $\leq$ 2µm

5 Theory

5.1 Introduction

Op-amp is a common abbreviation for an operational amplifier. It's a high gain DC-coupled differential input voltage device. Op-amps typically create

outputs that are millions of times bigger than the voltage difference between their two input terminals. A negative feedback circuit is employed to manage the huge voltage gain. If negative feedback is not employed, the op-amp works as a comparator and provides positive feedback for regeneration in specific applications.

The practical structure of op-amp consists of 3 main block as shown in the

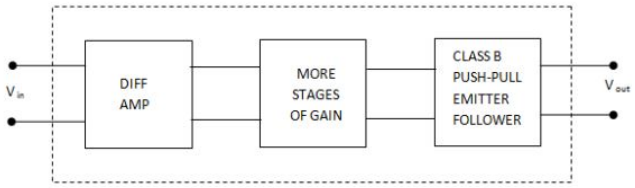

Figure 1: Block diagram of an op-amp

above figure

- The first block op-amp is an input differential amplifier that offers high input impedance, big CMRR and PSRR, low offset voltage, low noise, and high gain. The output should be single-ended to avoid symmetrical differential stages in the op-amp circuit. The input transistor should function in the saturation zone, resulting in a significant difference between the input and output signals of the input stages.

- Level shifting compensates for DC voltage changes in the input stage and ensures proper DC bias for subsequent stages.The gain offered by the input stage is insufficient; therefore, extra amplification is required. In differential-to-single-ended conversion, the input stage produces a differential output, followed by a conversion to single-ended signals.

- There is a third block called the output buffer. It provides the low impedance and high output current required to operate the opamp's load. It typically does not add to the increase. If the op-amp is an internal component of a switched-capacitor filter, the output load is a capacitor, therefore the buffer does not need to offer a high current or low output impedance. If the op-amp is at the filter output, it must drive a big capacitor or resistive load. To achieve high current driving capabilities and low output impedance, use big output devices with significant DC bias current.

5.2 Two stage Op-Amp

The below figure depicts a two-stage op-amp block diagram that includes two differential inputs and a common-source stage. The differential input gives an initial gain, which is then increased in the second stage to maximize output swing. The first stage of a two-stage amplifier has differential inputs that transform the input voltage to the current. The second stage is basically

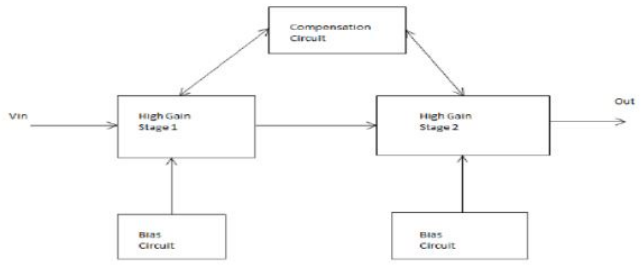

Figure 2: Block diagram of an two stage op-amp

a CS amplifier whose work is to convert current to voltage. The total DC gain of this two-stage structure can be expressed as,

$$A_{\mathrm{v}} = A_{\mathrm{v1}} * A_{\mathrm{v2}} \tag{1}$$

where,
A_{v} : Total gain of two stage Op-Amp
A_{v1} : Gain of first stage
A_{v2} : Gain of second stage

Advantages:
1) It has high output voltage swing.
Disadvantages:
1. It has compromised frequency response.
2. High power consumption due to two stages in its design.
3. It has poor negative supply PSRR at higher frequency.

6 Parameter Definitions

6.1 Trans conductance (g_m)

Trans conductance indicates sensitivity of circuit to its input voltage

$$g_m = \frac{dI_{ds}}{dV_{gs}} \tag{2}$$

6.2 Threshold Voltage(V_{th})

The minimum gate source voltage for which the MOSFET goes into inversion and turned on.

$$V_{th} = V_{gs} \ at \ which \ \frac{d^2 I_D}{dV_{GS}^2} \ is \ maximum \tag{3}$$

6.3 Early Voltage(V_A)

Since the drain and substrate PN diode becomes more reverse biased, the space change region increases at drain.since the drain current is more, there will be significant voltage drop across the space charge region. which is called *Early voltage*

$$V_A = \frac{1}{r_o I_{D_{sat}}} \tag{4}$$

6.4 Channel length modulation parameter(λ)

As we increase Vds, the pinch off point moves towards source which reduces effective channel length which is called channel length modulation. since there will be high electric field in space charge region it pulls electrons into drain. now the dependence of magnitude of current on Vds arises. the parameter that signifies the channel length modulation is λ

$$\lambda = \frac{1}{V_A} \tag{5}$$

7 AC analysis

By fixing all the DC values we make sure that the transistor is in saturation such that the we obtain significant AC parameters. now we apply small signal, make changes in circuit accordingly and observe the following parameters called AC Parameters.

7.1 AC parameters

7.1.1 voltage Gain $\mathbf{A_v}$:

After applying a significant DC input, we provide AC input such that there will be a significant voltage obtained at output. In order to compare the input and output obtained we make use of a parameter called AC Gain which is the ration of both.

$$A_v = \frac{v_{out}}{v_{in}} \tag{6}$$

7.1.2 Cut off frequency $\mathbf{f_c}$:

Any AC circuit will have a significant AC Gain till some frequency, after some frequency the gain of the circuit falls significantly. which we usually call roll off. cut off frequency is nothing but the value of frequency at which the gain will be 3dB less than that of maximum gain

$$\text{cut off frequency} = \text{frequency}_{\text{at 3db less than maximum gain}}$$

7.2 Output resistance $\mathbf{R_o}$

In practical circuits, we connect multiple blocks of analog circuits in cascade where one circuit loads another circuit with a resistance. Output of preceding circuit loads succeeding circuits with preceding circuits output resistance. Hence it is an important AC parameters.

$$Rout = \frac{V_{test}}{I_{test}} \tag{7}$$

7.3 Slew rate

Maximum rate of change of output is known as slew rate

$$Slewrate = \frac{dV_{out}}{dt}_{max} \tag{8}$$

7.4 CMRR

Usually in differential amplifiers, the common signal is considered as noise will be rejected and output will be free from noise. in order to quantify the ability to reject the noise we use CMRR

$$CMRR = \frac{A_{diff}}{A_{comm}} = infinite|_{ideal} \tag{9}$$

7.5 PSRR

A differential amplifier rejects common mode signal and amplifies differential signal. Hence to quantify the ability of differential circuit to amplify differential signal and suppress common mode signal we use PSRR

$$PSRR = \frac{\delta V_{cc}}{\delta V_{out}} = infinite|_{ideal} \tag{10}$$

7.6 ICMR

The range of common mode input we can apply so that all the transistors are in saturation

8 General design procedure

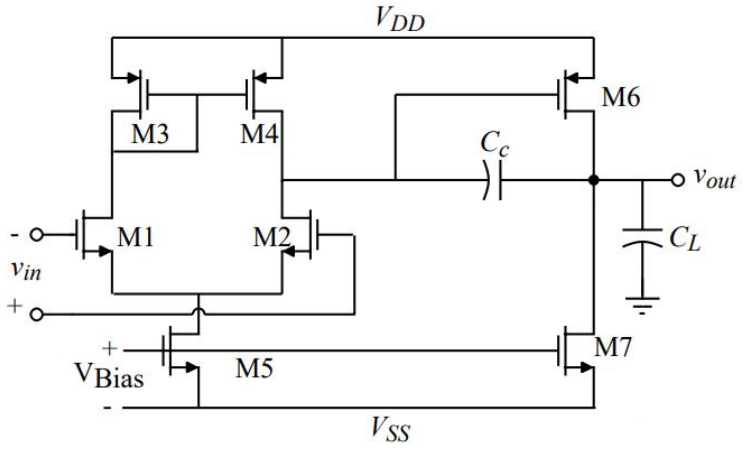

Figure 3: Design circuit of two stage op-amp

Notation: $S_{\mathrm{i}} = \frac{W_{\mathrm{i}}}{L_{\mathrm{i}}}$

8.1 DC Design procedure

For the best performance, keep all transistors in saturation.
M4 is the only transistor that cannot be forced into saturation by internal connections or external voltages. therefore we develop conditions to force M4 to be in saturation.
1) First assume VSG4 = VSG6. This will cause proper mirroring in M3 and M4. Also, the gate and drain of M4 will be at same potential to that of M4. hence it garuntees M4 to be in saturation.
2) If VSG 4 = VSG6, then

$$I6 = (\frac{S6}{S4})I4$$

3) However,

$$I7 = (\frac{S7}{S5})I5 = (\frac{S6}{S4}) * 2 * I4$$

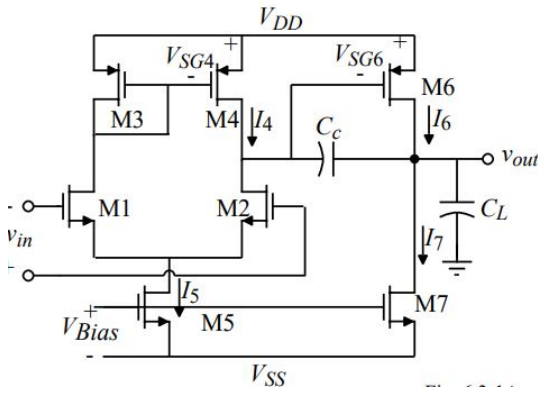

Figure 4: DC Design circuit of two stage op-amp

4) For balance, I6 must be equal to I7. Therefore

$$(\frac{S6}{S4}) = (\frac{2S6}{S4})$$

The above condition is called "DC Balance condition".If the above condition is maintained, VDG4 = 0 and M4 is saturated.

8.2 AC Design procedure

1) Check Idd from the power condition,

$$P_{\text{Disp}} = Idd * vdd = (I_{\text{ref}} + I5 + I7) * Vdd$$

2) From the desired phase margin, choose the minimum value for Cc, i.e. for a 60° phase margin we use the following relationship. This assumes that zero≥10GB.

$$CC \geq 0.22CL$$

3) From the slew rate, we can find I5

$$I5 = SR * CC$$

4)Since we know that,

$$GBW = \frac{Gm1}{CC}$$

,
find Gm1,Gm2 for the given GBW specification.
5)Find S1,S2 from the above obtained Gm1 using the below equation,

$$S1 = \frac{Gm1^2}{(\mu cox) * (I5)}$$

$$S2 = \frac{Gm2^2}{(\mu cox) * (I5)}$$

6)Find S3 from the ICMR_{Max} specification,

$$S3 = \frac{2Id3}{(\mu Cox)((Vdd - ICMR_{\text{Max}} - |Vtp| + Vtn)^2)}$$

7) Find $\text{Vd}_{\text{sat}}5$ using ICMR_{Min} specification,

$$Vd_{\text{sat}}5 \leq (ICMR_{\text{Min}} - Vth - \sqrt{\frac{2Id1}{\mu cox * S1}})$$

8) find S5, using above calculated Vdsat

$$S5 = \frac{2Id5}{\mu Cox * (Vdsat^2)}$$

9) Since, we are taking copy of current from Iref to I5,

$$\frac{I5}{S5} = \frac{I8}{S8}$$

we will be able to find S8, since we know I5,S5,I8(Iref) from the above calculations.
10)In order to have phase margin of 60 and Zero $\geq$ 10 GBW, we need to have,

$$Gm6 \geq Gm1$$

11) we can also find Gm4 since we know I4,S4

$$Gm4 = \sqrt{(\mu cox) * (S4) * (I4)}$$

12) Using "DC Balancing equation" we make sure that M4 and M6 are mirroring each other. For S6, we can make use of current copy equation.

$$S6 = (\frac{Gm6}{Gm4}) * S4$$

$$I6 = I4 * \frac{S6}{S4}$$

14) Since M6 and M7 are connected drain to drain, current must be same through both transistors, hence we find S7 using current mirror with M5 as below

$$S7 = (\frac{I6}{I5}) * S5$$

8.3 Parameter - Transistor dependencies

8.3.1 Parameters

- Slew rate SR = $\frac{I5}{CC}$ (Assuming I7 $\gg$ I5 and 0.22 CL $\geq$ Cc)
- First-stage gain Av1 = $\frac{Gm1}{I5*(L2+L4)}$
- Second-stage gain Av2 = $\frac{Gm6}{I6*(L6+L7)}$
- GBW = $\frac{Gm1}{CC}$
- Output pole P2 = $-\frac{Gm6}{CL}$
- RHP Zero Z = $\frac{Gm6}{CC}$
- Power = Vdd * (Iref + I5 + I6)
- ICMR$_{\text{min}}$ = $\sqrt{\frac{I5}{b1}}$+Vtn1+Vds5(Max)
- ICMR$_{\text{max}}$ = Vdd - $\sqrt{\frac{I5}{b3}}$+Vtn1-Vtp3

From the Above equations it is clear that Every transistor effects different factors in the design.
the summary of the relationship between both parameters and transistors is given in the below circuit.

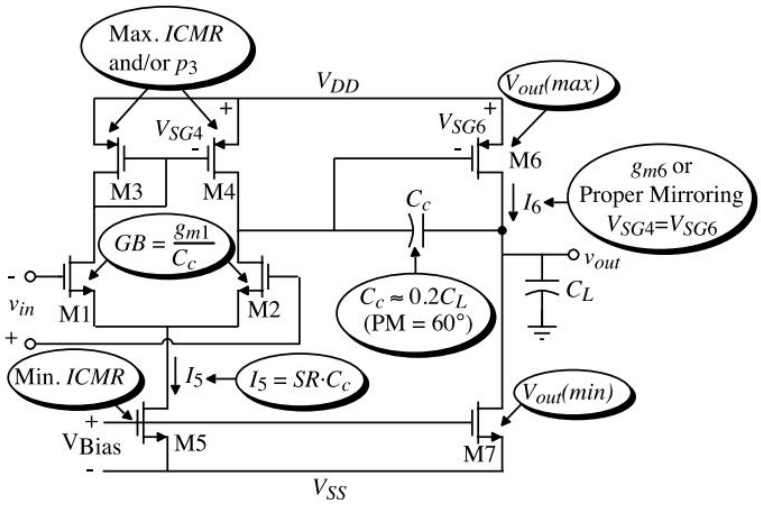

Figure 5: Design circuit of folded telescopic op-amp

9 Design approach for low area

- From the above parameter - transistor section we are clear about sizing of each transistor and its consequences.
- first, we find Maximum current Vdd can provide without failing power constraint (Idd = 550uA).
- Components of Idd are Iref, I5, I6. We know that Iref = 20uA, then I5 + I7 at max can be 530uA.
- since design procedure started from SR which is a function of I5 and CC we decide on them initially based on dependencies.
- I5 $\propto \frac{1}{S1}, \frac{1}{S8}, \frac{1}{S2}$,S3,$\frac{1}{S5}$,$\sqrt{Gm1}$,SR
- CC $\propto \frac{1}{GBW}$,Gm1,Gm6
- There is more Area dependence on I5 than on CC. Higher I5, Lower S1,S8,S2,S5.
- I5 will proportionally effect S3,S4 but both are limited by ICMR hence we can keep S3,S4 as 2.5.
- I5 is also proportional to I7(I6). But I5 and I6 both are limited by power constraints. Hence we cannot increase I5 as much as we want.
- since give SR(min) = 1, we have designed it for SR = 2.
- CC $\geq$ 0.22 CL, given CL = 10pf. Hence CC $\geq$ 22pf
- for SR = 2, We need I5 = 20uA.
- for safe stability , we need Zero ¿ 10 Pole_2. Hence we need CC $\geq$ 0.22 CL and Gm6 $\geq$ 10 Gm1.
- Above given constraints are not standardized but will ensure that circuit will not be unstable.
- we designed for Gm6 = 4 Gm1, still circuit is stable.
- using the above stated design procedure, we obtained values which are mentioned in the following sections.

9.1 Calculations

9.1.1 Step 1

We assumed a 60-degree phase margin and zero frequency at more than ten times the Gain Band width product.So, using the foregoing assumptions, we solved the equation of a one zero and two pole system to obtain the equation.

$$(millercapacitance)C_c > 0.22C_L \tag{11}$$

They given C_L is 10 pF.so we got miller capacitance is

$$C_c > 2.2pF \tag{12}$$

so we have taken minimum value 4.5pF

9.1.2 Step 2

The design specification specifies a slew rate of 10 volts per microsecond. In the circuit above, the maximum output value occurs when M1 is turned off and M2 is turned on. As M3 and M1 are in series, the M1 current is also zero. M3 and M4 are joined in

If the current is mirrored, then the M4 current is also zero.The entire VDD will be at the drain of M2, with M5 current flowing via the Cc capacitor.The slew rate for the above circuit will be

$$slewrate = \frac{I_5}{C_c} \tag{13}$$

we know slew rate and C_L from equation 8.so

$$I_5 = 20\mu A \tag{14}$$

9.1.3 Step 3

we have the gain band width product will be the voltage unit gain frequency .because we have dominent pole ,so we have 20 db decay will happens at unit gain frequency.

$$gm_1 = GBW * 2\pi C_c \tag{15}$$

we have the GBW ,cc values so we got gm_1

$$gm_1 = 622.03\mu A \tag{16}$$

we have the gm equation

$$gm_1 = \sqrt{2I_d\mu_n C_{ox}\frac{W}{L}_1} \tag{17}$$

if you substitute the values in above equation we got

$$\frac{W}{L}_1 = 56.55 \tag{18}$$

as we know M1 and M2 are need to be symmetric so we have taken

$$\frac{W}{L}_1 = \frac{W}{L}_2 = 56.55 \tag{19}$$

9.1.4 Step 4

They given maximum ICMR value 1.6.so from above circuit we for M1 in saturation

$$V_{d1} > V_g - V_{th1} \tag{20}$$

$$V_g < V_{d1} + V_{th1} \tag{21}$$

$$V_g < (V_{dd} - V_{sg3}) + V_{th1} \tag{22}$$

$$V_g < (V_{dd} - (V_{tp} + \sqrt{\frac{2I_D}{\mu_p C_{ox}\frac{W}{L}3}}) + Vth1 \tag{23}$$

here gate voltage is the maximum ICMR voltage .so if you you substitute the all values you got the (WŁ) of M3

$$ICMRmax = (Vdd - (V_{tp} + \sqrt{\frac{2I_D}{\mu_p C_{ox}\frac{W}{L}3}}) + Vth1 \tag{24}$$

$$\frac{W}{L}_3 = 2.5 \tag{25}$$

as we know M3 and M4 are need to be symmetric so we have taken

$$\frac{W}{L}_3 = \frac{W}{L}_4 = 2.5 \tag{26}$$

9.1.5 Step 5

we know the ICMR minimum value.it will be taken from minimum gate voltage so all transistor are in saturation.so

$$V_{dsat} = ICMR_{min} - \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}1}} - Vthn \tag{27}$$

if you substitute all the values you got the Vdsat value.

$$V_{dast} = 0.147 \tag{28}$$

if you substitute the value on the current equation you got the

$$\frac{W}{L}_5 = 11.609 \tag{29}$$

so we have taken

$$\frac{W}{L}_5 = 11.609 \tag{30}$$

9.1.6 Step 6

as we taken the assumption zero frequency is 10 times of the GBW. we got the

$$gm_6 > 4 * gm_1 \tag{31}$$

we know the gm_1 from the eqution 12

$$gm_6 > 2488.12\mu A \tag{32}$$

we know M6 and M4 are in current mirror so .

$$\frac{(W/l)_6}{(W/l)_4} = \frac{I_6}{I_4} = \frac{gm_6}{gm_4} \tag{33}$$

so we know the $(w/l)_4$ and I_4 so from gm equation we got the

$$gm_4 = 58.561\mu A \tag{34}$$

from equation 29, we got

$$(w/l)_6 = 106.22 \tag{35}$$

from equation 29 we can calculate the

$$Id_6 = 424.8\mu A \tag{36}$$

9.1.7 Step 7

$$\frac{(W/l)_7}{(W/l)_5} = \frac{I_7}{I_5} \tag{37}$$

M6 and M7 are in series so both currents are equal.so we got

$$(w/l)_7 = 248.27 \tag{38}$$

we got the all the (wł) ratios ,we need to calculate the lengths.we know gain of two stage op amp is

$$gain = gm_1 gm_6 (r01||r04)(ro6||ro7) \tag{39}$$

10 waveforms

10.1 DC analysis

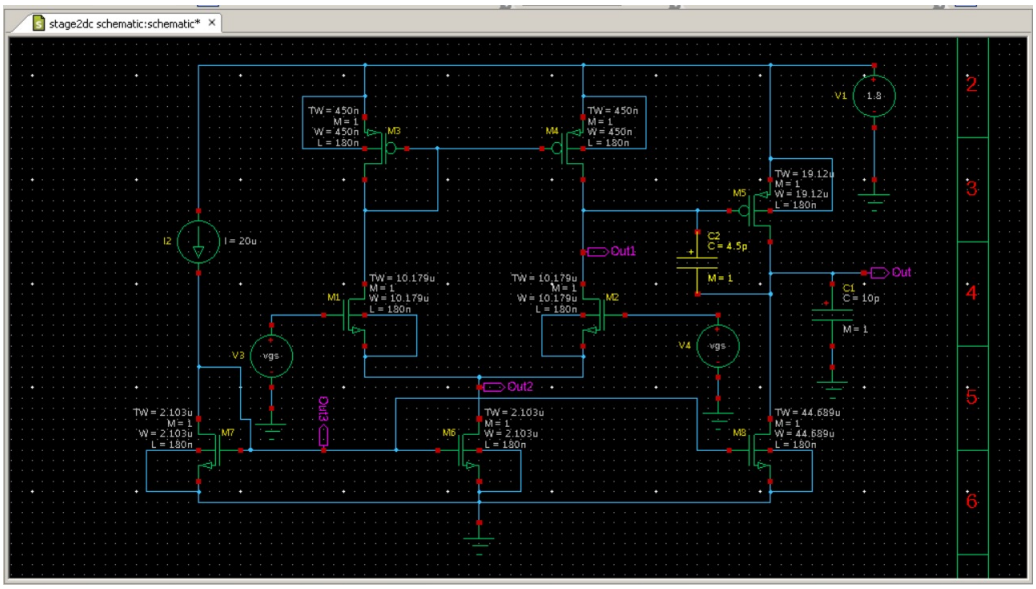

Figure 6: circuit diagram for DC analysis of 2 stage Op-Amp

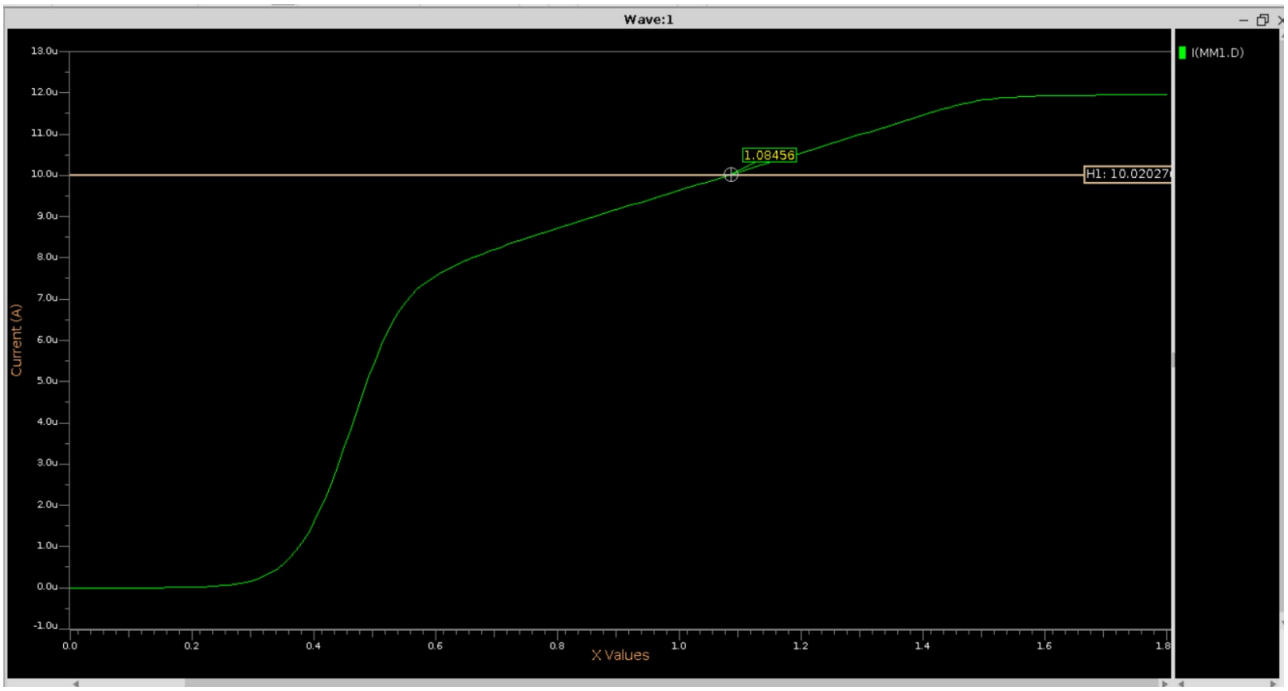

Figure 7: DC analysis of 2 stage Op-Amp

10.2 AC analysis

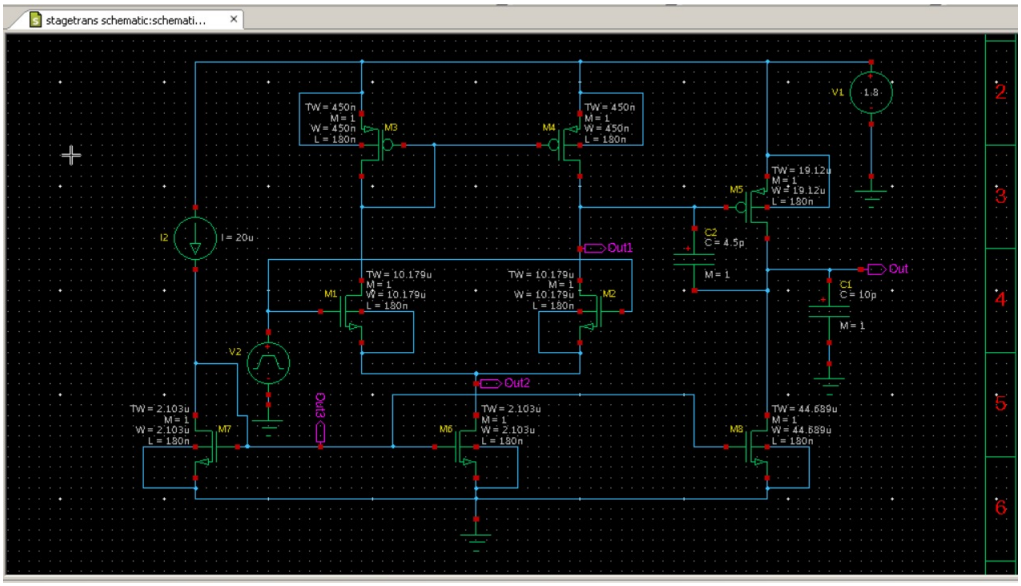

Figure 8: circuit diagram for AC analysis of 2 stage Op-Amp

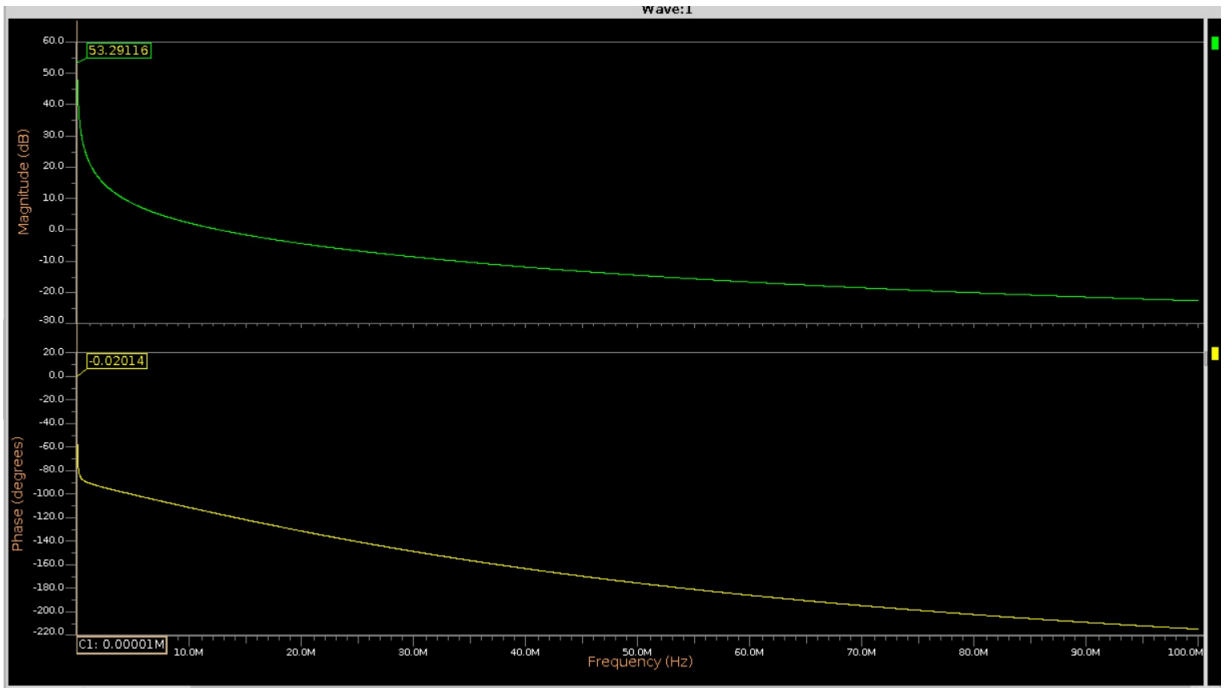

Figure 9: Amax of 2 stage Op-Amp

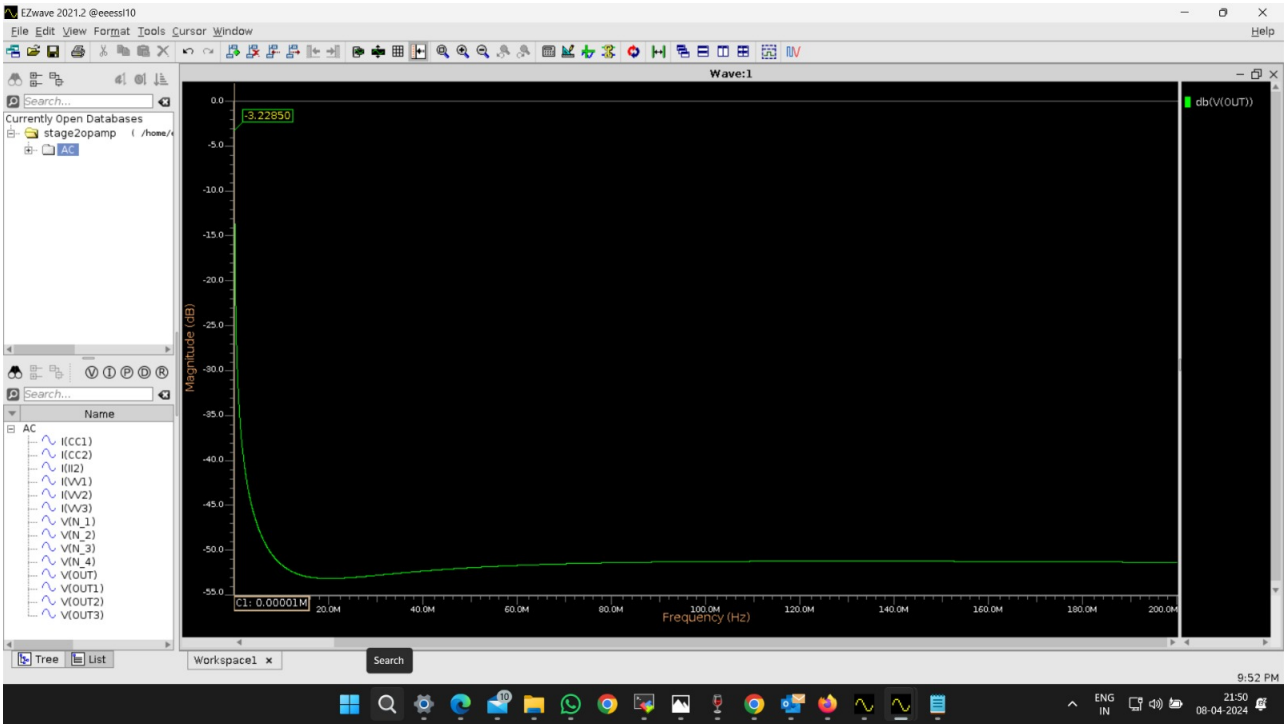

Figure 10: Acm of 2 stage Op-Amp

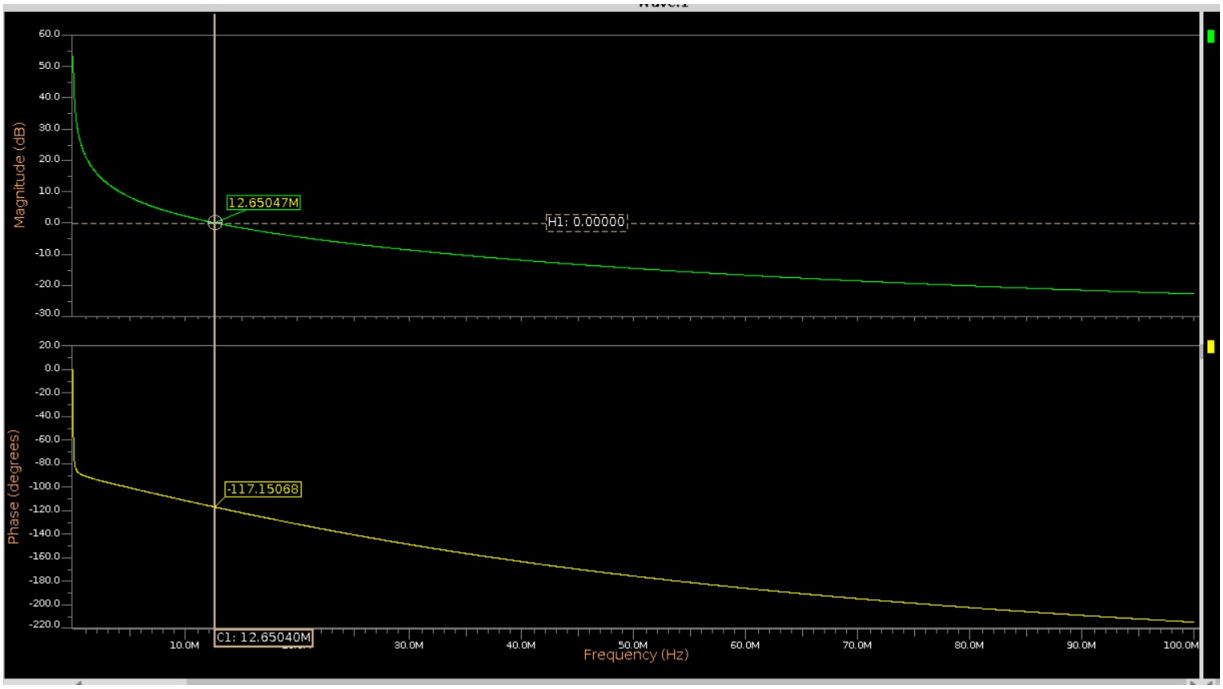

Figure 11: GBW and Phase Margin of 2 stage Op-Amp

10.3 PSRR

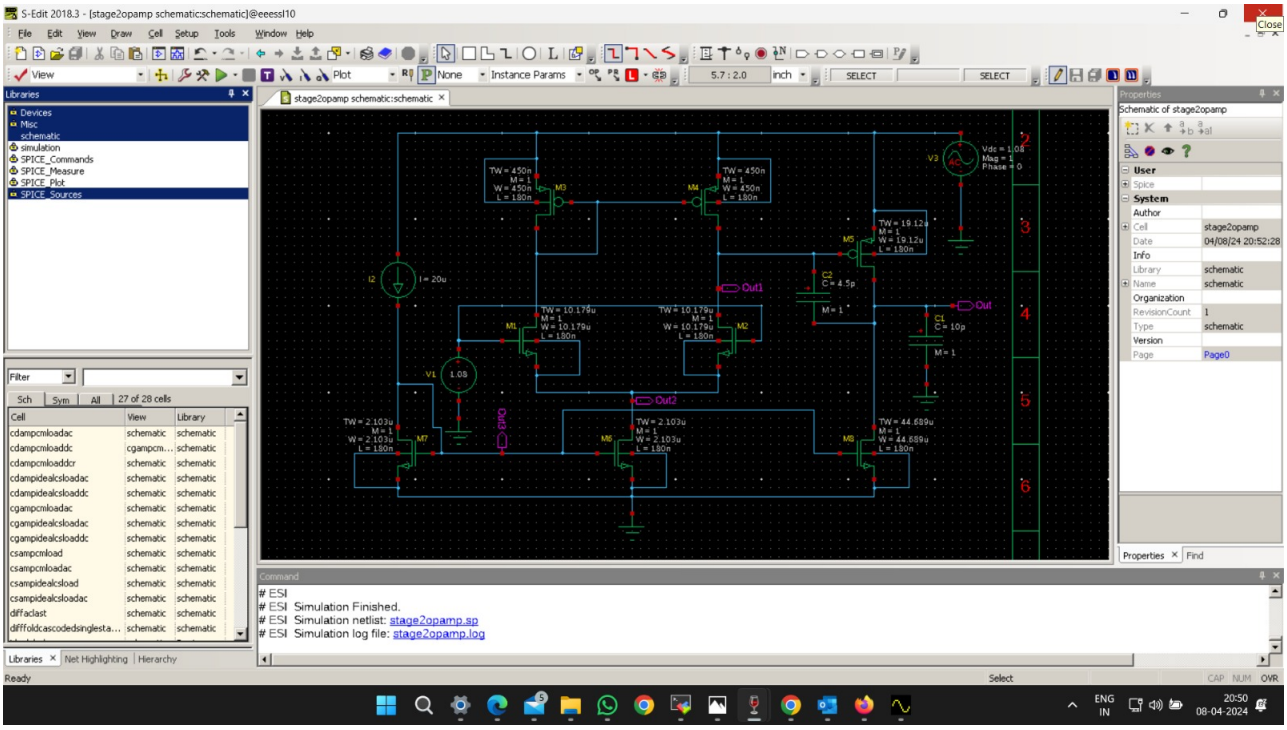

Figure 12: circuit diagram for PSRR analysis of 2 stage Op-Amp

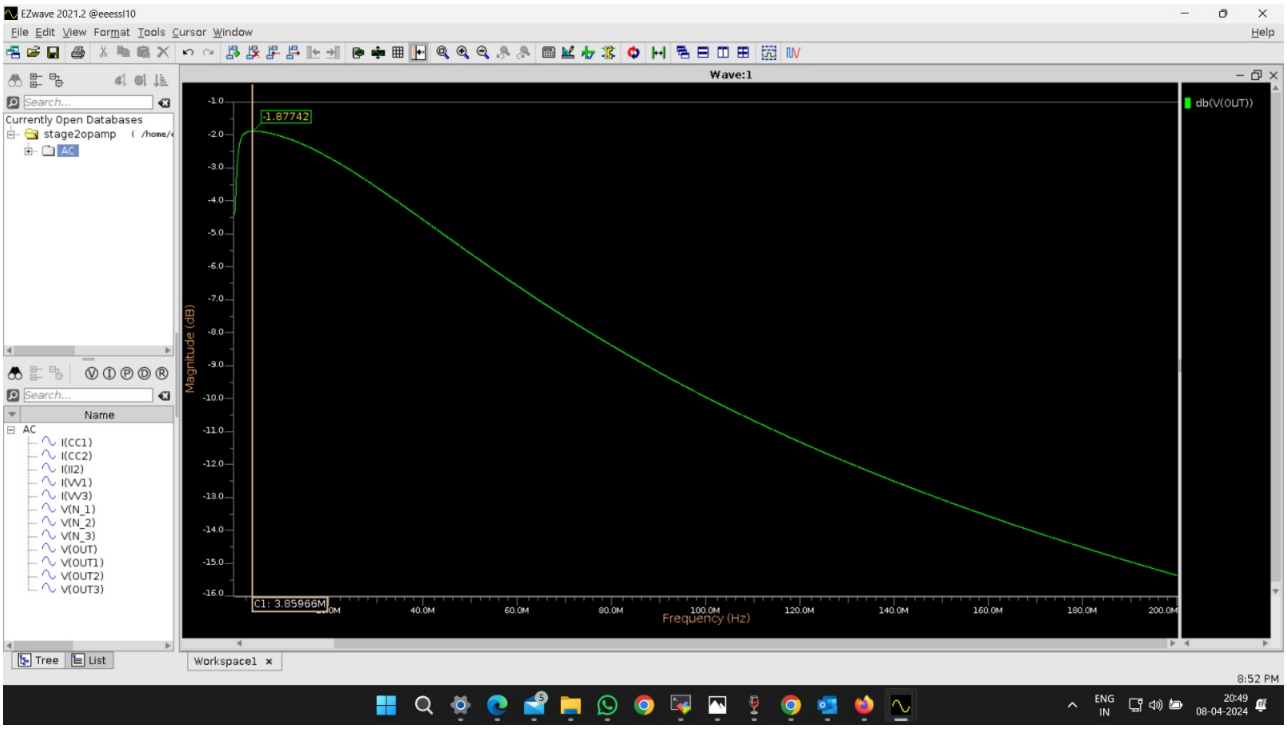

Figure 13: PSRR analysis of 2 stage Op-Amp

10.4 ICMR and OCMR

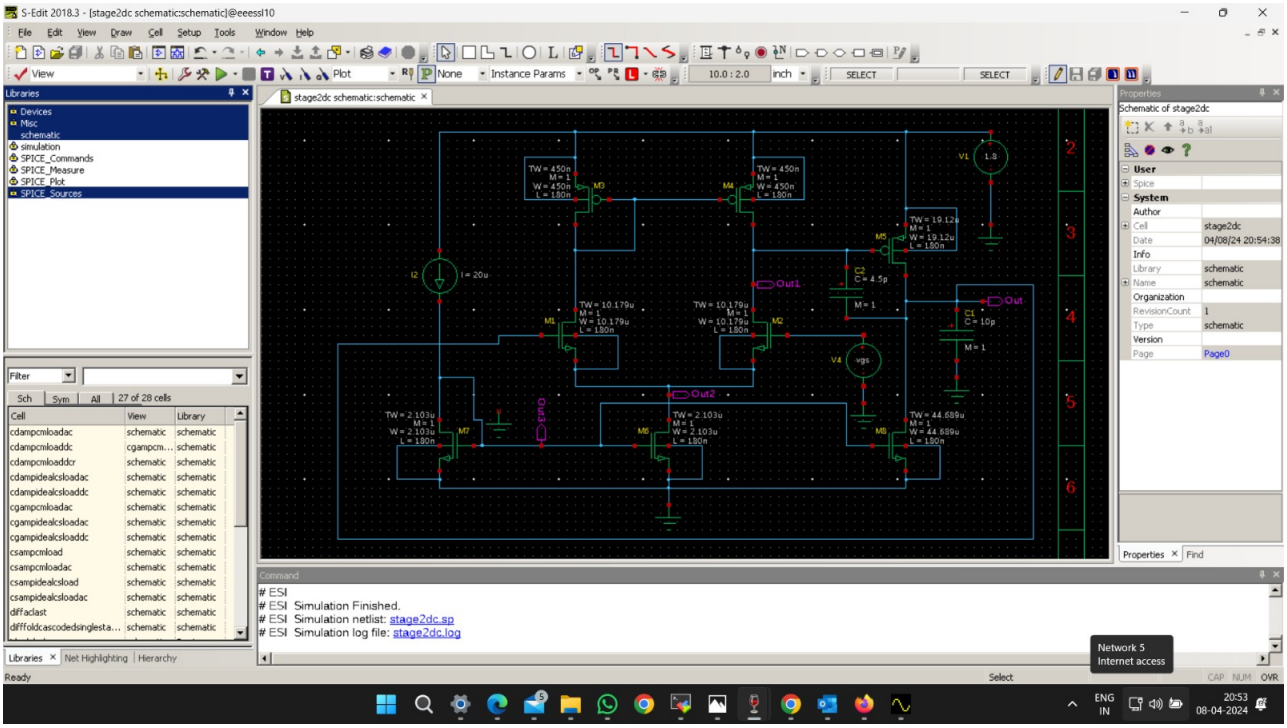

Figure 14: circuit of ICMR and OCMR analysis of 2 stage Op-Amp

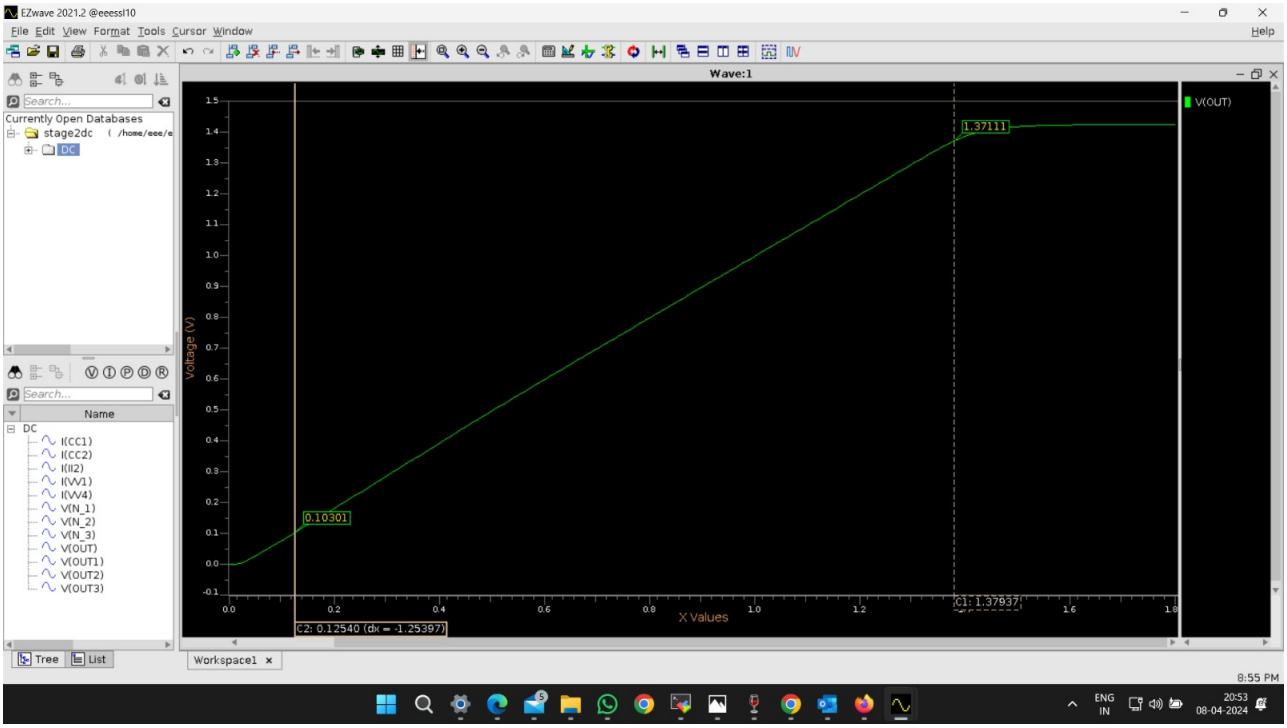

Figure 15: results of ICMR and OCMR analysis of 2 stage Op-Amp

10.5 Slew rate

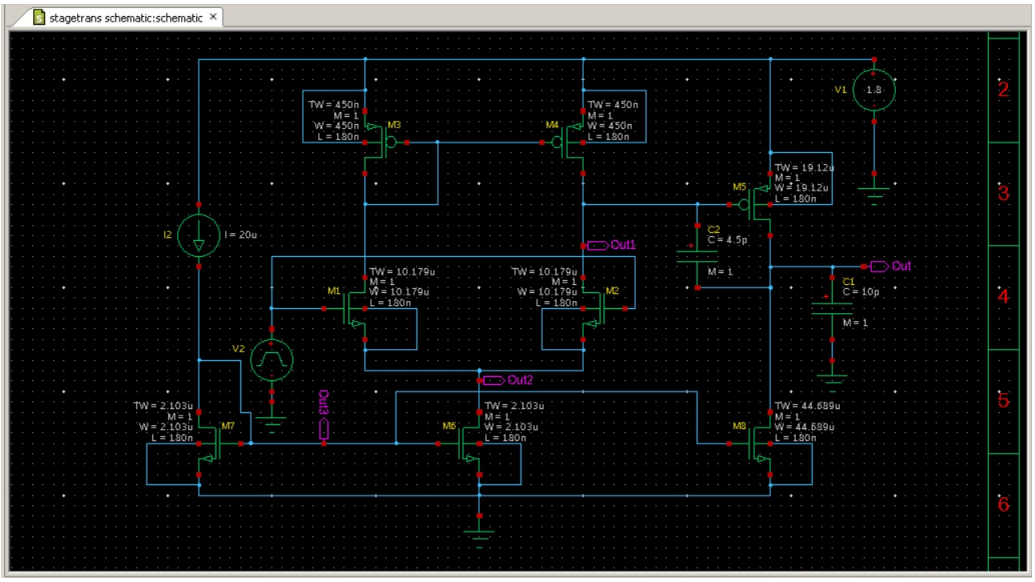

Figure 16: Circuit diagram to find the slew rate

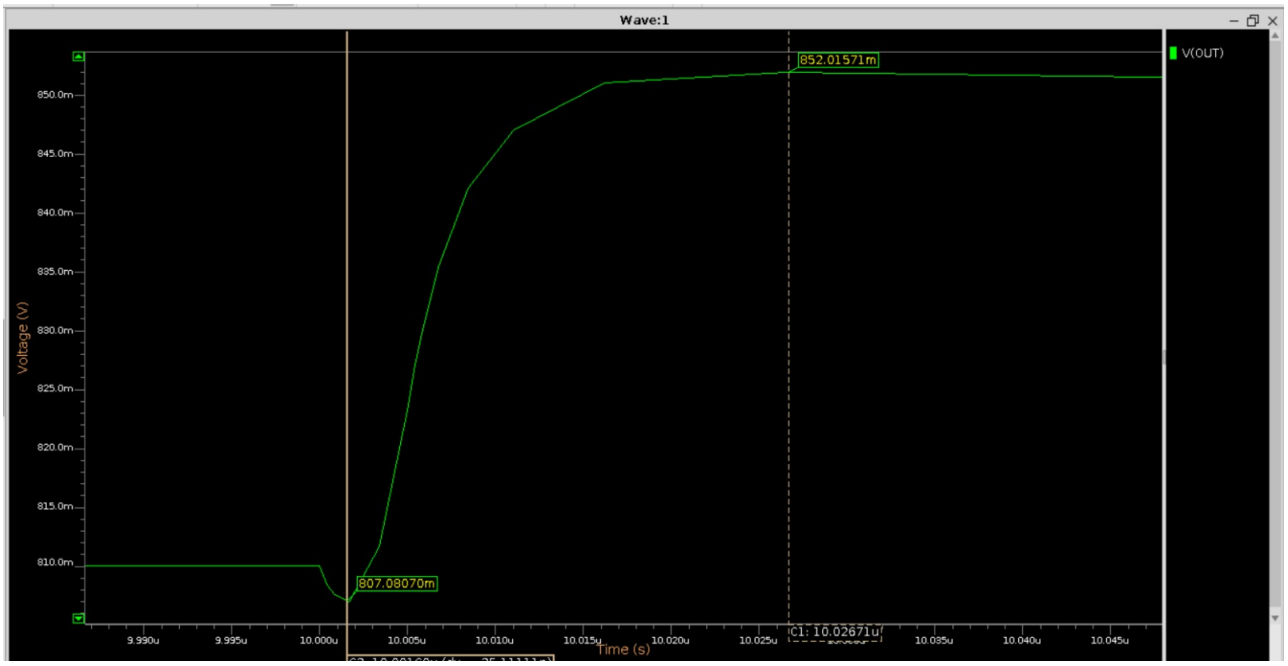

Figure 17: Results of slew rate

11 Comparsion Tables

12 RESULTS

12.1 (W/l) of all transistors

Transistor	aspect ratio	width	length
M1	56.55	10.179 um	180 nm
M2	56.55	10.179um	180 nm
M3	2.5	450 nm	180 nm
M4	2.5	450 nm	180 nm
M5	11.689	2.103 um	180 nm
M6	106.22	19.12 um	180 nm
M7	248.27	44.68 um	180 nm
M8	11.689	2.103 um	180 nm

12.2 CAPACITOR VALUE

capacitor	value
C_c	4.5pf
c_L	10pf

12.3 AC Results

Parameter	value
Gain	53.29dB
3dB-Bandwidth	0.0284Mhz
GBW	12.65Mhz
PM	62.86
CMRR	20dB
PSRR	-1.877db

12.4 Transient analysis

parameter	theoretical value	practical value
Slew rate	2	1.7
ICMR max	1.4	1.377
ICMR min	0.6	0.103
OCMR max	-	1.379
OCMR min	-	0.125

13 OBSERVATIONS

- In this project we considered low area as our design requirement. we desgined and analysed various parameters.
- Practically obtained results are compared to the theoretical values.
- We obtained higher gain as compared to other configurations since we are cascading two gain stages
- Phase margin and stability are maintained.

14 CONCLUSION

A low area 2 stage op-amp is designed with 180nm technology in mentor graphics tool.