Assignment - 7

For lanes - L1 AND L4 - Green(30 sec), Yellow(5sec), Red
And for lanes - L0,L2,L3 - Green(60sec), Yellow(5sec), Red

State	Red	Yellow	Green	Time Period
S0	11001	00010	00100	5 sec
S1	11011	00000	00100	55 sec
S2	10011	00100	01000	5 sec
S3	10111	00000	01000	55 sec
S4	00111	01000	10000	5 sec
S5	01111	00000	10000	25 sec
S6	01110	10000	00001	5 sec
S7	11110	00000	00001	55 sec
S8	11100	00001	00010	5 sec
S9	11101	00000	00010	25 sec
S10	10110	01000	00001	5 sec
S11	11010	00001	00100	5 sec

Based on the input of tr1 and tr4 ,4 cases are possible :
The 4 cases and their respective outcomes are given below :

Case 1 (tr1=0 and tr4=0):
S0 – S1 – S2 – S3 – S10 – S7 – S11 – S1 – S2 – S3 – S10 – S7 – S11 – S1 – and the cycle continues.

Case 2 (tr1=1 and tr4=0):
S0 – S1 – S2 – S3 – S10 – S7 – S8 – S9 – S0 – S1 – S2 – S3 – S10 – S7 – S8 – S9 – S0 – and the cycle continues.

Case 3 (tr1=0 and tr4=1):
S0 – S1 – S2 – S3 – S4 – S5 – S6 – S7 – S11 – S1 – S2 – S3 – S4 – S5 – S6 – S7 – S11 – S1 – and the cycle continues.

Case 4 (tr1=1 and tr4=1):
S0 – S1 – S2 – S3 – S4 – S5 – S6 – S7 – S8 – S9 – S0 – S1 – S2 – S3 – S4 – S5 – S6 – S7 – S8 – S9 – S0 – and the cycle continues.

I have considered the entire assignment as a FInite State Machine and shown the entire finite state machine in a combination of 12 states. Some states are not reachable based on the condition of tr1 and tr4 value.

As all the process statements in VHDl run concurrently and the statements inside a process statement are compiled sequentially, So I have used two processes to design the finite state machine.

One Process is used to define all the states of the FINITE STATE MACHINE and the other process is used to show the different transitions from one state to other based on the value of tr1 and tr4. And the same process is also used to control the timings of each and every state transition in the FINITE STATE MACHINE.

The clock that I have implemented in the testbench has a time period of 1 sec and in main code , I have counted the number of clock cycles using a variable count and using the variable and if condition, i have controlled the state transition time in the Finite State Machine implemented.