IITB-RISC

Multi-Cycle Implementation

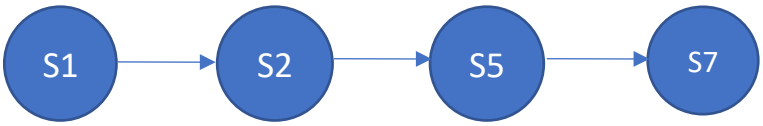
State Elaboration

S1	PC => MEM_a PC => R7 PC => ALU_a +1 => ALU_b ALU_out => PC MEM_d => IR		S6	IR_{6-8} => RF_a3 T1 => RF_d3
S2	IR_{9-11} => RF_a1 IR_{6-8} => RF_a2 RF_d1 => T1 RF_d2 => T2 IR_{0-7} => PE_{in}		S7	IR_{3-5} => RF_a3 T1 => RF_d3
S3	T1 => ALU_a IR_{0-5} => SE6 => ALU_b ALU_out => T1		S8	IR_{0-8} => SE9 => RF_d3 IR_{9-11} => RF_a3
S4	T2 => ALU_a IR_{0-5} => SE6 => ALU_b ALU_out => T2		S9	T2 => MEM_a MEM_d => T2
S5	T1 => ALU_a T2 => ALU_b ALU_out => T1		S10	T1 => MEM_a MEM_d => T2

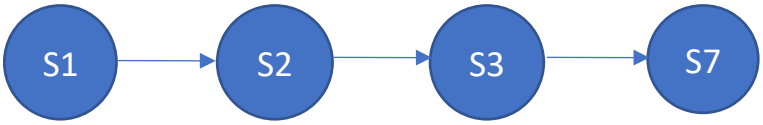
S11	T1 => MEM_d T2 => MEM_a		S16	T2 => MEM_d T1 => MEM_a , ALU_a T1 => ALU_b ALU_out => T1
S12	R7 => RF_d3 IR_{9-11} => RF_a3 IR_{0-8} => SE9 => ALU_b PC(R7 + 1) => ALU_a ALU_out => PC,R7		S17	R7(PC-1) => ALU_a IR_{0-5} => SE6 => ALU_b ALU_out => PC,R7
S13	IR_{6-8} => RF_a1 PC(R7+1) => RF_d3 IR_{9-11} => RF_d3 RF_d1 => PC,R7		S18	T2 => ALU_b +0 => ALU_a T2 => RF_d3 IR_{9-11} => RF_a3
S14	T2 => RF_d3 PE_out => RF_a3 T1 => ALU_a +1 => ALU_b ALU_out => T1		S19	T1 => ALU_a T2(left shifted by 1) => ALU_b ALU_out => T1
S15	PE_out => RF_a1 RF_d1 => T2		S20	T1 => ALU_a IR_{0-8} => SE9 => ALU_b ALU_out => PC,R7

State Transition For Instruction

1) ADD



2) ADC



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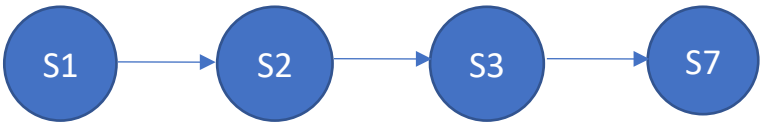

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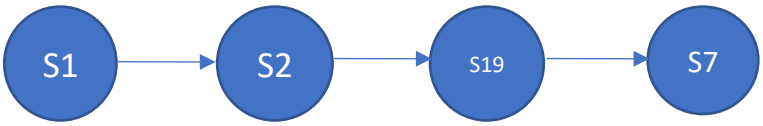

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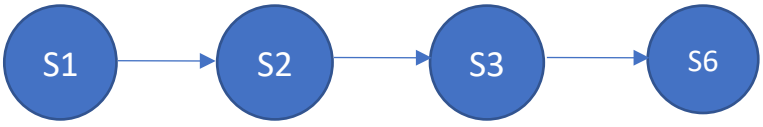
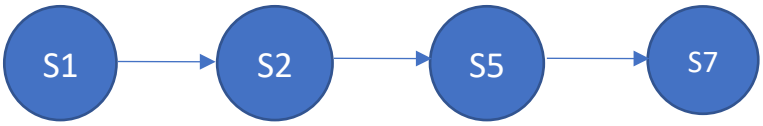
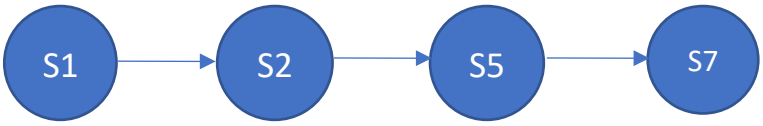


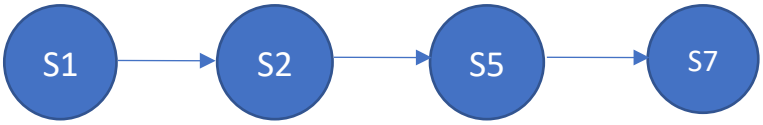
6) NDU



7) NDC



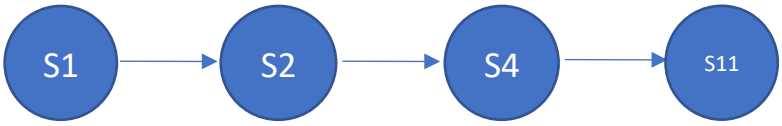
8) NDZ



9) LHI

10) LW

11) SW



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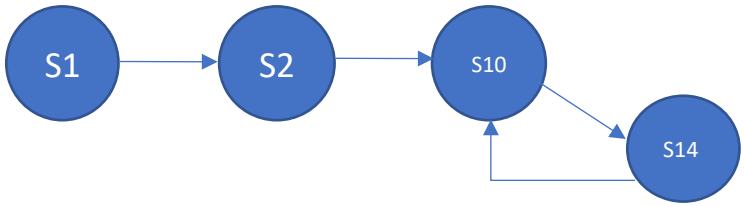
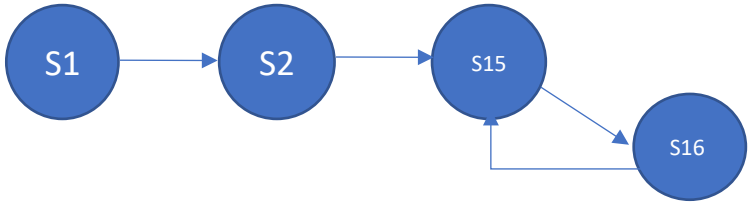
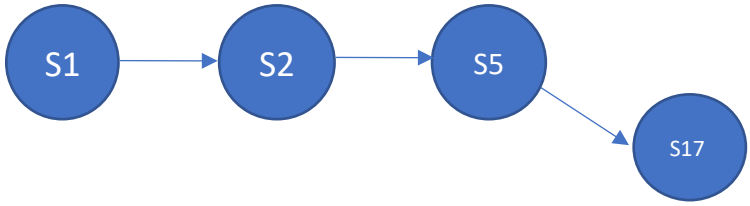


13) SM



14) BEQ



15) JAL

16) JLR

17) JRI