Computer-Aided VLSI System Design
Final Report

組別: 40

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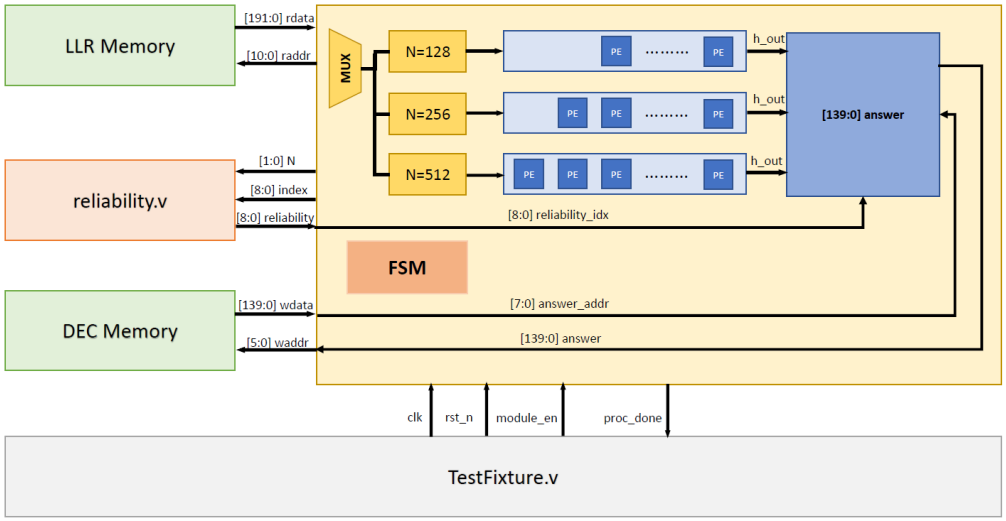
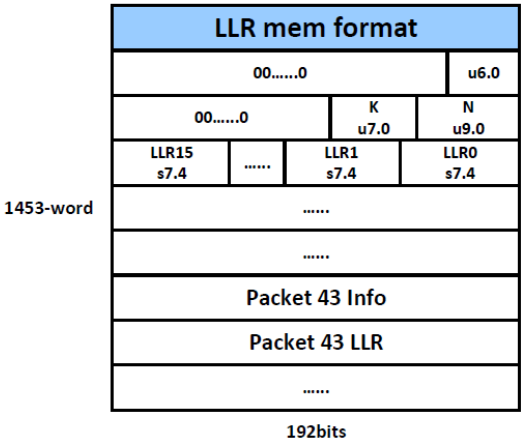
I. Introduction

a. Block Diagram



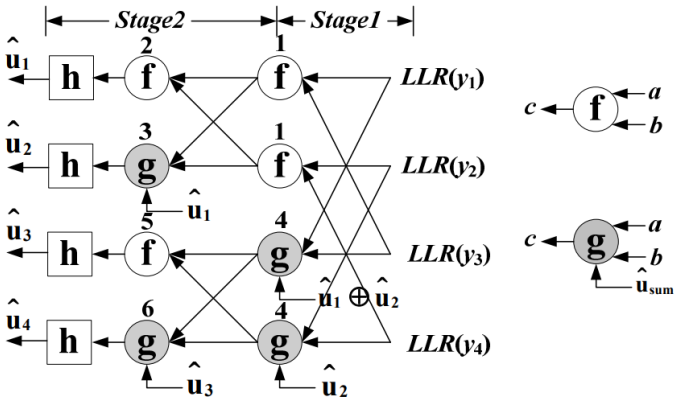
b. Architecture



1. **Read data:** 1 個 packet(32 words)用 N=128/256/512 分別定義 8/16/32 個 cycles 讀入 LLR memory 的資料。
2. **Decode:**使用 SC decoder 分成 f 及 g 運算

$$f(a,b)=\text{sign}(a)\text{sign}(b)\min(|a|,|b|)$$

$$g(a,b)=a(-1)^{\hat{u}_{sum}}+b$$



II. Optimization

原先將 decoder 展開，分成多個 f、g 作運算，後將 f、g 數量減少，並作了以下優化方式降低面積、功耗、cycle 數量:

A. Register sharing

起初，我們將 f 與 g function 分開運算，後將 2 function 合併節省面積及功耗。

B. Reduce cycle time

原先一次讀完所有 packet 中的 word 才運算，後改為拿到 2 個 word 就開始 decode。

C. Zero node cancellation

預先判斷 frozen，decode 前先去尋找非 frozen 需要運算的位置，找到後再開始 decode。

D. Compile method

1、 compile ultra

合成時使用 compile_ultra 將面積縮小。

2、 gated clock

clock_gating 將面積縮小及省功耗

E. APR method

1、 reduce amount of stripes

將 stripe 數量減少，減為一組，power 降低 1/3

2、 increase amount of fanout

將 fanout 調到 4 降低面積及功耗。

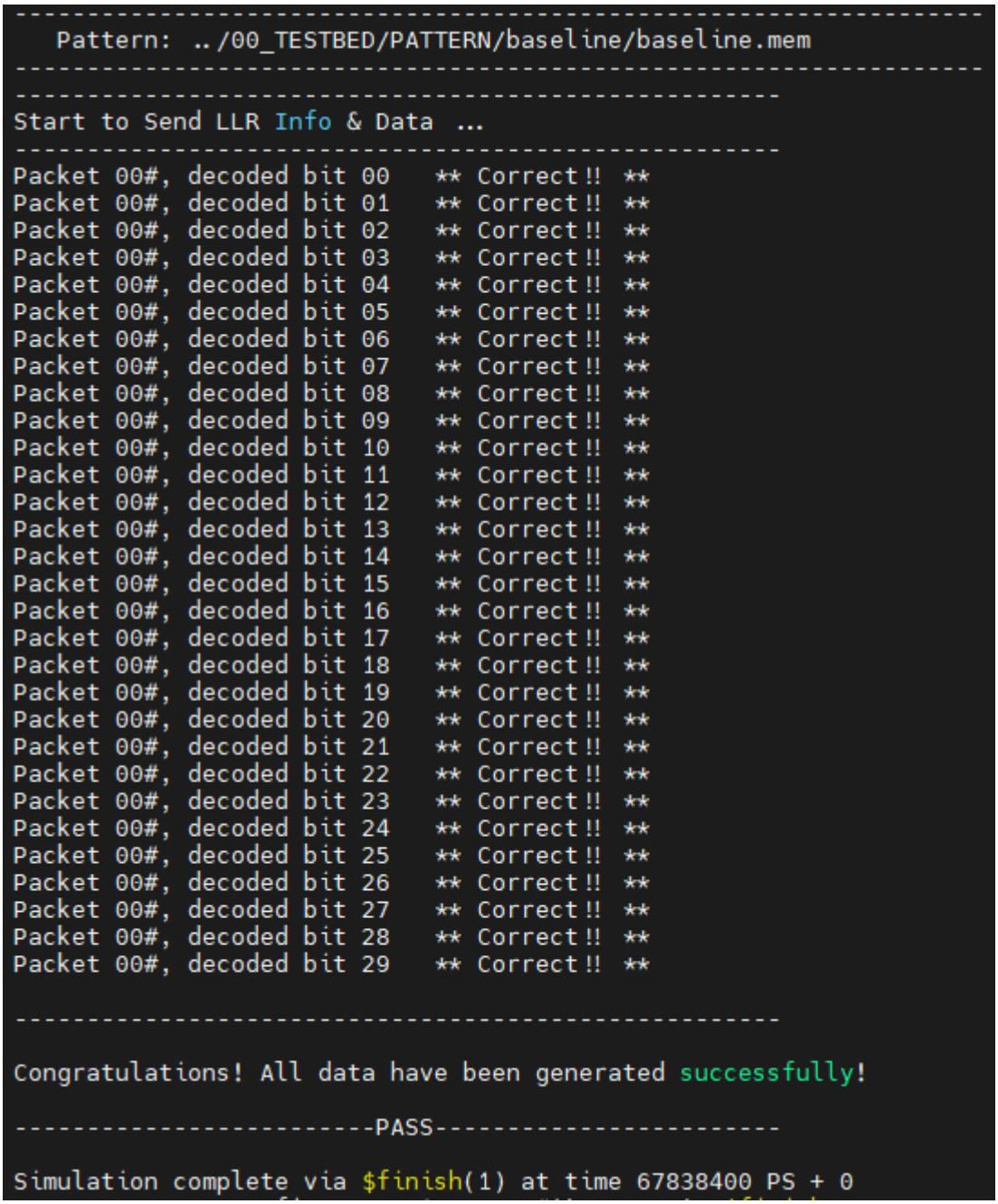
III. Result

a. RTL result

```
------------------------------------------------------------------
   Pattern: ../00_TESTBED/PATTERN/baseline/baseline.mem
------------------------------------------------------------------
--------------------------------------------------
Start to Send LLR Info & Data  ...
--------------------------------------------------
Packet 00#, decoded bit 00   ** Correct!! **
Packet 00#, decoded bit 01   ** Correct!! **
Packet 00#, decoded bit 02   ** Correct!! **
Packet 00#, decoded bit 03   ** Correct!! **
Packet 00#, decoded bit 04   ** Correct!! **
Packet 00#, decoded bit 05   ** Correct!! **
Packet 00#, decoded bit 06   ** Correct!! **
Packet 00#, decoded bit 07   ** Correct!! **
Packet 00#, decoded bit 08   ** Correct!! **
Packet 00#, decoded bit 09   ** Correct!! **
Packet 00#, decoded bit 10   ** Correct!! **
Packet 00#, decoded bit 11   ** Correct!! **
Packet 00#, decoded bit 12   ** Correct!! **
Packet 00#, decoded bit 13   ** Correct!! **
Packet 00#, decoded bit 14   ** Correct!! **
Packet 00#, decoded bit 15   ** Correct!! **
Packet 00#, decoded bit 16   ** Correct!! **
Packet 00#, decoded bit 17   ** Correct!! **
Packet 00#, decoded bit 18   ** Correct!! **
Packet 00#, decoded bit 19   ** Correct!! **
Packet 00#, decoded bit 20   ** Correct!! **
Packet 00#, decoded bit 21   ** Correct!! **
Packet 00#, decoded bit 22   ** Correct!! **
Packet 00#, decoded bit 23   ** Correct!! **
Packet 00#, decoded bit 24   ** Correct!! **
Packet 00#, decoded bit 25   ** Correct!! **
Packet 00#, decoded bit 26   ** Correct!! **
Packet 00#, decoded bit 27   ** Correct!! **
Packet 00#, decoded bit 28   ** Correct!! **
Packet 00#, decoded bit 29   ** Correct!! **

--------------------------------------------------

Congratulations! All data have been generated successfully!

-------------------------PASS-------------------------

Simulation complete via $finish(1) at time 65954 NS + 0
../00_TESTBED/testfixture.v:189     #(`CYCLE/2); $finish;
```

RTL 通過 Baseline pattern，當 cycle time 為 7 ns 時，latency 為 65954 ns。

b. Gate-SIM result



RTL 通過 Baseline pattern，當 cycle time 為 7 ns 時，latency 為 67838.4 ns。

c. APR