# **Traditional Uses of Compilers**

#### Last lecture

- Optimizing OO languages

### **Today**

- Start low-level issues
- Register allocation

CIS 570 Lecture 18

Register Allocation

2

# **Register Allocation**

#### Problem

- Assign an unbounded number of symbolic registers to a small, fixed number of architectural registers (which might get renamed by the hardware to some number of physical registers)
- Simultaneously live data must be assigned to different architectural registers

#### Goal

- Minimize overhead of accessing data
  - Memory operations (loads & stores)
  - Register moves

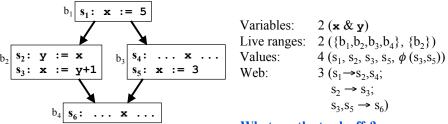
# **Granularity of Allocation**

### What is allocated to registers?

- Variables
- Live ranges (i.e., set of basic blocks in which a variable is live)
- Values (i.e., definitions; same as variables with SSA)



→ Webs (*i.e.*, du-chains with common uses)



What are the tradeoffs?

Each allocation unit is given a symbolic register name (e.g., s1, s2, etc.)

CIS 570 Lecture 18 Register Allocation

### **Scope of Register Allocation**

**Expression** 

Local



Global



# **Local Register Allocation for Loops**

#### Idea

- Estimate the benefit of allocating variables in basic blocks or loops
- Allocate variables with greatest benefit to registers
- Estimates are a function of execution frequency (from profiles, heuristics)

### **Surprisingly effective!**

- IBM 360/370 Fortran H compiler (1968)

CIS 570 Lecture 18

Register Allocation

6

### **Local Register Allocation for Loops (cont)**

#### **Definitions**

- *ldcost*: Cost (time) of load instruction
- stcost: Cost of store instruction
- mvcost: Cost of register-to-register transfer instruction
- usesave: Savings (time) for each use of variable in a register vs. memory
- defsave: Savings for each assignment of variable in a register vs. memory
- Static counts for variable v:  $u_i$ ,  $d_i$ ,  $l_i$ ,  $s_i$  ( $l_i$  and  $s_i$  are 0 or 1)

Benefit of allocating variable v to a register in block b<sub>i</sub> is

$$netsave(v,i) = u_i \cdot usesave + d_i \cdot defsave - l_i \cdot ldcost - s_i \cdot stcost$$

$$benefit(v, L) = 10^{depth(L)} \sum_{i \in blocks(L)} netsave(v, i)$$

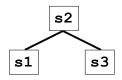
CIS 570 Lecture 18

Register Allocation

# Global Register Allocation by Graph Coloring

### Idea

- 1. Construct interference graph G=(N,E)
  - Represents notion of "simultaneously live"
  - Nodes are units of allocation (e.g., variables, live ranges, webs)
  - $-\exists$  edge  $(n_1, n_2) \in E$  if  $n_1$  and  $n_2$  are simultaneously live
  - Symmetric (not reflexive nor transitive)
- 2. Find k-coloring of G (for k registers)
  - Adjacent nodes can't have same color
- 3. Allocate the same register to all allocation units of the same color
  - Adjacent nodes must be allocated to distinct registers

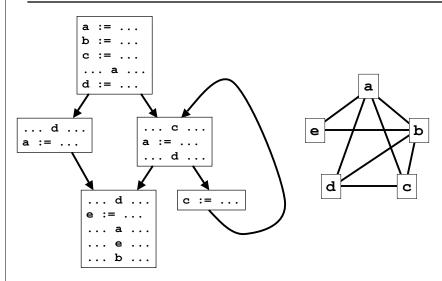


CIS 570 Lecture 18

Register Allocation

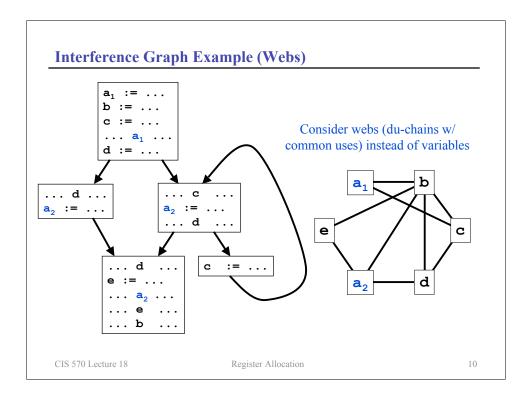
8

### **Interference Graph Example (Variables)**



CIS 570 Lecture 18

Register Allocation



# **Computing the Interference Graph**

### Use results of live variable analysis

CIS 570 Lecture 18

Register Allocation

# **Allocating Registers Using the Interference Graph**

### K-coloring

- Color graph nodes using up to k colors
- Adjacent nodes must have different colors

### Allocating to k registers $\equiv$ finding a k-coloring of the interference graph

- Adjacent nodes must be allocated to distinct registers

#### But...

- Optimal graph coloring is NP-complete
  - Register allocation is NP-complete, too (must approximate)
- What if we can't *k*-color a graph? (must **spill**)

CIS 570 Lecture 18

Register Allocation

12

### **Spilling**

### If we can't find a k-coloring of the interference graph

- Spill variables (nodes) to stack until the graph is colorable

### Choosing variables to spill

- Choose least frequently accessed variables
- Break ties by choosing nodes with the most conflicts in the interference graph
- Yes, these are heuristics!

CIS 570 Lecture 18 Register Allocation 13

# **Weighted Interference Graph**

#### Goal

```
- Weight(s) = \sum_{\text{V references } r \text{ of } s} f(r) \text{ is execution frequency of } r
```

# Static approximation

- Use some reasonable scheme to rank variables
- One possibility
  - Weight(s) = 1
  - Nodes after branch: 1/2 weight of branch
  - Nodes in loop: 10 × weight of nodes outside loop

CIS 570 Lecture 18 Register Allocation

14

# **Simple Greedy Algorithm for Register Allocation**

```
for each n \in N do { select n in increasing order of weight }

if n can be colored then
do it { reserve a register for n }

else

Remove n (and its edges) from graph { allocate n to stack (spill) }
```

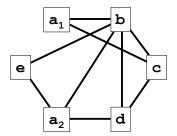
### Note

- Reserve 2-3 temp registers for manipulating data on stack

CIS 570 Lecture 18 Register Allocation 15

# **Example**

Attempt to 3-color this graph ( , , , ,



Weighted order:

a<sub>1</sub>
b
c
d
a<sub>2</sub>
e

What if you use a different weighting?

Problems with this approach?

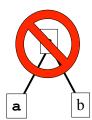
CIS 570 Lecture 18

Register Allocation

16

# **Example**

Attempt to 2-color this graph ( \_\_\_\_\_, \_\_\_)



Weighted order: a b

CIS 570 Lecture 18

Register Allocation

# **Improvement #1: Simplification Phase**

#### Idea

- Nodes with  $\leq k$  neighbors are guaranteed colorable

### Remove them from the graph first

- Reduces the degree of the remaining nodes

Must spill only when all remaining nodes have degree  $\geq k$ 

CIS 570 Lecture 18

Register Allocation

18

### Algorithm [Chaitin82]

```
while interference graph not empty do
    while \exists a node n with \leq k neighbors do
                                                 simplify
        Remove n from the graph
        Push n on a stack
   if any nodes remain in the graph then { blocked with >= k edges }
                                           { lowest spill-cost or }
        Pick a node n to spill
                                           { highest degree }
        Add n to spill set
        Remove n from the graph
if spill set not empty then
   Insert spill code for all spilled nodes { store after def; load before use }
    Reconstruct interference graph & start over
while stack not empty do
    Pop node n from stack
    Allocate n to a register
```

CIS 570 Lecture 18

Register Allocation

# **More on Spilling**

### Chaitin's algorithm restarts the whole process on spill

- Necessary, because spill code (loads/stores) uses registers
- Okay, because restarts usually only happen a couple times

### Alternative

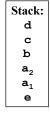
- Reserve 2-3 registers for spilling
- Don't need to start over
- But have fewer registers to work with

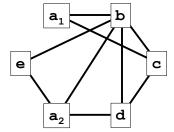
CIS 570 Lecture 18

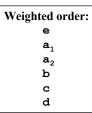
Register Allocation

20

# **Example**







How do we order the nodes here?

CIS 570 Lecture 18

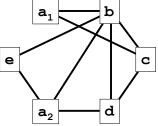
Register Allocation

# **Example**

Attempt to 2-color this graph ( \_\_\_\_\_, \_\_\_\_)









Many nodes remain uncolored even though we could clearly do better

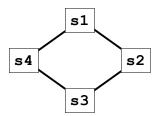
CIS 570 Lecture 18

Register Allocation

22

# **The Problem: Worst Case Assumptions**

Is the following graph 2-colorable?



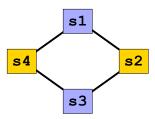
### Clearly 2-colorable

- -But Chaitin's algorithm leads to an immediate block and spill
- The algorithm assumes the worst case, namely, that all neighbors will be assigned a different color

CIS 570 Lecture 18

Register Allocation

# **Improvement #2: Optimistic Spilling**



#### Idea

- Some neighbors might get the same color
- So nodes with *k* neighbors **might** be colorable
- Blocking does not imply that spilling is necessary
  - Push blocked nodes on stack (rather than place in spill set)
  - Check colorability upon popping the stack, when more information is available

Defer decision

25

CIS 570 Lecture 18 Register Allocation 24

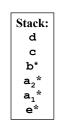
# Algorithm [Briggs et al. 89]

```
while interference graph not empty do
    while \exists a node n with \leq k neighbors do
                                                   simplify
         Remove n from the graph
         Push n on a stack
    if any nodes remain in the graph then
                                             \{ blocked with >= k edges \}
         Pick a node n to spill
                                              { lowest spill-cost/highest degree }
         Push n on stack
                                                    defer decision
         Remove n from the graph
while stack not empty do
    Pop node n from stack
    if n is colorable then
                                                    make decision
         Allocate n to a register
    else
         Insert spill code for n
                                              { Store after def; load before use }
         Reconstruct interference graph & start over
```

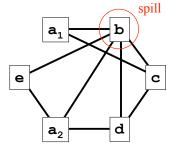
CIS 570 Lecture 18 Register Allocation

# **Example**

Attempt to 2-color this graph ( \_\_\_\_\_, \_\_\_\_)







Weighted order:

e
a<sub>1</sub>
a<sub>2</sub>
b
c
d

CIS 570 Lecture 18

Register Allocation

26

# Improvement #3: Live Range Splitting [Chow & Hennessy 84]

#### Idea

- Start with variables as our allocation unit
- When a variable can't be allocated, split it into multiple subranges for separate allocation
- Selective spilling: put some subranges in registers, some in memory
- Insert memory operations at boundaries

Why is this a good idea?

CIS 570 Lecture 18

Register Allocation

### **Improvement #4: Rematerialization**

#### Idea

- Selectively re-compute values rather than loading from memory
- "Reverse CSE"

#### Easy case

- Value that can be computed in single instruction, and
- All operands are available

### **Examples**

- Constants
- Addresses of global variables
- Addresses of local variables (on stack)

CIS 570 Lecture 18

Register Allocation

28

# **Coalescing**

#### **Move instructions**

- Code generation can produce unnecessary move instructions mov t1, t2
- If we can assign **t1** and **t2** to the same register, we can eliminate the move

#### Idea

 If t1 and t2 are not connected in the interference graph, coalesce them into a single variable

#### **Problem**

- Coalescing can increase the number of edges and make a graph uncolorable
- Limit coalescing to avoid uncolorable graphs coalesce

CIS 570 Lecture 18

Register Allocation

# **Next Time**

### Lecture

- More register allocation
  - Allocation across procedure calls

CIS 570 Lecture 18 Register Allocation