Memory Organization

Internal Memory: Internal memory in a computer is required for execution of a program. Internal memory is a form of semiconductor random access memory. There are two basic forms of semiconductor memories.

1. SRAM – static RAM
2. DRAM – Dynamic RAM.

SRAM is faster, more expensive and less dense than DRAM

SRAM is used for cache memory.
DRAM is used for main memory.

A cache or cache memory is an area of computer memory that is used for temporary storage of data and can be accessed more quickly than the main memory

Characteristics of memory system:

- **Storage Capacity**: It is a representative of the size of the memory. The size of internal memory can be expressed in terms of number of words or bytes.

- **Unit of Transfer**: Unit of transfer is defined as the number of bits read or written in a single read or write operation. For main memory and internal memory, the normal unit of transfer of information is equal to the word length of process

Infact it depends on number of data lines in the system bus.

- Access Modes: Memory is considered to consists of various memory locations. The information from memory devices can be accessed in the following ways.
  - Random access
  - sequential access
  - Direct access
  - Associative access.
- Access Time: The access time is the time required between the request made for operation (read or write) and the time the data is made available or written at the requested location. The access time depends on the physical characteristics and access mode used by the device.

- Permanence of storage: It is possible to lose information by the memories over a period of time. There could be several reasons for losing stored information.
These are dynamic storage, volatile, hardware failure, destructive readout.

There are some memories (DRAM) where the stored '1' loses its strength to become '0' over a period of time. This kind of memory requires refreshing.
The memories which require refreshing are known as dynamic memories.

The memories which do not require refreshing are called static memories

- Cycle Time: It is the minimum time elapsed between two consecutive read requests. It is normally equal to access time except the ones in which destructive readout is encountered or a refreshing cycle is needed prior to next read.

- Data Transfer Rate: The amount of information transferred per unit time is known as data transfer rate. It is measured in bits/second.
- Physical characteristics: A variety of physical types of memories are in use. The most common today are two
  Semiconductor memory using VLSI technology.
  Magnetic surface memory used for disk & tape

Several physical characteristics of data storage are important. In a volatile memory, information decays naturally or is lost when electrical power is switched off.

In a nonvolatile memory, information once recorded remains intact.

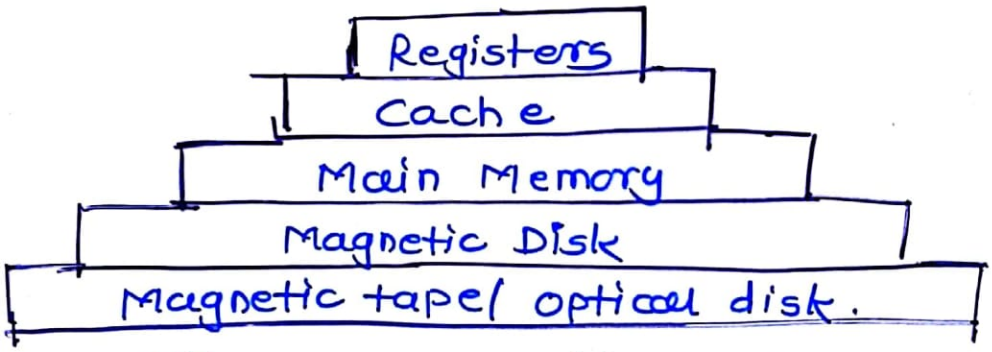
Magnetic surface memories are nonvolatile

Semiconductor memory may be either volatile or nonvolatile.

Characteristics of Memory

Type of memory	Access Mode	Permanence of storage	Physical nature of storage
Semiconductor memories	Random	Volatile	Electronic
• Magnetic disk	Direct	Non-volatile	Magnetic
• Magnetic tape	Sequential	Non- volatile	Magnetic
• Compact disk ROM	Direct	Non-volatile	Optical

Memory Hierarchy



The memory hierarchy.

Memory in computer is required for storage and subsequent retrieval of instructions or data. A memory system of a computer must be able to keep up with the CPU. That is as the CPU is executing instructions, it should not wait for the operands or instructions to be read from the memory. For practical system the cost of the memory must be reasonable

A memory system has three basic characteristics.

- Cost per bit
- Capacity
- Access time

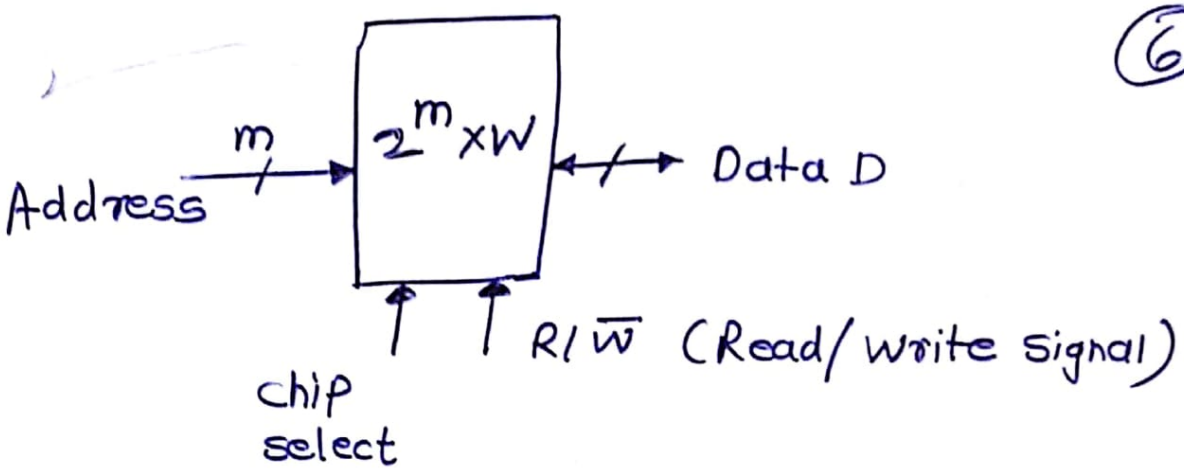
There found to be a trade-off among the three characteristics of memory. The following relationship hold:

- Smaller access time, greater cost per bit
- Greater capacity, smaller cost per bit
- Greater capacity, greater access time.

A typical memory hierarchy is as shown. As we move from top to bottom, the following occurs.

- Decreasing cost per bit
- Increasing capacity
- Increasing access time
- Decreasing frequency of access of the memory by the CPU

The memory hierarchy will work only if the frequency of access to slower memories is significantly less than the faster memories.



A RAM IC showing its major external connections

A typical RAM IC is shown in fig. A RAM IC contains all required access circuitry, including address decoders, drivers and control circuits.

- Fig shows a $2^m \times W$ bit RAM IC.
- m-bit address lines can be used to select a word
- There are 2^m words in RAM
- Each word is of W bits
- If R/$\overline{W}$ control line is 1 then the data stored at an address selected by address A is read
- If R/$\overline{W}$ control line is 0 then a new data is written at an address selected by address A.
- Data to be written is sent on data lines ($D_0 - D_{W-1}$)
- Select signal CS (chip select) is required to be active for any operation on RAM chip.

16K x 8 memory chips are used to construct 64K x 16 memory:

i) Find how many chips will be needed?

ii) Draw block diagram showing connections of chips to address lines.

Solution:

- Word size is being increased from 8 bits to 16 bits.
- Number of words being increased from 16K to 64K

∴ Number of chips required $= \frac{64K}{16K} \times \frac{16 \text{ bits}}{8 \text{ bits}}$

$= 8$ chips.

Number of address lines in system bus

$= \log_2 64K$

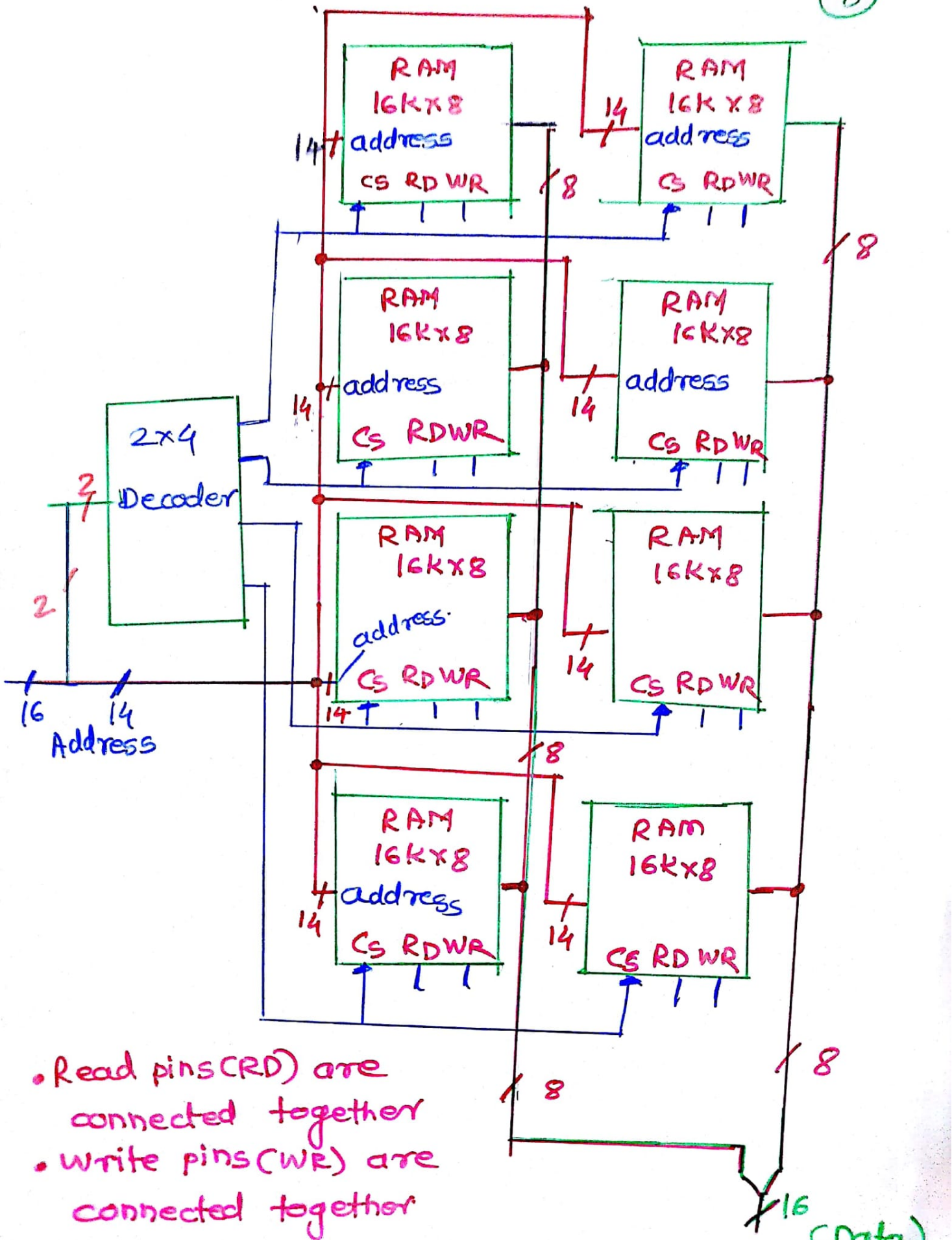
$= \log(2^6 \times 2^{10}) = 16$

Number of address lines required by 16K x 8 memory chip $= \log_2(16K)$

$= \log_2(2^4 \times 2^{10}) = 14$

Word size is of 16 bit so two memory chips will be required (each of 8 bits)

16 - 14 = 02, 02 lines are required for decoder (2 x 4 decoder)



- Read pins (RD) are connected together
- Write pins (WR) are connected together

How many 128 bytes RAM chips are required to provide a memory of 2048 bytes? Show the details of connections, clearly indicating address, data and decoder configuration. (9)

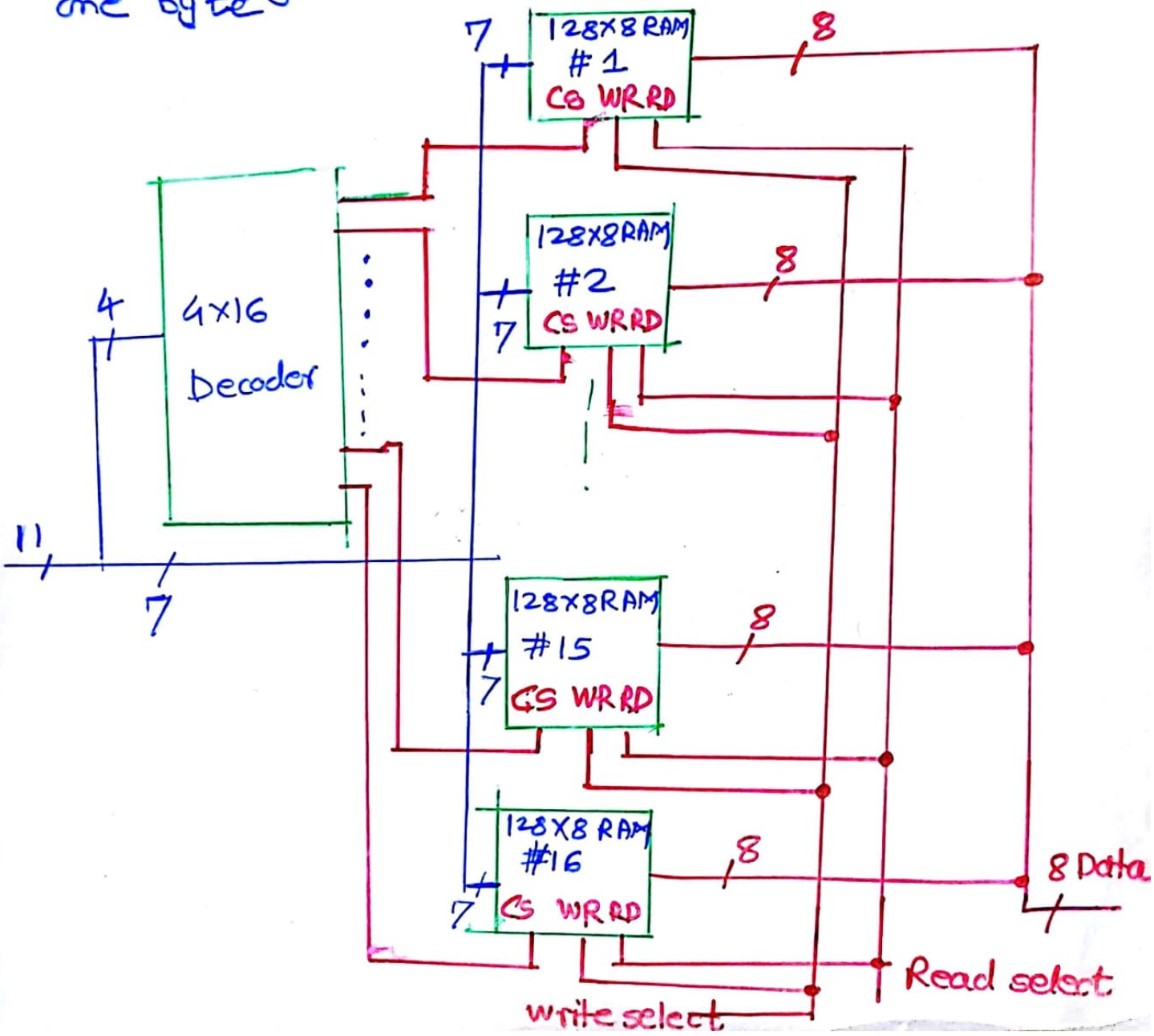
Solution:

Number of address lines in system bus = $\log_2 2048 = 11$

Number of address lines in chip = $\log_2 128 = 7$

Number of chips required = $\frac{2048}{128} = 16$

(Here wordsize of both the memory is same) one byte



Design a 4M x16 memory unit, using 256K x1 memory chips. Explain in detail assumptions made while designing the system.

Solution:

- Word size is increased from 1 bit to 16 bit, so such 16 chips will be required in a row
- Number of words is being increased from 256K to 4M
- Number of chips required = $\frac{4M}{256K} \times \frac{16 \text{ bits}}{1 \text{ bit}} = \frac{4 \times 2^{10} \times 2^{10} \times 16}{2^8 \times 2^{10} \times 1}$

  $= 16 \times 16 = 256$
- Number of address lines in system bus = $\log_2 4M$
- Number of address lines required in memory chip = $\log_2 \frac{256K}{1}$

  $= \log_2 (2^8 \times 2^{10})$

  $= 18$

  $= \log_2 (4 \times 2^{20})$

  $= 22$

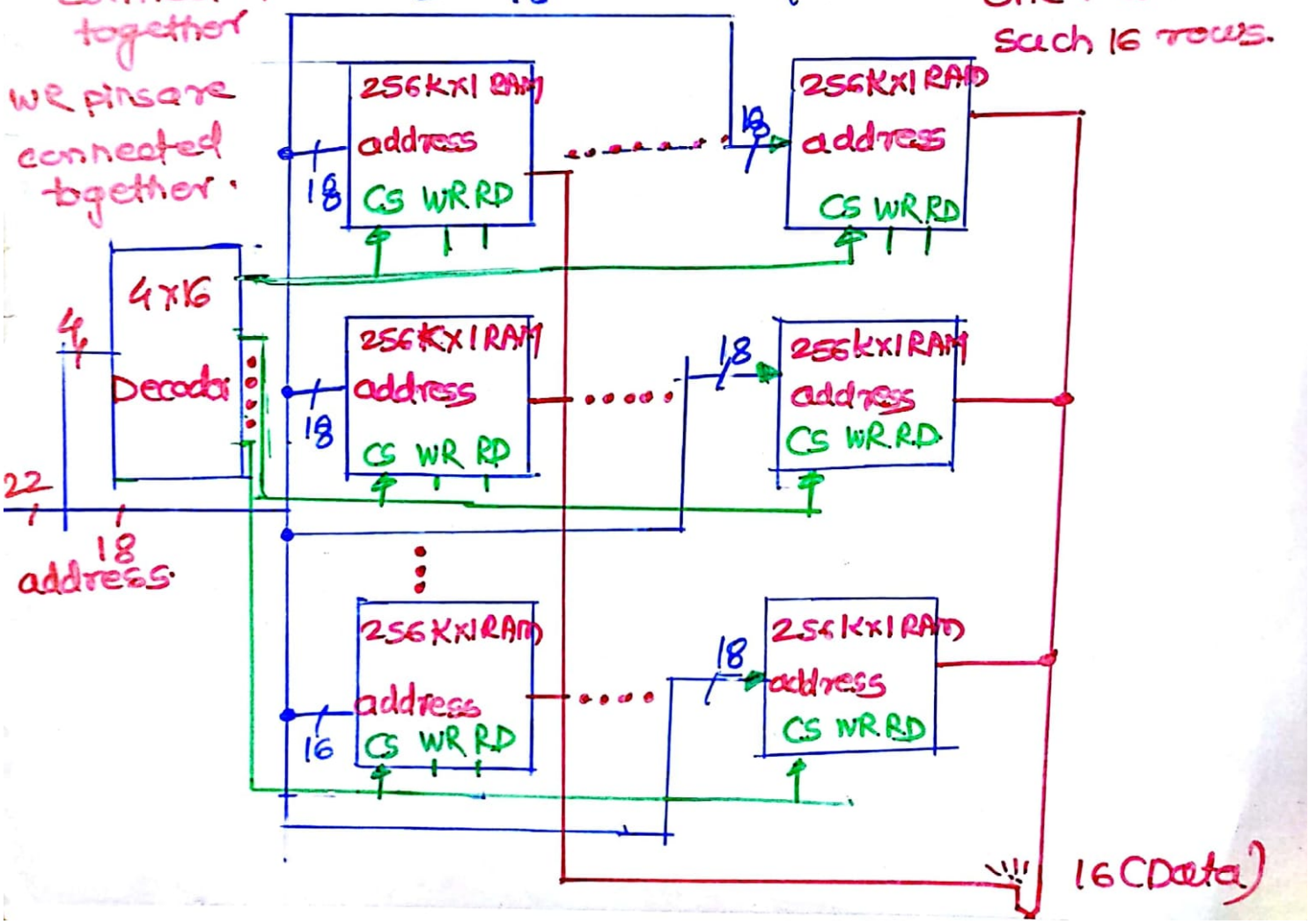
4 lines for decoder

RD pins are connected together

WR pins are connected together.

one row 16 chips

Such 16 rows.



A computer uses RAM chips of the 1024×1 capacity. How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes.

→ Word size is increased from 1 bit to byte.

8 memory chips of 1024×1 capacity are connected in a row as shown.

Number of address in system are 10