AMEY THAKUR SE-Comps B-50

Practice Test COA

Class: SE B - 50 Date: 04/05/2020 Time: 10 AM to 11AM

| 50 | Q1) Explain cache consistency and coherency with suitable examples .Also | |
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| | give methods to maintain cache consistency? | |
| | Q2) Explain programmed I/O and Interrupt Driven I/O | |
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| | Ans: Programme to be to |
| 3 | The Cache Coherence Problem |
| | - In a maltiprocessor system data inconsistency may occur |
| | among adjacent levels or within the same level of memory |
| 1.74 | hierarchy |
| | - For ex- the cache and the main memory may have inconsistent |
| | copies of the same object. |
| ī | - As multiple processor operate in parallel and independently |
| 1 | multiple caches may posses different copies of the same |
| | memory block this creates cache coherence problem |
| 10 | Cache coherence Schemes help to avoid this problem |
| | by maintaining a uniform state for each cached |
| 116 | block of data of an appear in mattible me will - |
| | 115 PRO 1200 120 1717 |
| | Processor 1 P. P. P2 P2 |
| | been it out they are not be to them |
| r i | caches x x x x x |
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| | I'd word tripper wave to shall egint on it |
| | Shared X |
| | memory |
| | Before write - Write - |
| | update through back |
| 77 | place person since one but sol in will - |
| | - Let x be an element of shared data which has been |
| 1 | referenced by 2 processors, P, 4 Pz. |
| | - In the beginning 3 copies of x are consistent. |
| | If the processor P, writer a new data X2 into |
| | the cache, by using write storough policy. |
| | The same copy will be written isomediately into |
| | the shared memory. |
| Trans. | |

| Name: | Amey Thakur | Class: | _Div: B Roll No: 50 | 0 |
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| Subject: | Topic: | _Date: | Page No: | _ |
| | cr inconsistency occur | ss between | cache memory | |
| | main memory. | | 57 A. J. | . |
| | write - back police | | | īΛ |
| | will be updated wh | | 34.11 | |
| - In gener | al there are 3 | Sources of | inconsistenty prol | b ler |
| | ring of writable d | | M Alexander | |
| | ocers wichation - | Pre- 7 0 | reino de la companya | |
| | 10 Activity | | * <u>**</u> ** * * * * * * * * * * * * * * * | |
| | ing cache cohere | | problem in a | |
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| _ | cache memory | ilia pertan | Alt I The | - 2 |
| Data | Pronsistency between | een differ | ent (aches easi) | y |
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| Ans: Interrupt Driver IO Theory Driver IO overcomes the disadvantage of programmed IO i.e. CPU waiting for IO derice This disadvantage is overcome by CPU not repeatedly checking for the device being recody or not instead the IO module interrupt when result The sequence of operation for interrupt driven TO OPU issues the read command to TO derice CPU close other work To module gets data from peripheral while CPU close other work Once the IO module completes the data hander from IO derice it interrupts CPU (4) On getting the interrupt CPU These CPU gets an interrupt it performs the peration of module to interrupt it performs the O save context is the content of the register on the stack Processes interrupt by executing the corresponding ISR Restore the register content from the stack All D module when Interrupt lines and is used All D module when Interrupt driven IO is used | |
|--|--|
| Interrupt Driven IO Tatestrupt Driven IO Overcomes the disadvantage of programmed IO. i.e. CPU waiting for IO derice. This disadvantage is overcome by CPU not repeatedly checkering for the device being ready or not instead the IO module interrupt when ready. The Sequence of operation for interrupt driven TO. ORU issues the read command to TO derice. DIO module gets data from peripheral while CPU close other work. Once the IO module completes the data hander from IO derice it interrupts CPU. (4) On getting the interrupt CPU requers data from TO module transfers the data to complete in peripheral while. These CPU gets an interrupt it performs the operations. Save context, i.e. the contents of the register on the stack. Processes interrupt by executing the corresponding ISR. (5) Restore the register contents from the stack. IC 8259 has 8 suterrupt lines, and is used. | 02 |
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| ① CPU issues the read command to 30 derice. ② IO module gets data from peripheral while CPU docs other work ③ Once the IO module completes the date hander from IO derice it interrupts CPU. ④ On getting the interrupt. CPU requests data from IO module transfers the date to copt. Theo CPU gets an interrupt it performs the a perations— ① Save context. I.e. the contexts of the register on the stack ② Processes interrupt by executing the corresponding ISR ③ Restore the register context from the stack — IC 8259 has 8 gaternapt lines. and is used | |
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| as IO module when Enterrupt driven To is used | - IC 8259 has 8 gaterrypt lines and is used |
| | as IO module when interrupt driven To is used |
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Amey Thakur

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| - Transferring a block of dat | ra using interrupt |
|-------------------------------|--|
| Oriven 70, | |
| | ** * * * * * * * * * * * * * * * * * * |
| Begin | · |
| CPU issues at read | |
| . Or write command to | CPV -> IO |
| IO device | |
| 1 | |
| IO module interms | |
| about its stare by | Io->epu. |
| Entersypting CPU. | e de la companya del companya de la companya del companya de la co |
| | |
| | |
| | > IO -> CPV |
| Feror | |
| Ready | 1 2.00 /00 |
| CPU reads a word from | |
| menory and writes it to | Memory -> CPU -> IO |
| clevice CPU reads | · |
| a word from ID device | ID -> CPU -> Memor |
| and writes it in memory | V |
| | / |
| Ta | |
| No semolères | |
| No complète l' | |
| Yes | |
| | |
| to Execute N | Jext waterworker |
| | |

| 8 |
|--|
| Programmed IO |
| |
| - In programmed IO method of interfacing, |
| CAN be direct control over 10 |
| - To Drucestor, Checks the status or the devices |
| and issues read write command and then |
| |
| During the data transfer. CPU waits for. |
| In module to complet operation |
| home this xystem waits the CAV time |
| - That's why Interrupt Driver -0 |
| Syperior than programmed ID- |
| |
| - In programmed IO sequence of operations to be |
| carried out |
| (i) CPV requests for 20 operation |
| (2) IO module performs the said operation |
| (3) IO module updates the status bits |
| La clatus bit begacheally |
| Neither the IO module cannot inform CPU |
| directly nor can in modula initial |
| (5) CPU may wait for operation to complete of |
| may continue the operation later |
| |
| the state of the s |
| |
| |
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| • |

| - Transferring a block of d | ata crossed brodsenmed 30 |
|--|--|
| Begin | the state of the s |
| | · · · · · · · · · · · · · · · · · · · |
| CPU ispues a read | |
| or white command to | CPU -> IO |
| To device | naula |
| | 1165 in |
| Read status of | 10 -> cpo |
| ID device | and the second of the |
| | |
| Not Ready | with . n |
| Status | |
| | OT THE PROPERTY AT THE |
| Ready | |
| Cipu reads a word from | 1 (1) |
| To denice and write it to | |
| memory or writer a word | memory 3cpv - 30 |
| to I'v device after reading | JO -> CPV -> Ma |
| it how memory | JO -> CPV -> Memor |
| - 7 | |
| de la companya dela companya dela companya dela companya de la com | |
| ĮĮ, | |
| No block franter | |
| Complete? | |
| | |
| - Yes | |
| Exection ment instruction | |