

21/03/2020
SATURDAY

Mumbai University

Terna Engineering College, Nerul, Navi Mumbai

Department of Computer Engineering

Course Code	CSC403	Program	B.E. (CMPN)
Semester	IV	Year	II
Name of the Faculty	Rohini Palve	Class / Div	A & B
Course Title	Computer Organization and Architecture	Academic year	2019-20

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ASSIGNMENT 3

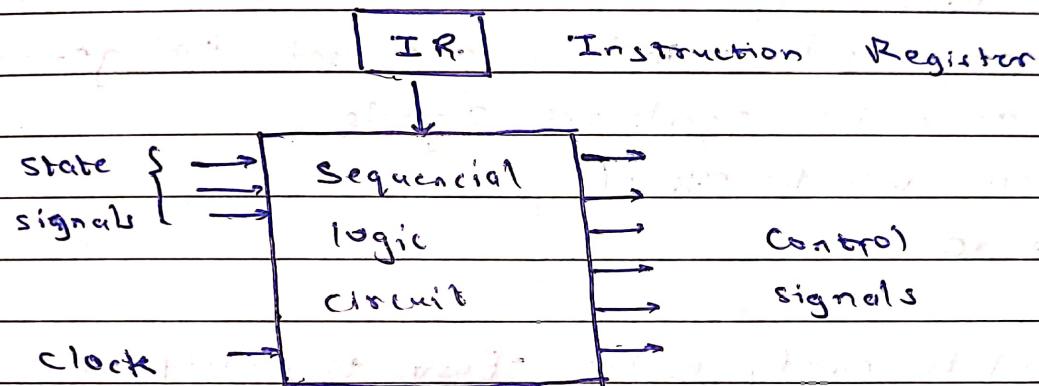
- Q1) Explain the hardwired control unit with neat diagram and specify its advantages.
Compare it with the microprogrammed control unit
- Q2) Explain different techniques for the design of a control unit of a computer.
- Q3) Write a short note on the performance measure.
- Q4) State the functions of the control unit. Explain the microprogrammed control unit.
- Q5) Explain microinstruction sequencing and execution
- Q6) Compare RISC and CISC processors.

(CO3): To describe instruction-level parallelism and hazards in typical processor pipelines and study control unit design

Q.1:

Ans:

- The hardwired control unit is implemented as a sequential logic circuit or a finite state machine that generates a specific sequence of control signals to execute an instruction.
- Structure of an hardwired control unit



- Hardwired control unit uses a fixed logic to interpret an instruction and generate appropriate control signals. While designing a control unit we have to consider various factors like
 - Amount of hardware used
 - Speed of operation
 - Cost of design

Advantages of hardwired control unit are

- ① It is faster than micro programmed unit
- ② It can be optimized to produce fast mode of operation

Hardwired control Unit

- It generates the control signals needed for the processor using logic circuits

- Faster when compared microprogrammed control unit as control signals are generated with the help of hardware

- Difficult to modify as the control signals that need to be generated are hardwired

- More costlier as everything has to be realized in terms of logic gates

- Used in computer that makes use of reduced instruction set computers (RISC)

Microprogrammed Control Unit

- Generates the control signal with the help of micro instruction stored in control memory

- Slower as micro instructions are used for generating signals.

- Easy to modify as the modification need to be done only at instruction level.

- Less costlier than hardwired control as microinstructions are used for generating signals.

- Used in computer that makes use of complex instruction set of computers (CISC)

Q.2.

Ans:

- There are 4 techniques to design hardwired:

(1) State Table method

- It is a classical method of sequential circuit design
- It attempts to minimize the amount of hardware

(2) Delay Element method

- It is a method based on the use of clocked delay element for control signals timings

(3) Sequential Counter method

- It uses counter for timing purposes.

(4) PLA Method

- It uses programming logic.

(1) State Table method

- Starts with the construction of state transition table.
- In every state, the control unit generates a set of control signals
- This state table is then implemented using flip flops and combinational circuits to generate different control signals.
- Example:-

Inputs

state	I_1	I_2	I_m	
S_1	$s_{1,1}, o_{1,1}$	$s_{1,1}, o_{1,2}$		$s_{1,m}, o_{1,m}$	
S_2	$s_{2,1}, o_{2,1}$	$s_{2,2}, o_{2,2}$		$s_{2,m}, o_{2,m}$	
:	:	:			
S_n	$s_{n,1}, o_{n,1}$	$s_{n,2}, o_{n,2}$			

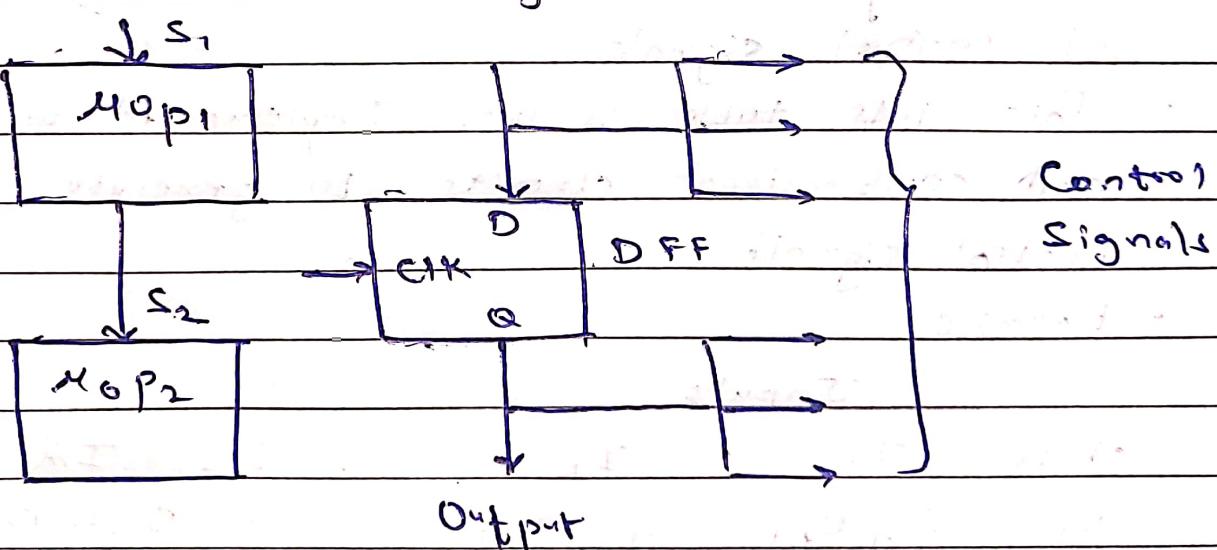
meale's
Table

Inputs

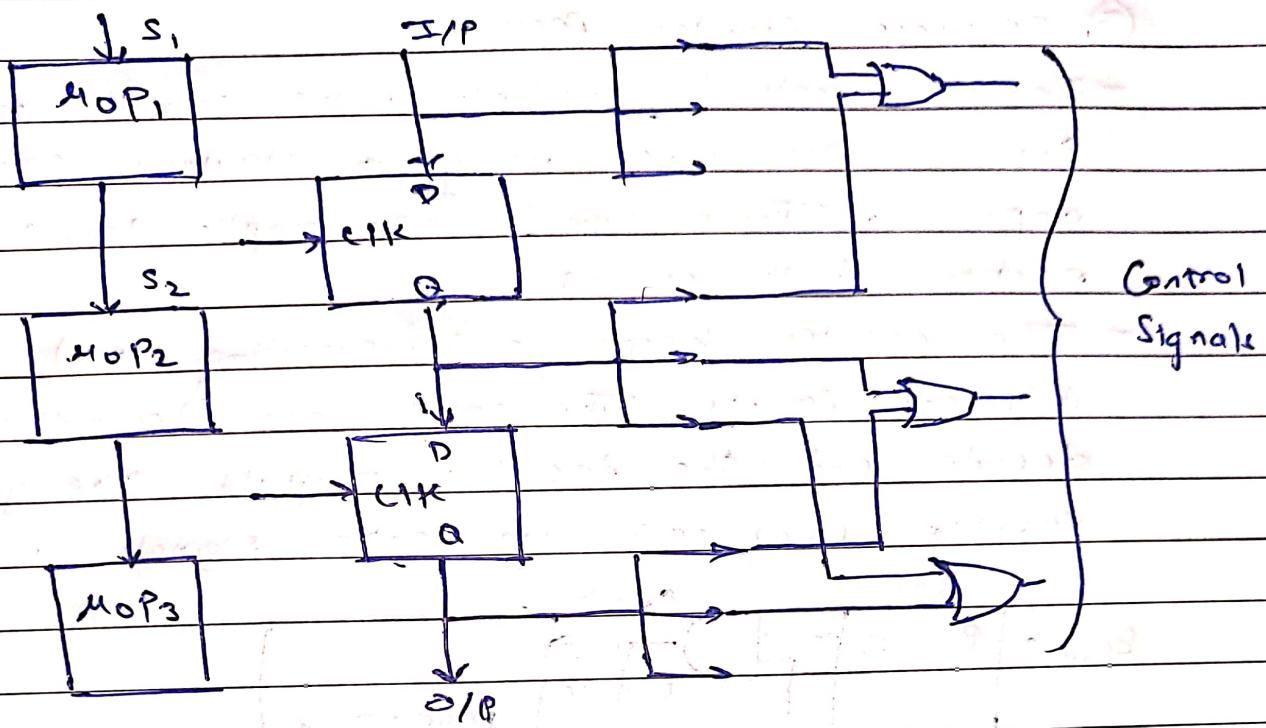
State	I_1	I_2	I_m	Output
S_1	$S_{1,1}$	$S_{1,2}$		$S_{1,m}$	O_1
S_2	$S_{2,1}$	$S_{2,2}$		$S_{2,m}$	O_2
\vdots	\vdots	\vdots		\vdots	Moore's Table
S_n	$S_{n,1}$	$S_{n,2}$		$S_{n,m}$	O_n

② Delay element method

- This method is implemented using delay elements, i.e. D-flip flops.
- The control sequence are activated in proper sequence. There is a specific delay time between activation of two groups of consecutive control signals. A sequence of delay elements can be used to generate control signals one after the other.
- To ensure synchronous operation, delay elements are implemented by D-flip flops and controlled by a common clock signal.

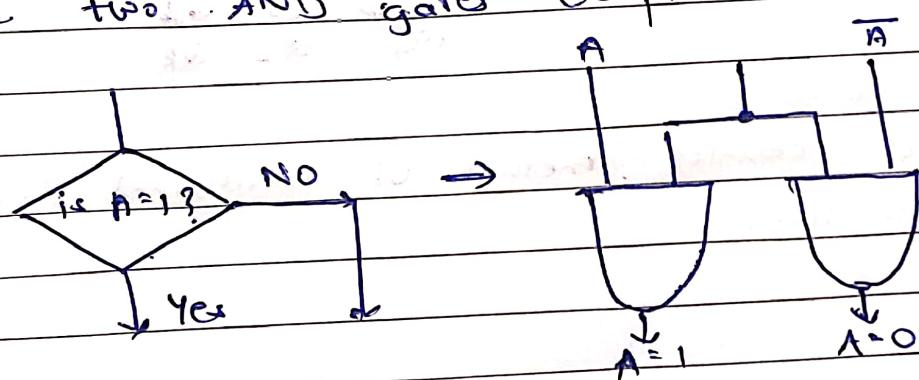


Use of D flip-flops as a delay element between two sets of control signals



Use of OR gate in delay element method of Hardwired Control Unit.

- The signals that activate the same control signal are ORed together. i.e. If signals has to be activated from outputs of multiple flipflops then an OR gate is used
- In case, if a decision is to be made then it is implemented using an If-then-Else circuit. we two AND gates coupled to a OR gate.



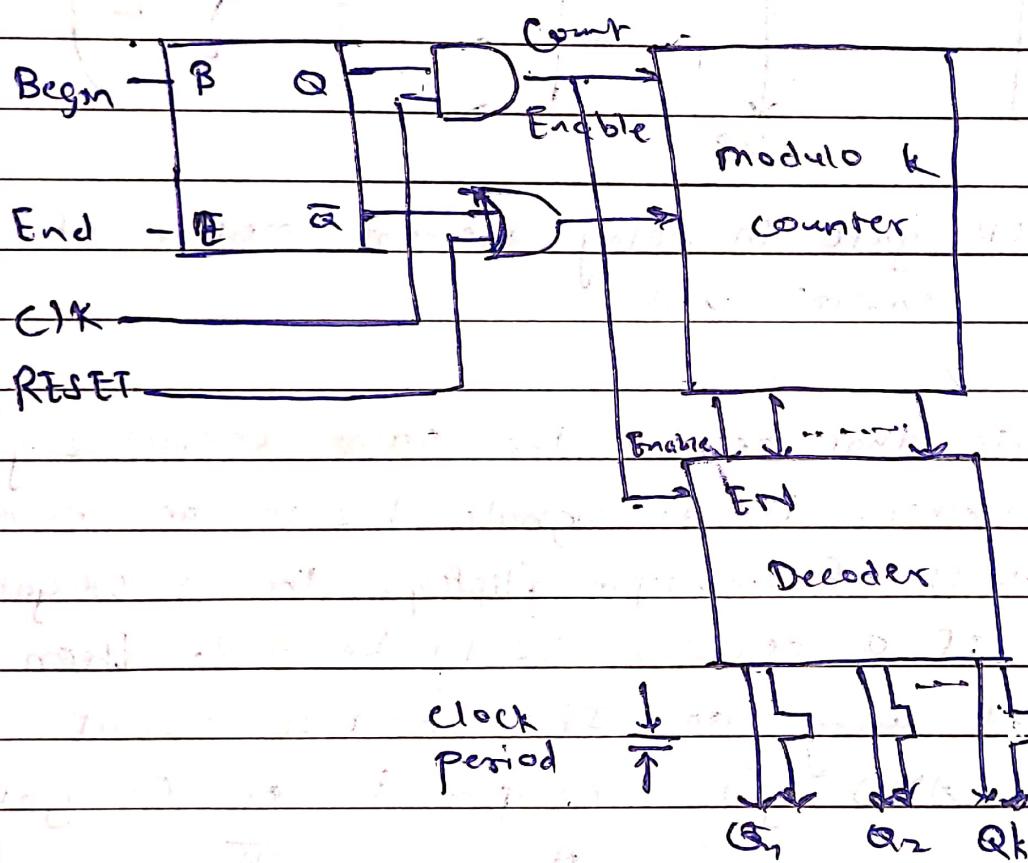
Implementation of If-then-else in delay element method of hardwired unit

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③ Sequence Counter Method

- In this method, multiple clock signals are derived from master clock using a standard counter decoder approach. These signals are applied to combinational portion of the circuit.
- The counter keeps on incrementing and generating different counts. The counts are decoded using a decoder and the decoder outputs are given to various components as control signals in the CPU.



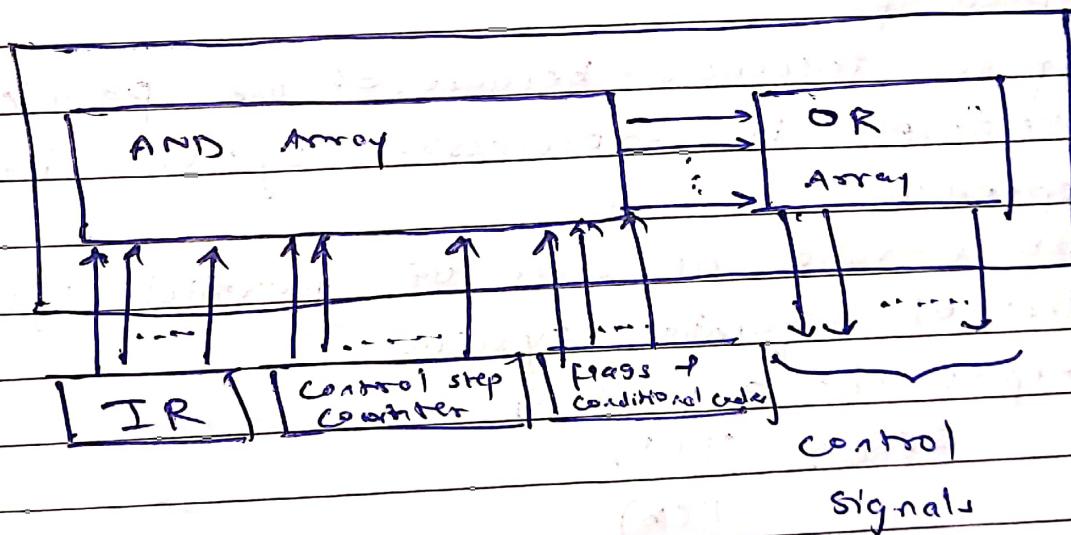
Sequential counter method of hardwired control unit implementation.

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④ PLA method

- In this method a PLA (Programmed Logic Array) is used to generate the controls signals. PLA is an array of AND gates at input and OR gate at output.
- The inputs are to be given to the AND gates which can be connected to the specific OR gates as required.
- The OR gates outputs are the outputs of the overall PLA and are used as control signals in the system - i.e. The inputs to the AND array is from various control signals generated and the output of the OR array is given as control signals to various components of the processor as well as the external control signals required.



Q3.

Ans:

- These are the various parameters that are used to measure the performance of system

(1) Sequential Execution Time:

- It is represented by $T(1)$
- It is the time required by program to be executed sequentially

(2) Parallel Execution Time:

- It is time required for a program to be executed on an n-parallel processor
- System is called as parallel execution time for n-number of processor
- It is represented by $T(n)$
where n, is no. of processor

(3) Speed up

- Speed increases because of the parallel system compared to uniprocessor system it is called as speed up
- It is ratio of speed of parallel system to that of sequential system
- Represented as $s(n)$

$$s(n) = \frac{T(1)}{T(n)}$$

(4) Efficiency

- It is ratio of actual speed up obtained by a system to the ideal speed up that should be achieved according to no of processor in parallel system

- Ideal time required should be $T(1)/n$

$$n \text{ of } E(n) = \frac{\text{Actual speed up}}{\text{Ideal speed up}} = \frac{T(1)}{T(n)}$$

(5) Throughput:

- It is defined as no. of programs executed per unit of time
 - Represented as WS
- $$WS = \frac{\text{No. of programs}}{\text{Time in second}}$$

Q4.

Ans:

Functions of Control Unit.

- It coordinates the sequence of data movements into, out of and between a processor's many sub units
- It interprets instructions.
- It controls data flow inside the processor
- It receives external instruction or commands to which it converts to sequence of control signals
- It controls many execution units i.e. ALU, data buffers and registers contained within CPU.
- It also handles multiple tasks such as fetching, decoding, executing, handling and storing result.

Micro programmed Control Unit.

- It is implemented using programming approach. A sequence of micro operations are carried out by executing a program consisting of micro instructions.
- Micro program consisting of microinstruction is stored in the control memory of control unit.
- Execution of a micro instruction is responsible for generation of a set of control signals.
- Micro instruction can cause execution of one or more operation and sequence of micro instruction can cause execution of an instruction.

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Memory address	Control field	Address field
1 0000	c ₀ c ₁ c ₂ c ₃ c ₄ c ₅ c ₆ c ₇ c ₈ c ₉ c ₁₀ 0001	0001
2 0001	1 0 0 1 1 1 0 0 1 0 1 0	0010
3 0010	1 1 0 0 0 1 1 0 0 1 0	0011

micro program

A micro instruction consist of

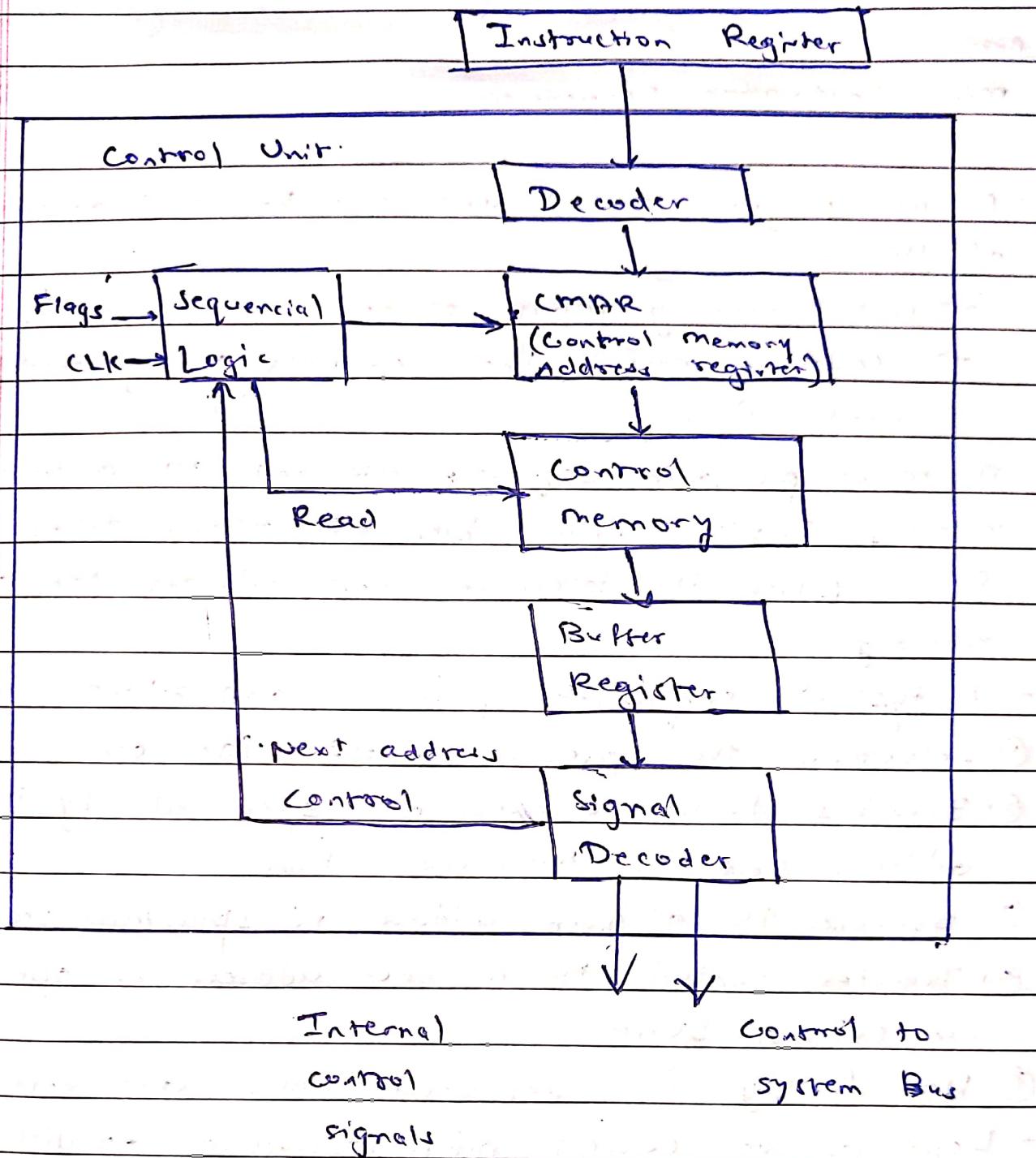
- One or more micro operation to be executed
- Address of the next micro instruction to be executed.

Advantages:

- Micro program can be changed relatively easily therefore it is flexible in comparison to hardwired control unit.

Disadvantages:

- Slower than hardwired control unit because the micro instructions are to be fetched from control memory which is time consuming



Functioning of microprogrammed control unit.

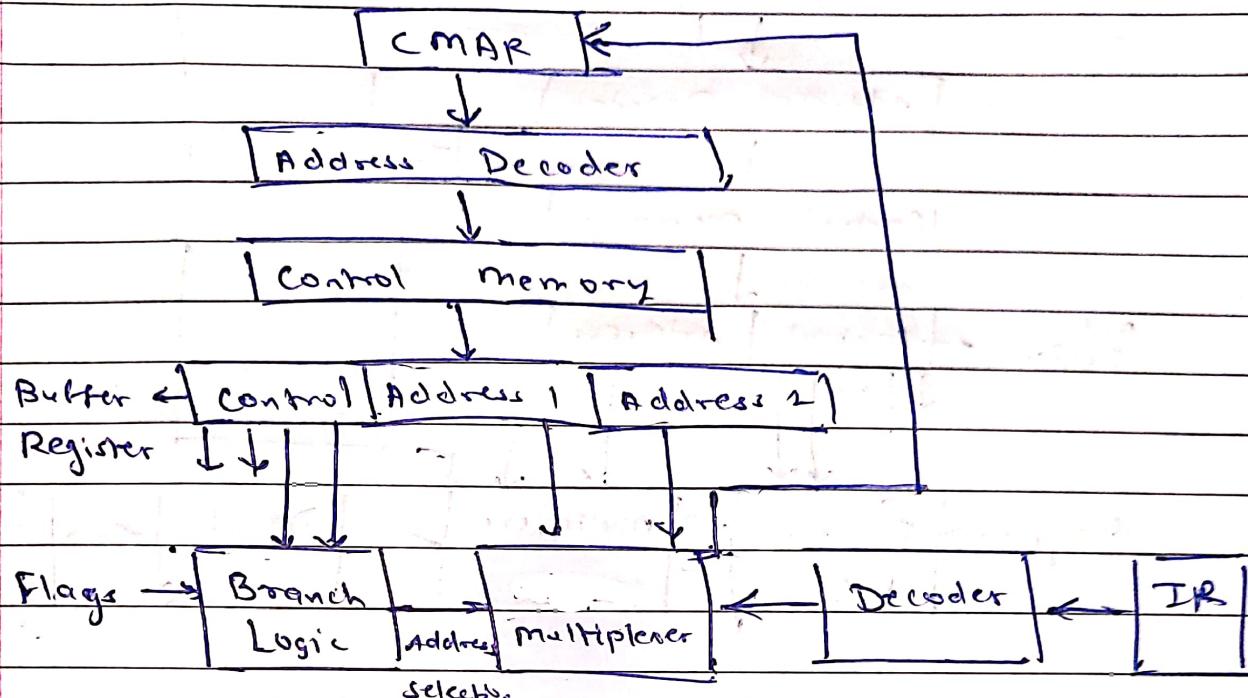
Q5.

Ans:

Micro Instruction Sequencing

- A micro program control unit can be viewed as consisting of two parts
 - Control memory which stores micro instructions
 - Sequencing circuit that controls the generation of next address.
- A micro program sequencer attached to a control memory inputs certain bits of micro instruction from which it determines next address for control memory
- A typical sequencer provides capabilities like
 - ① Increment the present address for control memory
 - ② Branches to an address as specified by the address field of micro instruction
 - ③ Branches to a given address if specified status bit = 1.
 - ④ Transfer control to a new address as specified by an external source
 - ⑤ Has facility for subroutine calls and returns
- Depending on current micro instruction condition flags and contents of instruction register, a control memory address must be generated for next micro instruction
- There are 3 general techniques based on format of the address information in micro instruction
 - ① Two Address Field
 - ② Single Address Field
 - ③ Variable Format

① Two address field



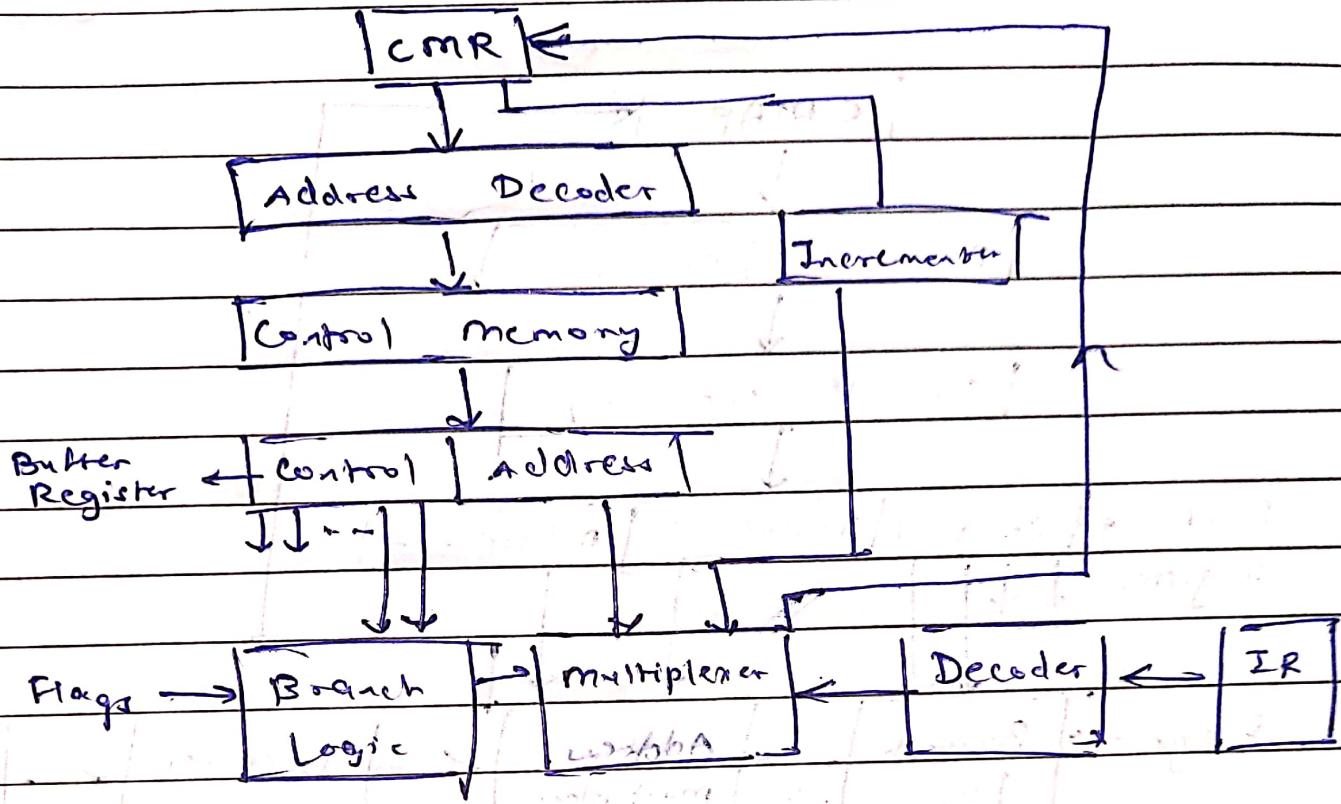
- The simplest approach is to provide 2 address fields in each micro instruction and multiplexer is provided to select
 - Address from second address field
 - Starting address based on the OP code field in current instruction
- The address selection signals are provided by a branch logic module where input consists of control unit flags plus bits from control partition of microinstruction

② Single address field

- Two address approach is simple but requires more bit in micro instruction
- With simpler approach, we can have single address field in micro instruction with options of next address
 - Address field
 - Based on OP code in IR
 - Next sequential Address

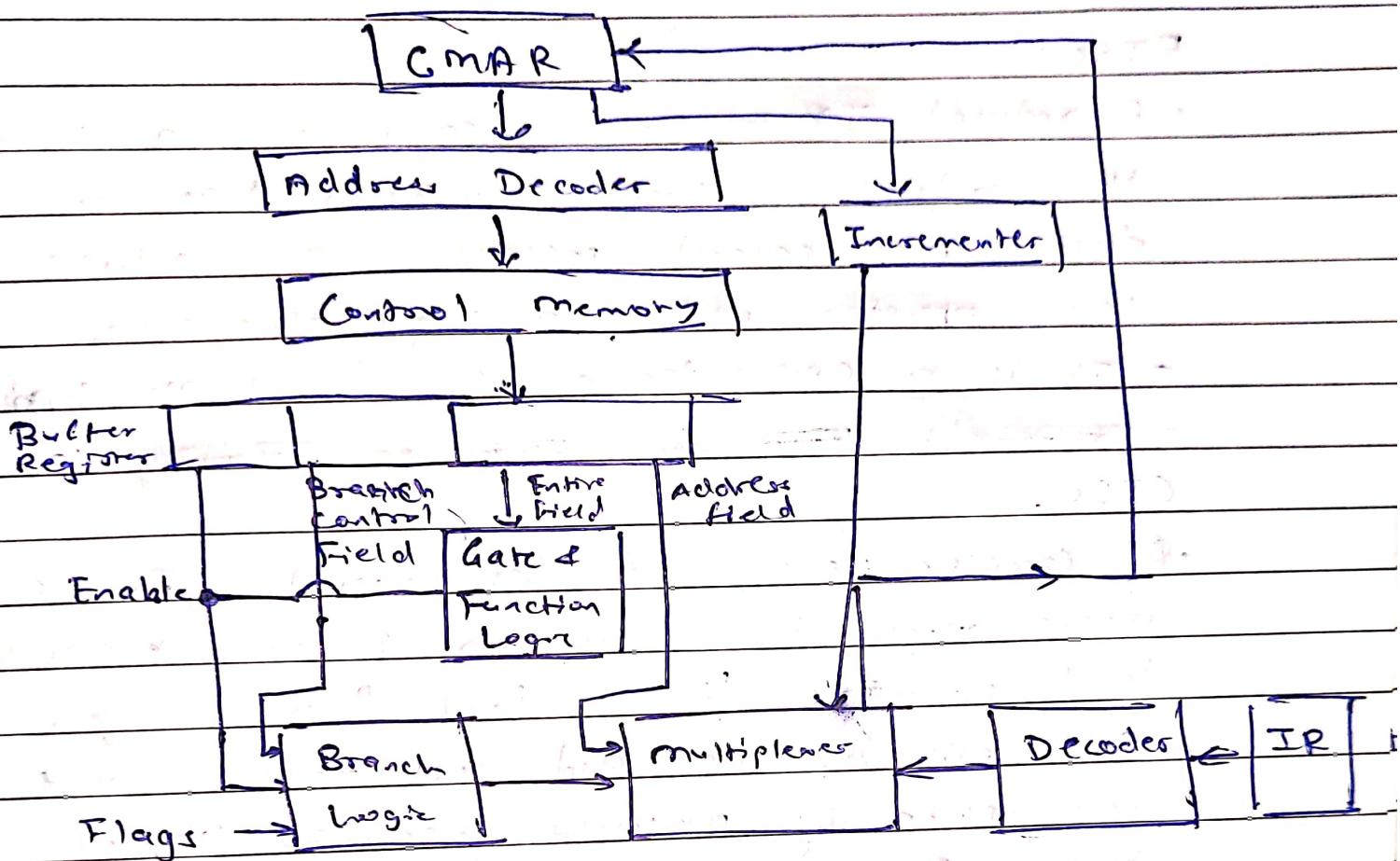
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- The address selection signals determine which option is selected. This approach reduces the no. of address field to one
- In most cases, the address field will not be used. Thus the microinstruction encoding does not efficiently utilize the entire micro instruction

③ Variable Format



In this approach, there are 2 entirely different microinstruction Format.

- One bit designated which format is being used. In the first format, the remaining bits are used to activate control signals. In the second format, some bits drive the branch logic module and the remaining bits provide the address. With the first format, the next address is either the next sequential address or an address derived from IR. With second format, either a conditional or unconditional branch, is specified.

Q.6.

Ans:

RISC:

- A reduced instruction set computer is a computer that only uses simple commands that can be divided into several instructions that achieve low level operation within a single clock cycle.
- It is a CPU design plan based on ~~single~~ ~~one~~ ~~step~~ ~~in~~ ~~executing~~ each inst.

CISC:

- A complex instruction set computer is a computer where single instructions can perform numerous low level operation like a load from memory, an arithmetic operation and an memory store are accomplished by multi-step processes or addressing modes in single instruction.
- It is a CPU design plan based on single commands which are skilled in executing multi-step operation.

RISC

CISC

① Reduced Instruction Set Computer

① Complex Instruction Set Computer

② It has single instruction taking about one clock cycle

② It has complex instruction that take up multiple clock for execution

③ Performance is optimized with more focus on software

③ Performance is optimized with more focus on hardware

- | | |
|---|--|
| (4) It has no memory unit and uses different hardware to implement instruction | (4) It has a memory unit to implement complex instructions |
| (5) It has a hardwired unit of programming | (5) It has a microprogramming unit. |
| (6) Instruction set is reduced. i.e. It has only few instructions in instruction set. | (6) Instruction set has a variety of different instructions that can be used for complex operation |
| (7) It can be used for complex operation | (7) It can be used to represent high level programming language statements |
| (8) Processors are highly pipelined | (8) Normally not pipelined or less |
| (9) Less execution time | (9) High Execution time |
| (10) Applications <ul style="list-style-type: none">- Video processing- Telecommunication- Image Processing | (10) Application <ul style="list-style-type: none">- Security system- Home Automation |