



VHDL

CH:10

VHDL

Q. short note on VHDL (Dec 14, May 15, May 16 7M)

- ↳ The long form of VHDL is very High speed integrated circuit (VHSIC) hardware description language.
- ↳ VHDL is hardware description language used to form digital system at many level of ideas ranging from the algorithmic to the gate level.
- ↳ VHDL language define the syntax as well as simulation semantics for each language. It is strong typed language which frequently contains too many words to write.
- ↳ VHDL is an official IEEE standard which will become the industry standard language for explaining digital circuits.
- ↳ The original standard for VHDL called IEEE 1076 was accepted in 1987.

* features of VHDL

1. Concurrency: VHDL is current language which execute statement simultaneous in parallel.
2. Supports sequential Statement:
VHDL can execute one statement at a time in sequence only.
3. Strongly typed languages:
only LHS and RHS operators of same type are allowed in VHDL.



3. Support hierarchies:
using VHDL hierarchy can be represented.
eg full adder, in this case it is composed of
half adder and OR gate.

Q. Structure of VHDL / VHDL Design units.
• (D-16 8M)

→ ↳ Design units of VHDL code are independent components which are separately compiled and stored in library.

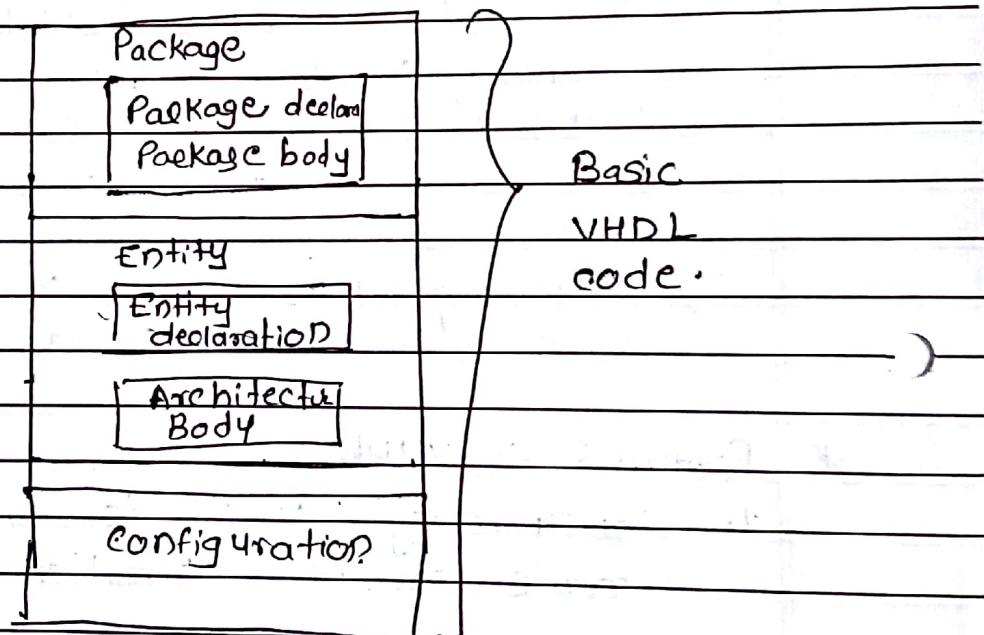


Fig: Design units of VHDL code.

↳ Design

VHDL program is composed following units

1) Package,

2) Entity

3) Architecture

4) Configuration.

1] Package :

- ↳ A VHDL Package is method to store and share some declaration which are common across many design units.
- ↳ Package is optional design unit. A set of declarations included in a package declaration can be shared by many design units.

2] Entity :

- ↳ The basic unit of VHDL hardware design is entity. The entity describes the interface between design and external environment.
- ↳ An entity is represented by using an entity declaration and associated architecture body.
- ↳ An entity described input and output ports of design.

3] Architecture Body

- ↳ An architecture describe the internal organization or entity operation and it include the statement which are used to model the entity behaviour.
- ↳ Architecture body is used to explain internal details of design entity using any one of the following modelling styles:
 - a) structural style.
 - b) Dataflow style.
 - c) Behavioral style.
 - d) Mixed style.



4] Configuration Declaration :

- ↳ The configuration statement denotes the binding bet'n entity and architecture. It is used to select any one input of architecture from multiple architecture bodies and binds it to corresponding entity.
- ↳ In VHDL design configuration allows you to change bet'n different architecture for entity.
- ↳ In a VHDL Design configuration statement is optional.
- ↳ Multiple configuration may available in an entity.

* Modeling Styles in VHDL

- 1] Structural modeling
- 2] Dataflow modeling
- 3] Behavioral Modeling
- 4] Mixed Modeling

* Comparison of modeling styles

Dataflow	structural	Behavioral
1. Dataflow modeling Style shows that how data/signal flows from ilp to alp through the registers/Components.	1. structural modeling style shows the graphical representation of component with their interconnect	1. Behavioral modeling style shows how our system performs according to current ilp values
2. Works on concurrent execn	2. Works on concurrent execn	2. Works on sequential execn.
3. for design specification, Boolean eq'n are needed.	3. for design specification, logic diagram is needed.	3. for design specification, truth table is needed.
4. Level of abstraction is gate	Level of abstraction is RTL (Register Transistor Logic)	Level of abstraction is gate

* VHDL Statement

- ↳ Sequential Statement.
- ↳ Concurrent Statement

Statements

- ↳ Sequential statements execute in sequential manner.
- ↳ The behaviour of sequential and concurrent statement is identical.
- ↳ In an architecture body, if statement appears outside a process, it is concurrent statement whereas if statement appears inside statement Process it is sequential statement

* Comparison b/w concurrent and sequential Statement.

concurrent statement

- 1) In this order of execution is not important.
- 2) It can appear anywhere in the architecture body.
- 3) Example of concurrent Statement is process, Concurrent signal assignment, block etc.

sequential state

- 1) In this order of execution is important as they appear within process.
- 2) It must be in process.
- 3) Example of sequential Statement is for, case, if etc.

*

Advantage of VHDL

- 1] For design and simulation only one language ie VHDL can be used.
- 2] VHDL allows user to pick any synthesis tool.
- 3] VHDL is multipurpose i.e once calculation block is created it can be used in many other project.

*

Application of VHDL :

- 1] It is used in electronic design automation to describe mix signal system such as FPGA (Field Programmable Gate Arrays) & integrated circuits.
- 2] VHDL can be used as general purpose parallel programming language.

Octal Addition

$$(634)_8 + (152)_8$$

$$\begin{array}{r}
 6 \ 3 \ 4 \\
 1 \ 5 \ 2 \\
 \hline
 8 \ 8 \ 6 \\
 -8 -8 \\
 \hline
 1 \ 0 \ 0 \ 6 \\
 = 1006
 \end{array}$$

(2)

$$\begin{array}{r}
 3 \ 5 \ 4 \\
 2 \ 6 \ 8 \\
 1 \ 2 \ 3 \\
 \hline
 1
 \end{array}$$

$$14 \ 13$$

$$-8$$

$$-8$$

$$(7 \ 6 \ 5)_8$$



Method :

Direct Subtraction

$$\begin{array}{r} (75)_8 - (68)_8 \\ \hline = \quad \quad \quad \end{array}$$

8 8 8 13
7 5 8
6 8
1

0 5

(2) 6 5 3

$$\begin{array}{r} - \quad 1 \quad 7 \quad 7 \\ \hline \quad 1 \\ \hline 4 \quad 5 \quad 04 \end{array}$$

using 7's complement

- 1] obtain 7's complement of number to be subtracted.
- 2] Add first num and 7's complement of num to be subtracted.
- 3] if carry is produced then add it to sum obtained in (2). The result will be in true form.
- 4] if carry is not produced then it is negative so take in 7's comp form



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①

$$(536)_8 - (345)_8$$

$$\begin{array}{r} 7 & 7 & 7 \\ 3 & 4 & 5 \\ \hline 4 & 3 & 2 \end{array}$$

$$\begin{array}{r} 5 & 3 & 6 \\ 4 & 3 & 2 \\ \hline 9 & 8 \end{array}$$

$$\begin{array}{r} & & 8 \\ & 1 & 1 & 7 & 0 \\ \hookrightarrow & & 1 & 1 & 1 \\ \hline & 1 & 7 & 1 \end{array}$$

②

$$161 - 243$$

$$\begin{array}{r} 7 & 7 & 7 \\ - 2 & 4 & 3 \\ \hline 5 & 3 & 4 \\ + 1 & 6 & 1 \\ \hline 9 & 5 \\ 1 & -8 & 1 \\ \boxed{0} & 7 & 1 & 5 \end{array}$$

Negative Result:

$$\begin{array}{r} 7 & 7 & 7 \\ - 7 & 1 & 5 \\ \hline 0 & 6 & 2 \end{array}$$



Hexadecimal addition

$$(C2) + (3E)$$

$$\begin{array}{r} C \quad 2 \\ + \quad 3 \quad E \\ \hline 1 \quad 1G \quad 1G \\ -1G \quad -1G \\ \hline 1 \quad 6 \quad 0 \end{array}$$

(2)

$$\begin{array}{r} D \quad D \quad C \quad C \\ B \quad B \quad A \quad A \\ \hline 13 & 13 & 12 & 12 \\ 11 & 11 & 10 & 10 \\ \hline 1 & 1 & 1 \\ 25 & 25 & 23 & 22 \\ 16 & 16 & 16 & -16 \\ \hline 1 & 9 & 9 & 7 \\ & & & 6 \end{array}$$

* Hexadecimal subtraction

$$(73 - 1C)_{16} = \begin{array}{r} 16 \\ 3 \\ \hline 1 \\ c \\ \hline 5 \end{array} \begin{array}{r} 7 \\ 12 \\ \hline 7 \end{array}$$

(A65) - (777)

$$\begin{array}{r}
 & 16 & 16 & 21 \\
 A & 6 & 5 & \} \\
 7 & 7 & 7 \\
 \hline
 2 & 14 & 14 \\
 \text{SEE) } & 16
 \end{array}$$

using 15's Complement

DAD - 426

$$\begin{array}{r}
 15 & 19 & 15 \\
 4 & 2 & 6 \\
 B & D & 9 \\
 \hline
 7 & B
 \end{array}$$

$$\begin{array}{r}
 B & D & 9 \\
 D & 8 & A \cdot C102 \\
 \hline
 1 & 1
 \end{array}$$

$$\begin{array}{r}
 25 & 22 & 19 \\
 -16 & -16 & -16 \\
 \hline
 \end{array}$$

$$\begin{array}{r}
 1 & 9 & 6 & 3 \\
 \hline
 9 & 6 & 4
 \end{array}$$



H.W

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Solve without converting base.

$$\textcircled{1} (BC5)_H - (A2B)_H$$

$$\textcircled{2} (210.2)_4 + (312.2)_4$$

Perform Hexadecimal of

$$DADA + BABA.$$

Gray code.

Q> Short note on Gray code - Dec 2, 4M

What are gray code - Dec-3, M-07.

Short note - May 15

↪ Gray code is another non weighted code
It is not an arithmetic code.

↪ It has very special feature that only one bit in gray code will change, each time decimal num is incremented as shown in table.

As only one bit changes at a time,
the gray code is called unit distance code.
The Gray code is cyclic code.

Decimal	Binary	Gray	?
0	0000	0 0 0 0	only
1	0001	0 0 0 1	encircled
2	0010	0 0 1 1	bit changes
3	0011	0 0 1 0	when decimal
4	0100	0 1 0 0	no is incre
5	0101	0 1 0 1	by one.
6	0110	0 1 1 0	
7	0111	0 1 1 1	

↪ Gray code also exhibits reflective property.

Application of Gray Code:

↪ Gray Code is popularly used in shaft position encoder.

↪ A shaft position encoder produces a code word which represent the angular position of shaft.

↪ Shaft encoder consist of light source, optical disc, light detectors, fig 1

↪ Patterns of opaque and transparent segments is etched out on optical disc.

So corresponding the black portion, the photodetector produces '1' and corresponding to transparent portion '0' is produced.

↪ fig 2 shows pattern for binary code and fig 3 shows pattern for gray code.

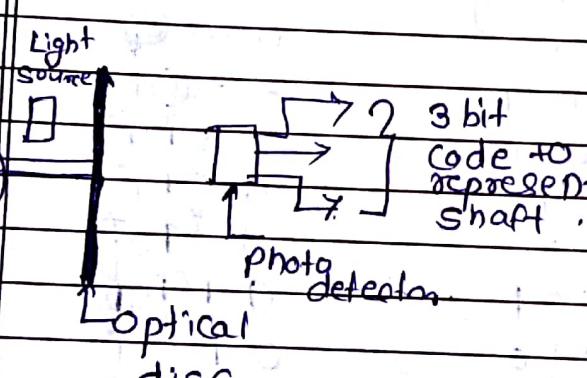
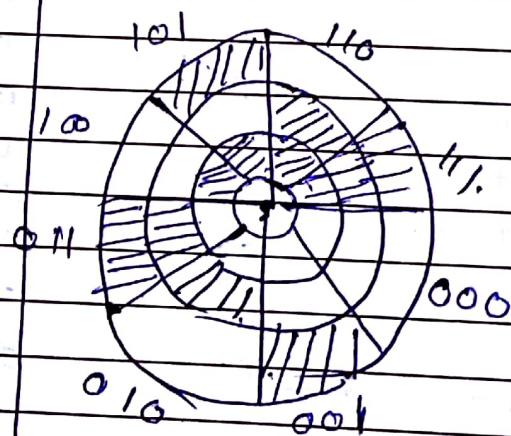
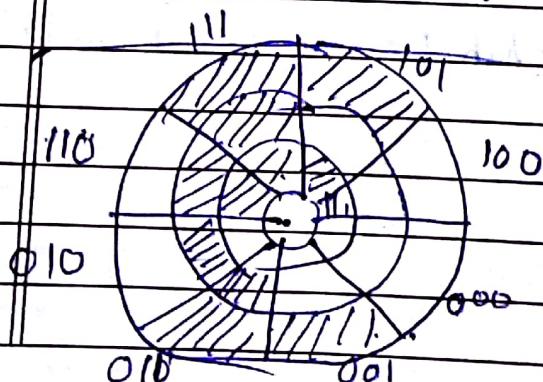


fig 1 shaft position encoder



b) Pattern for binary code.



c) Pattern for gray code.

Page No.

Name: Sucheta P.



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Conversion

Gray to binary

1110 gray to binary

1 1 1 0
| | | 0
↓
1 0 1 1

D

Binary to Gray:

1 0 1 1
↓
1 1 1 0