

## Bipolar Junction Transistor

### CONSTRUCTION

BJT is a three terminal semiconductor device.

Flow of current is due to both electrons and holes hence the name bipolar junction transistor.

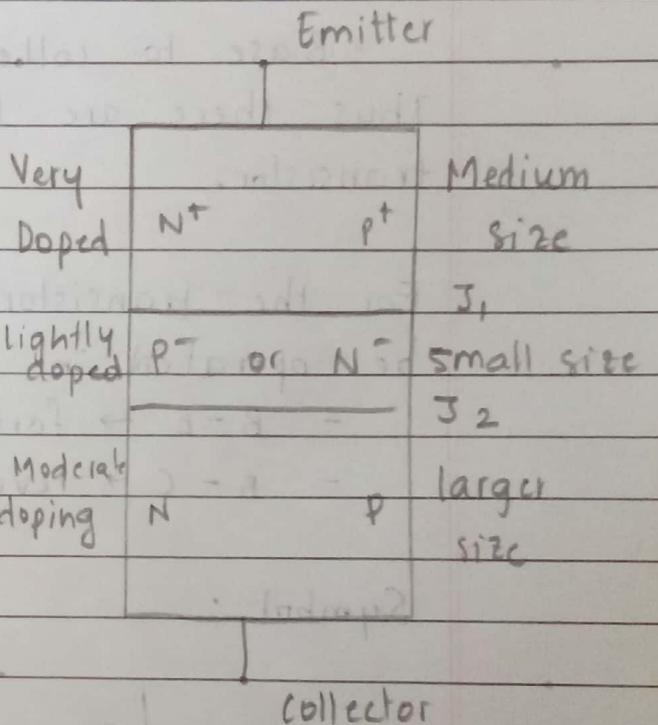
BJT has:

- a - 3 semiconductors layers
- b. two junctions

Collector:

This semiconductor layer has large area and moderate doping

Compared to other two regions, collector regions carries more current.



Hence it generates large amount of heat. To dissipate, that heat, it's made up of large area.

Emitter:

This semiconductor layer has moderate area and high doping.

As the name suggest, this region is supposed to emit more electrons.

Hence doping of this region is always high.

Base:

- This region is always between emitter and collector
- It has less area and less doping.
- This terminal is called as the control terminal and is used to control the collector current of transistor.

There are two junctions in a transistor:

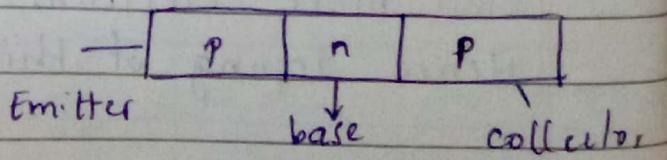
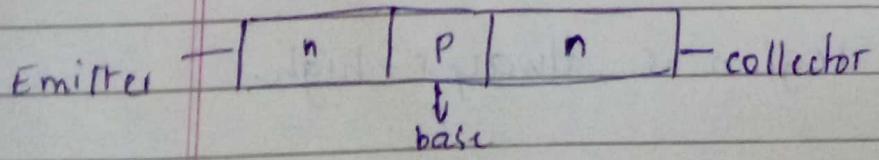
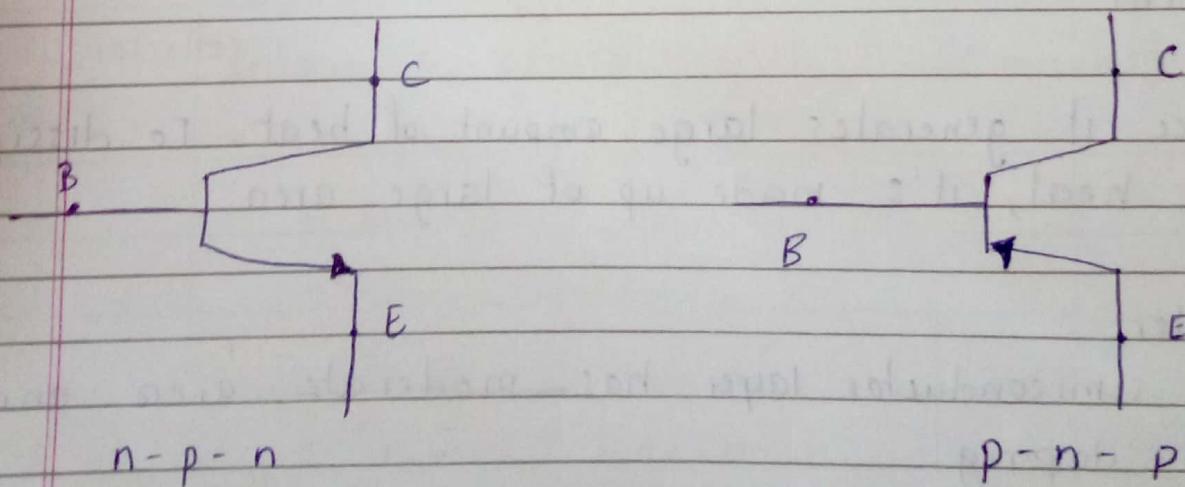
- Base to emitter junction
- Base to collector junction

Thus there are four methods of biasing the transistor.

For the transistor to work as an amplifier, it must be operated in its active mode.

- B - E  $\rightarrow$  forward biased
- B - C  $\rightarrow$  reverse biased

Symbol :

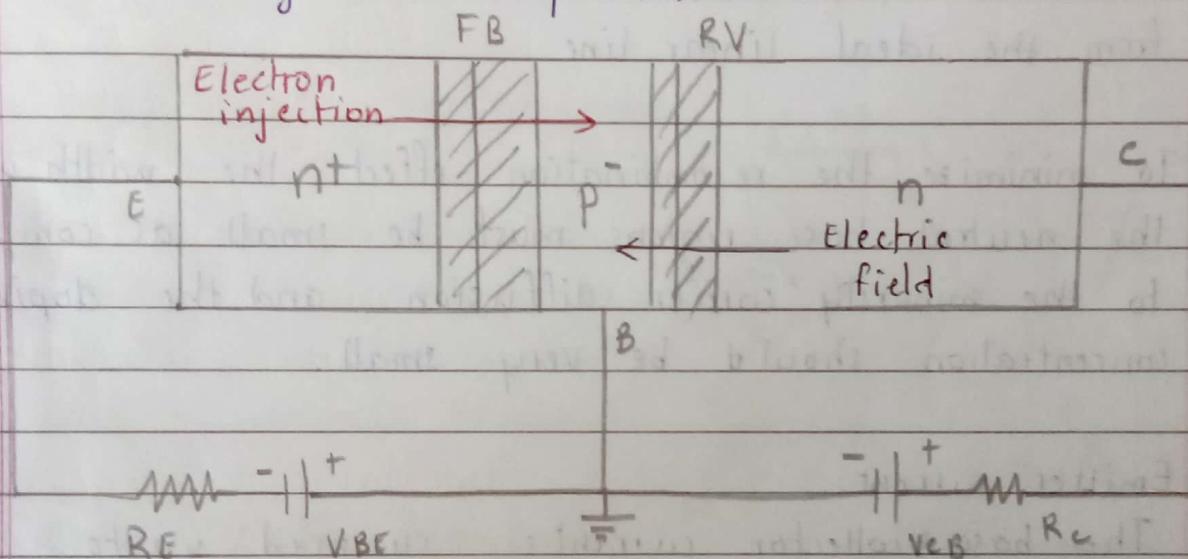


## TRANSISTOR ACTION

Since the Base-Emitter junction is forward biased, electrons from the emitter are injected across the B-E junction.

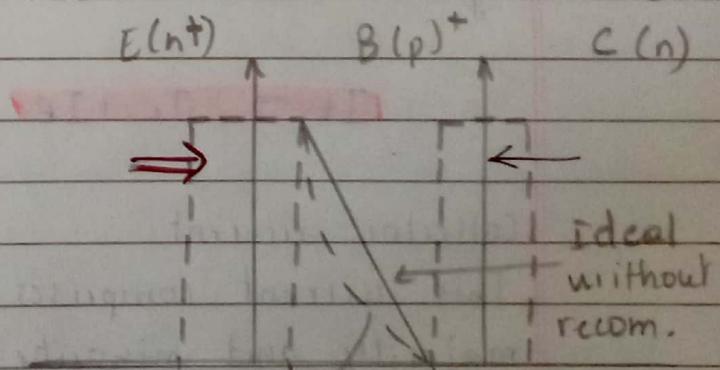
As the base-collector junction is reverse biased, the electron concentration at the edge of this junction is approximately zero.

The base region is very small.



In the ideal case, the injected electrons will not recombine with any of the holes in the base.

Ideally, the electron distribution versus distance through the base is a straight line.



$\Rightarrow$  injection of electrons  
 $\Rightarrow$  electrical field

Electrons injected from the emitter diffuse across the base into the base collector space charge region.

The electric field which exists across the space charge region sweeps the electrons into the collector region creating the collector current.

However if some carrier recombination does occur in the base, the electron concentration will deviate from the ideal linear line.

To minimize the recombination effect, the width of the neutral base regions must be small as compared to the minority carrier diffusion, and the doping concentration should be very small.

Emitter current:

The base & collector currents summed up to give emitter current:

$$I_E = I_C + I_B$$

Collector current:

This current comprises of two components: the majority and minority carriers.

The minority current component is called the leakage current  $I_{CBO}$

$$I_C = I_{C \text{ majority}} + I_{CBO}$$

$$I_C = I_{C(m)} \quad \text{Since } I_{CBO} \approx 0$$

The collector current is slightly smaller than the emitter current.

The emitter and collector currents are related by the following equation:

$$I_C = \alpha I_E$$

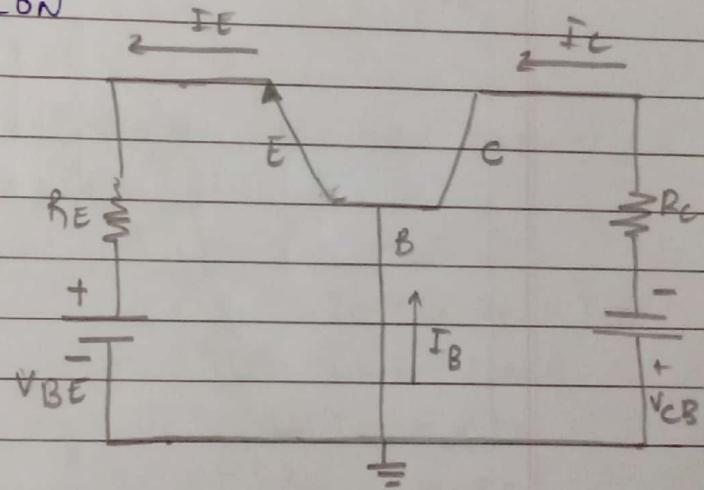
where  $\alpha$  = common base current gain.

### COMMON BASE CONFIGURATION

In this configuration,  
 emitter = input terminal  
 collector = output terminal  
 base = common terminal

E.B J<sub>1</sub> → Forward biased

B.C J<sub>2</sub> → Reverse biased.



$$V_{BE} = V_{EE}$$

$$V_{CB} = V_{CC}$$

I<sub>CBO</sub>: reverse saturation current

$$I_E = I_B + I_C$$

$$I_C = \alpha I_E + I_{CBO} \quad \text{R.S.C.}$$

$$I_C = \alpha I_E$$

since I<sub>CBO</sub> is negligibly small

$\alpha$  is the current gain. (Common base).

$$\text{where gain} = \frac{\text{O/P}}{\text{I/P}} = \frac{I_C}{I_E}$$

$\alpha$ : amplification factor.

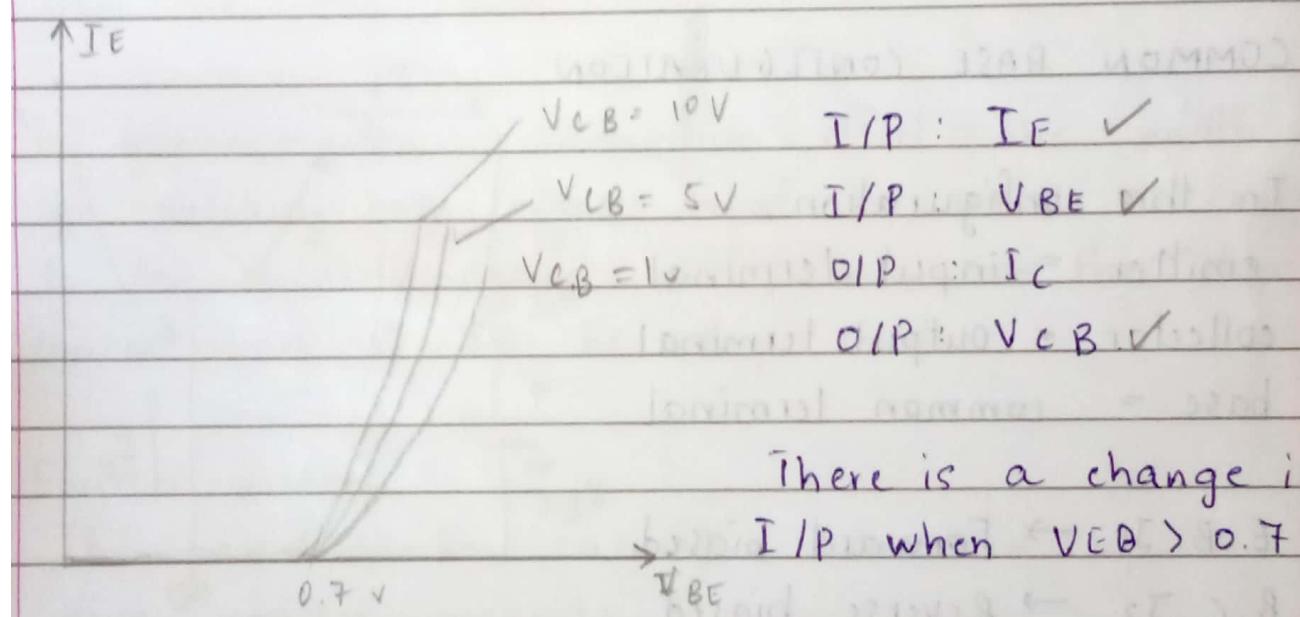
$$\alpha = 0.95 \text{ to } 0.98$$

## input characteristics

- Same as of forward biased diode.

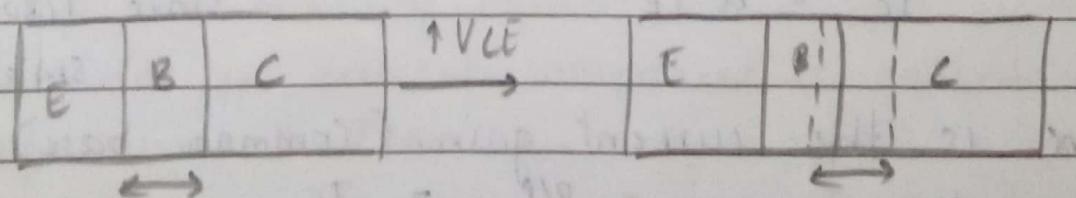
Also for a given input voltage ( $V_{EB}$ ), more input current flows when higher levels of collector are used.

Graph: Relation between input current and input voltage for changing output voltage.



Early Effect / Base width modulation

With  $\uparrow$  in R.B voltage, there is modulation of base width.



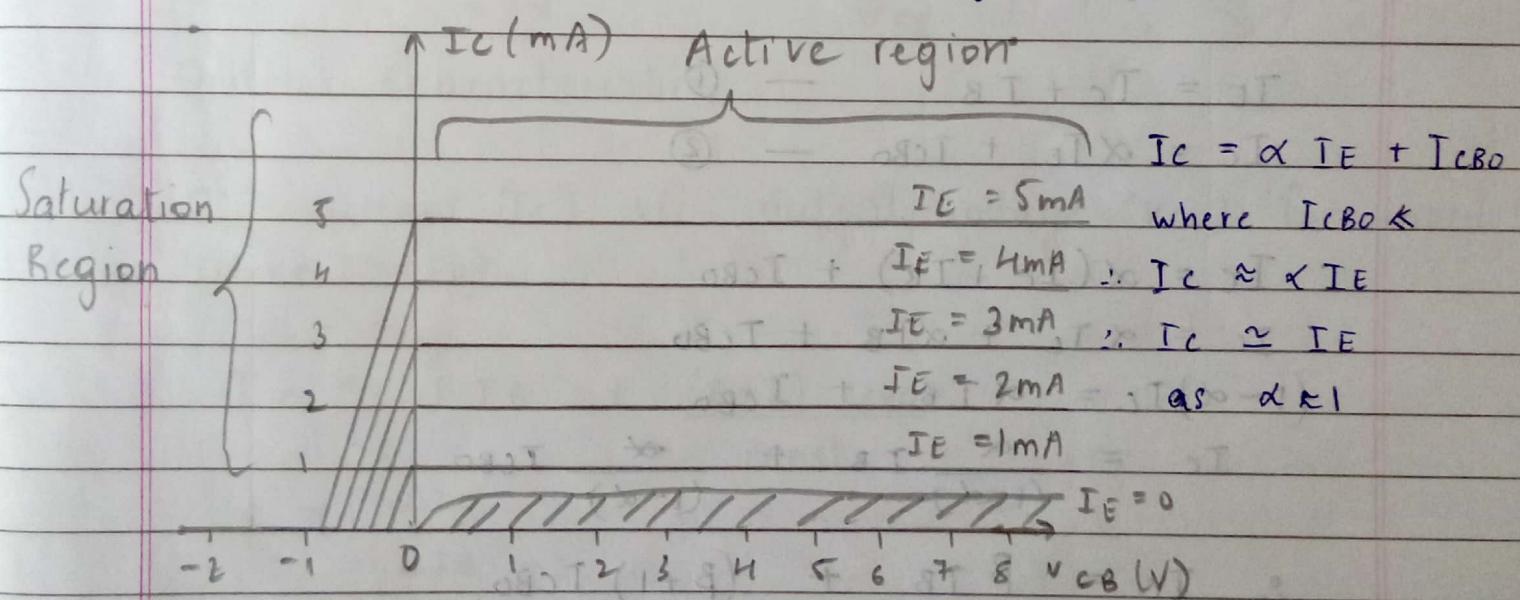
The width of depletion region increases in the base

This decrease has three consequences:

- less chance for recombination within the base region,  $I_B \downarrow$  hence  $I_C \uparrow$ , hence  $\alpha \uparrow$  with  $V_{CB}$
- Charge increased in the base
- For extreme large voltages. The effective base width may be reduced to 0  $\Rightarrow$  voltage breakdown in the transistor. Also called as punch through.

### Output characteristics

Output current vs output voltage for input current



### COMMON Emitter CONFIGURATION

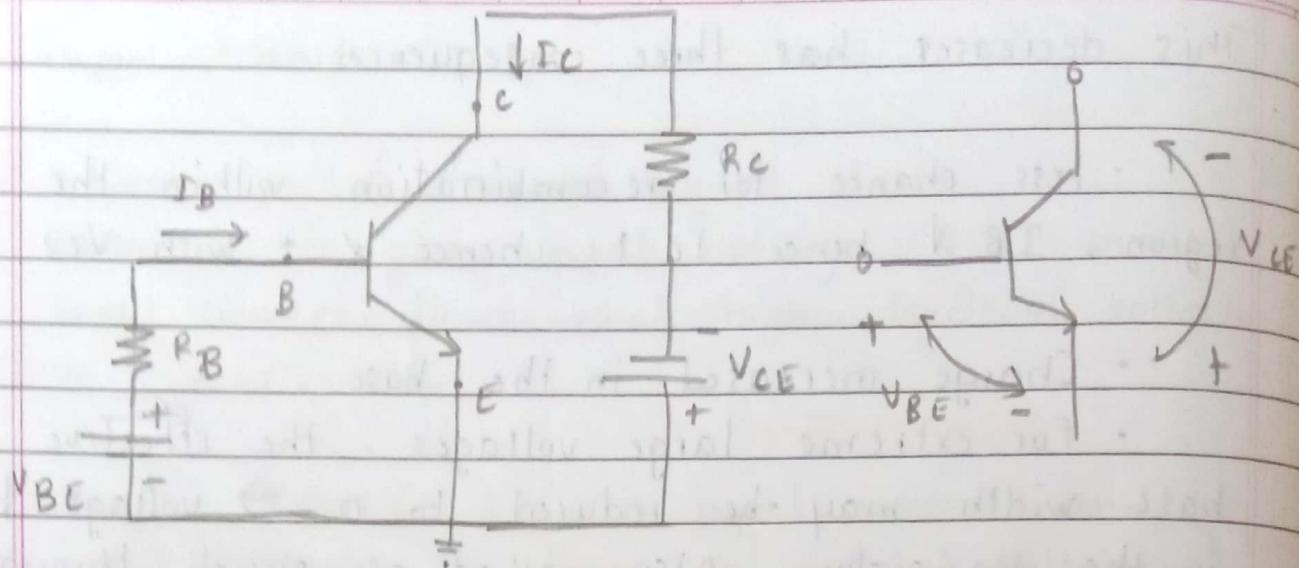
Emitter is the common terminal.

Collector : output terminal

Base: input terminal

$V_{BB}$ : forward biased  $\Rightarrow$  base emitter

$V_{CE}$ : reverse biased  $\Rightarrow$  collector base



$$\text{i/p current} = I_B$$

$$\text{i/p voltage} = V_{BE}$$

$$\text{o/p current} = I_C$$

$$\text{o/p voltage} = V_{CE}$$

$$I_E = I_C + I_B \quad \dots \quad (1)$$

$$I_C = \alpha I_E + I_{CBO} \quad \dots \quad (2)$$

$$I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$I_C = \alpha I_C + \alpha I_B + I_{CBO}$$

$$(1 - \alpha) I_C = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{(1 - \alpha)} I_B + \frac{\alpha}{(1 - \alpha)} I_{CBO}$$

$$\therefore I_C = \beta I_B + \underbrace{(\beta + 1) I_{CBO}}$$

where  $\beta = \frac{\alpha}{1 - \alpha}$ . R.S.C. in C.E.

$$\therefore I_C = \beta I_B + I_{CEO}$$

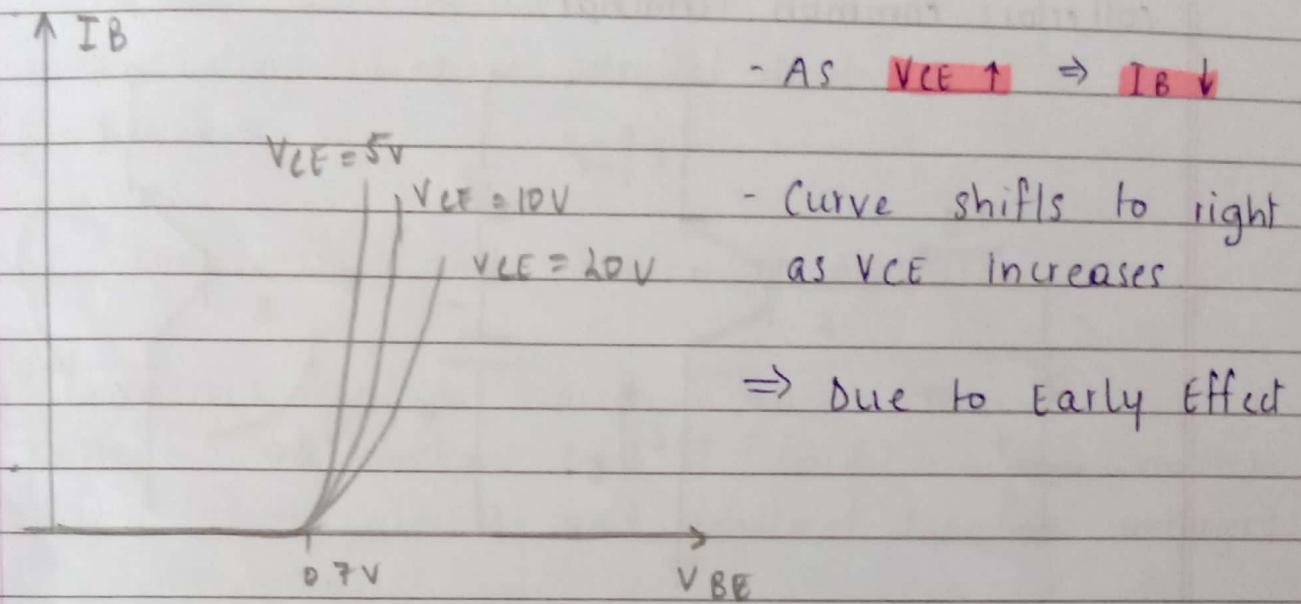
$$\text{but } I_{CEO} \ll \beta I_B$$

$I_C = \beta I_B$  where  $\beta$ : current amplification factor

For CE configuration,  $\beta : 50 \rightarrow 400$

## Input characteristics

I/P current ( $I_B$ ) v/s Input voltage ( $V_{BE}$ ) for output voltage ( $V_{CE}$ )



- As  $V_{CE} \uparrow \Rightarrow I_B \downarrow$

- Curve shifts to right  
as  $V_{CE}$  increases

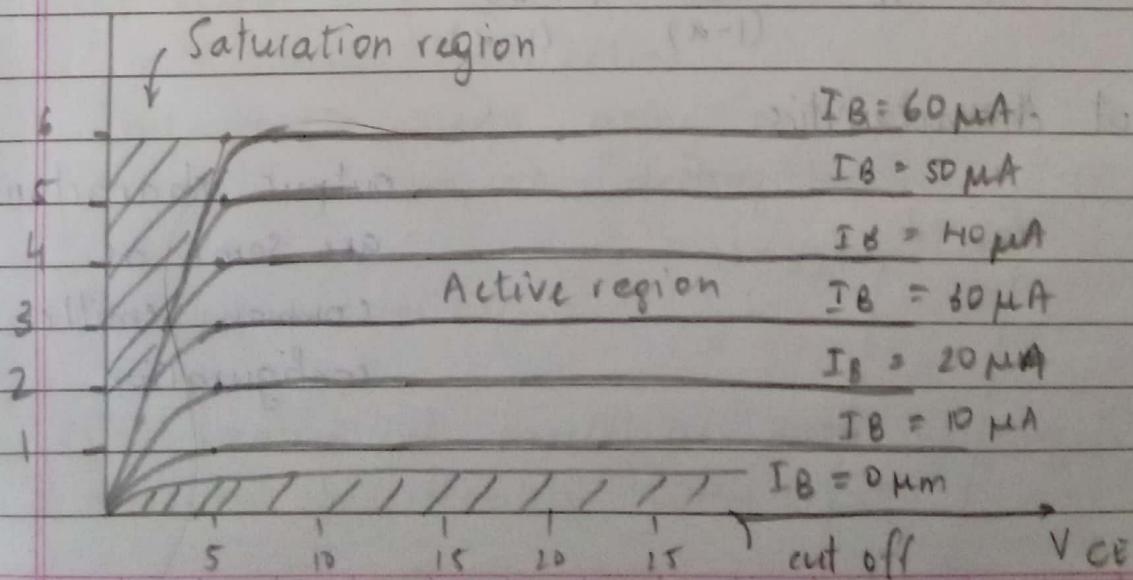
$\Rightarrow$  Due to Early Effect

## Output characteristics

O/P current ( $I_C$ ) v/s output voltage ( $V_{CE}$ ) for input current ( $I_B$ )

$$I_C = \beta I_B + (\beta + 1) I_{CBO}$$

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

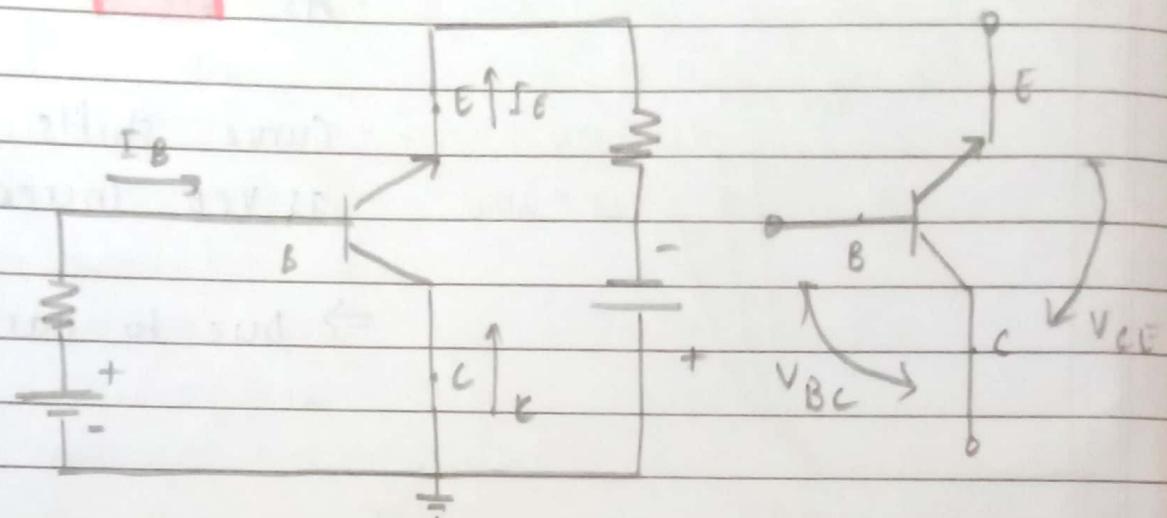


## COMMON COLLECTOR CONFIGURATION

Emitter: input terminal

base: output terminal

collector: common terminal



$$y = \frac{\Delta I_E}{\Delta I_B}$$

$$I_E = I_C + I_B \quad \text{--- (1)}$$

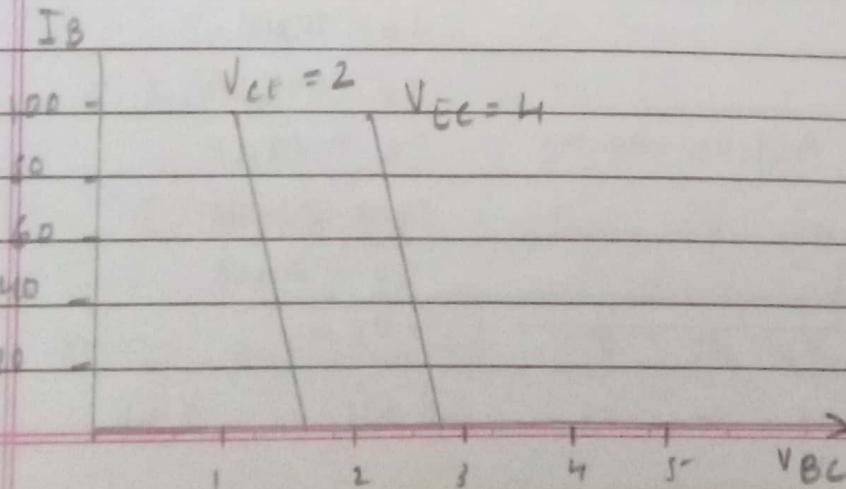
$$I_C = \alpha I_E + I_{CBO} \quad \text{--- (2)}$$

$$\therefore I_E = \alpha I_E + I_{CBO} + I_B$$

$$(1 - \alpha) I_E = I_{CBO} + I_B$$

$$I_E = \frac{I_{CBO}}{(1-\alpha)} + \frac{I_B}{(1-\alpha)}$$

Input characteristics.



Output characteristic  
are same as  
common emitter  
configuration.

## BIASING TECHNIQUES

Fixed bias

Collector to base bias

Fixed bias with emitter resistor

Voltage divider bias or potential divider

Emitter bias

## DC LOAD LINE and REGION OF OPERATION

Transistors must be biased in an on state

with : - constant level of collector, base, emitter  
- current and constant terminal voltages.

Level of  $I_C$  and  $V_{CE}$  define operating point of transistor, also known as quiescent point (Q point)

With increase of temperature of C-B junction, resistance  $\downarrow$  and  $I_C \uparrow$ .

The operating point shifts with change in transistor parameters such as  $B$ ,  $I_{BO}$  and  $V_{BE}$

For every  $10^\circ \uparrow$  in  ${}^\circ\text{C}$ ,  $I_{BO} \times 2 \rightarrow I_C \uparrow$

$\hookrightarrow$  power dissipation

This process keeps going on and it will lead to thermal runaway  $\rightarrow$  destroy transistor.

## Stability Factor ( $s$ )

Stabilization of current  $I_C$  with varying  $I_C$  is measured by stability factor ( $s$ )

Defined as rate of change of collector current w.r.t. to collector base leakage current  $I_{CBO}$  with  $I_B$  and  $\beta$  constant

$$S = \frac{dI_c}{dI_{CBO}} \quad | \quad \beta, V_{BE}$$

Expression for stability factor

$$S = \frac{dI_c}{dI_{CBO}}$$

We know that

$$I_c = \beta I_B + (1 + \beta) I_{CBO}$$

Differentiating both sides w.r.t ' $I_c$ '

$$\frac{dI_c}{dI_c} = \beta \frac{dI_B}{dI_c} + (1 + \beta) \frac{dI_{CBO}}{dI_c}$$

$$1 = \beta \frac{dI_B}{dI_c} + (1 + \beta) \frac{dI_{CBO}}{dI_c}$$

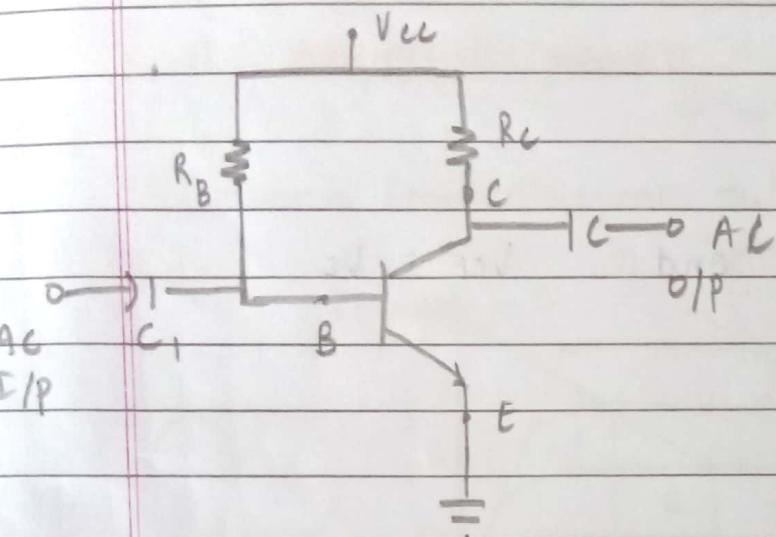
$$1 - \beta \frac{dI_B}{dI_c} = (1 + \beta) \frac{dI_{CBO}}{dI_c}$$

$$\frac{dI_{CBO}}{dI_c} = \frac{1 - \beta \frac{dI_B}{dI_c}}{1 + \beta}$$

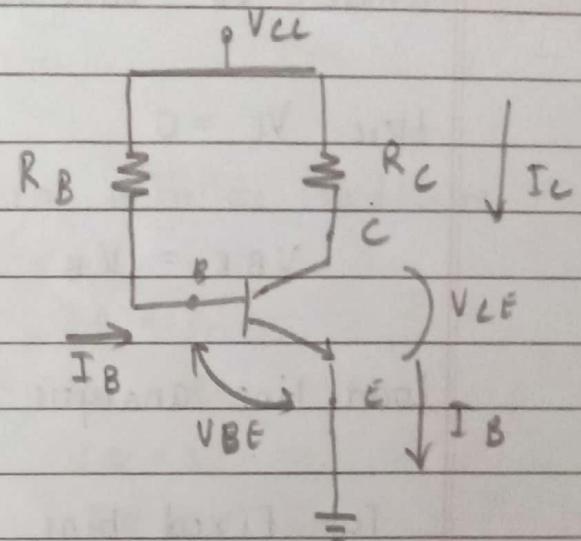
$$\frac{dI_c}{dI_{CBO}} = \frac{1 + \beta}{1 - \beta \frac{dI_B}{dI_c}}$$

⇒ To calculate S factor we need to calculate  
First  $\frac{dI_B}{dI_C}$

### FIXED BIAS CIRCUIT



Fixed Bias LCT



DC equivalent of  
Fixed Bias Ckt

Applying KVL in i/p loop:

$$V_{CC} - R_B I_B - V_{BE} = 0 \quad \text{--- (1)}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Applying KVL in o/p loop:

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C \quad \text{--- (2)}$$

Magnitude of current given by  $I_C$  by  
use this eq  
to calculate

$$I_C = \beta I_B \quad \text{--- (3)} \quad I_C$$

From eq (2) :

$$I_C = \frac{V_{CC} - V_{CE}}{R_C} \quad \text{--- (4)}$$

$$V_{CE} = V_C - V_E \quad \text{--- (5)}$$

where  $V_C$ : collector voltage,  $V_E$ : emitter voltage

$$V_{BE} = V_B - V_E$$

where  $V_B$ : base voltage — (6)

Here  $V_E = 0$ ,

$$V_{BE} = V_B$$

and

$$V_{CE} = V_C$$

### Load Line analysis

For Fixed bias ckt:

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

$$I_C = \frac{V_{CC}}{R_C} - \left[ \frac{1}{R_C} \right] V_{CE}$$

$$I_C = \left[ \frac{-1}{R_C} \right] V_{CE} + \frac{V_{CC}}{R_C}$$

⇒ equation of straight line.

$$y = mx + c$$

where  $y = I_C$

$$m = -\frac{1}{R_C}$$

$$c = \frac{V_{CC}}{R_C}$$

To get points on line, we have to assume:

-  $I_C = 0$  then  $V_{CE} = V_{CC}$

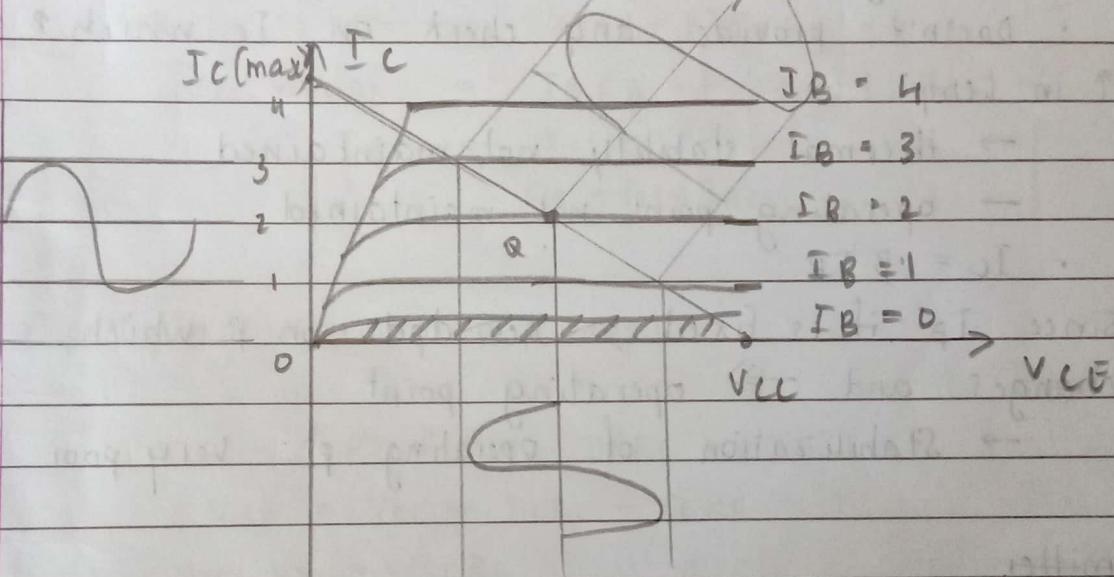
-  $V_{CE} = 0$  then  $I_C = \frac{V_{CC}}{R_C}$

Q point : center of DC Load Line to prevent distortion and must be in active region.

If Q point near saturation region, it gives clipping at positive peaks.

If Q point near cut-off region, it gives clipping at negative peaks.

Common Emitter open output ckt with dc load line



DC line : plot of  $I_c$  vs  $V_{ce}$

To identify the operating region of transistor we can observe certain conditions:

For saturation  $I_B > \frac{I_C}{\beta_{dc}}$

For active region  $V_{ce} > V_{ce}(\text{sat})$

## Advantages of fixed bias circuit

- Simple circuits which uses few components
- Q point can be fixed anywhere in the active region by changing value of  $R_B$ .  
→ maximum stability in design.

## Disadvantages of Fixed bias circuit.

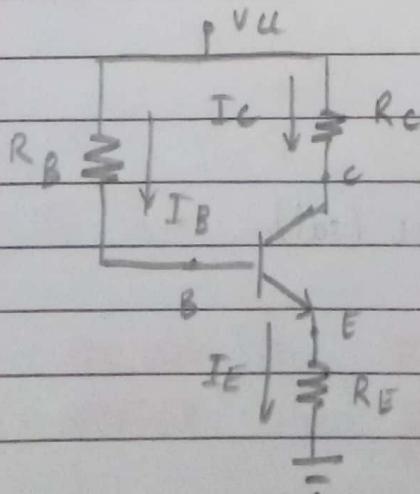
- Doesn't provide any check on  $I_C$  which ↑ with ↑ in temp.  
→ thermal stability not maintained
- operating point not maintained
- $I_C = \beta I_B$   
since  $I_B$  if is fixed ;  $I_C$  depends on  $\beta$  which changes and → operating point  
→ Stabilization of operating pt. very poor.

## Emitter

### EMITTER STABILIZED BIASED CIRCUIT

To improve stability of biasing in fixed circuit,  $R_E$  is connected to biasing ckt.

⇒  $\beta$  Emitter Bias circuit



## Circuit Analysis

Applying KVL in i/p loop:

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \quad \text{--- (1)}$$

$$\text{We have, } I_E = (1 + \beta) I_B \quad \text{--- (2)} \quad I_C = I_C + I_B \\ = \beta I_B + I_B \\ = (1 + \beta) I_B$$

Put (2) in (1)

$$V_{CC} - I_B R_B - V_{BE} - (1 + \beta) I_B R_E = 0$$

$$V_{CC} - V_{BE} = I_B R_B + (1 + \beta) I_B R_E$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta) R_E}$$

Applying KVL in o/p loop:

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$V_E = I_E R_E$$

$$V_{CE} = V_C - V_E$$

$$V_C = V_{CC} - I_C (R_C + R_E)$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \quad \text{--- (3)}$$

Stability improvement

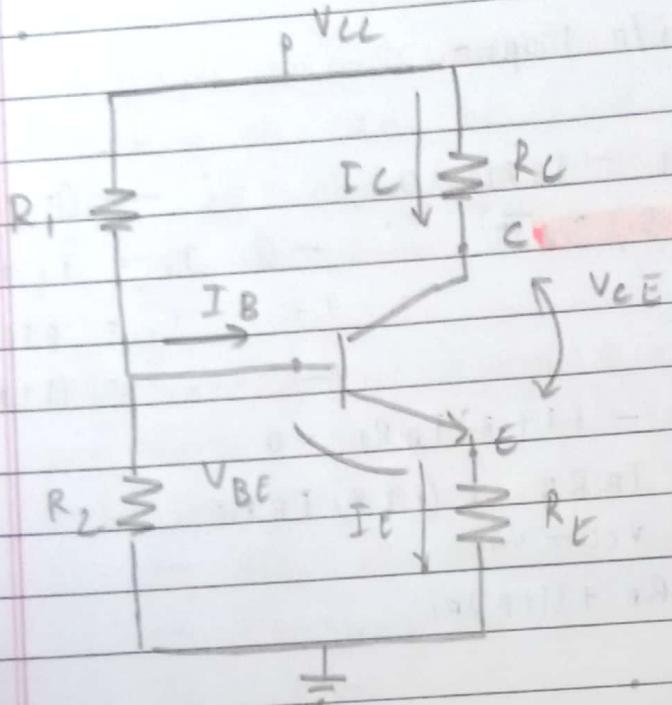
+ of  $R_E$  in clkt improve the stability.

Load Line Analysis

Plot:  $I_C$  Vs  $V_{CE}$ .

$$A = \frac{V_{CC}}{R_C + R_E} \quad B = V_{CC}$$

## VOLTAGE DIVIDER BIASED (V.D.B)



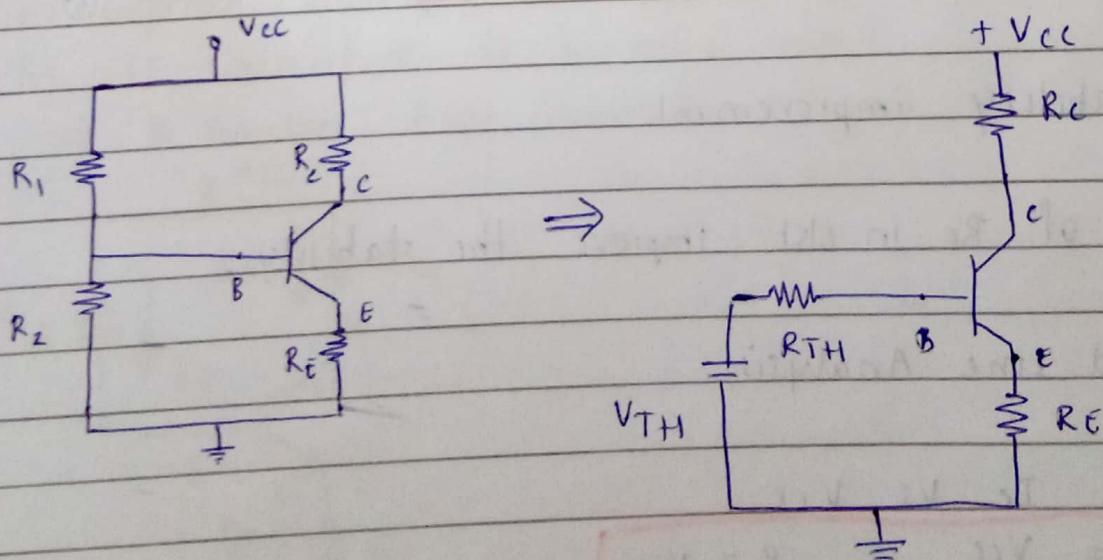
V.D.B ckt

Biasing given by  $3R_1, R_2$  and  $R_E$

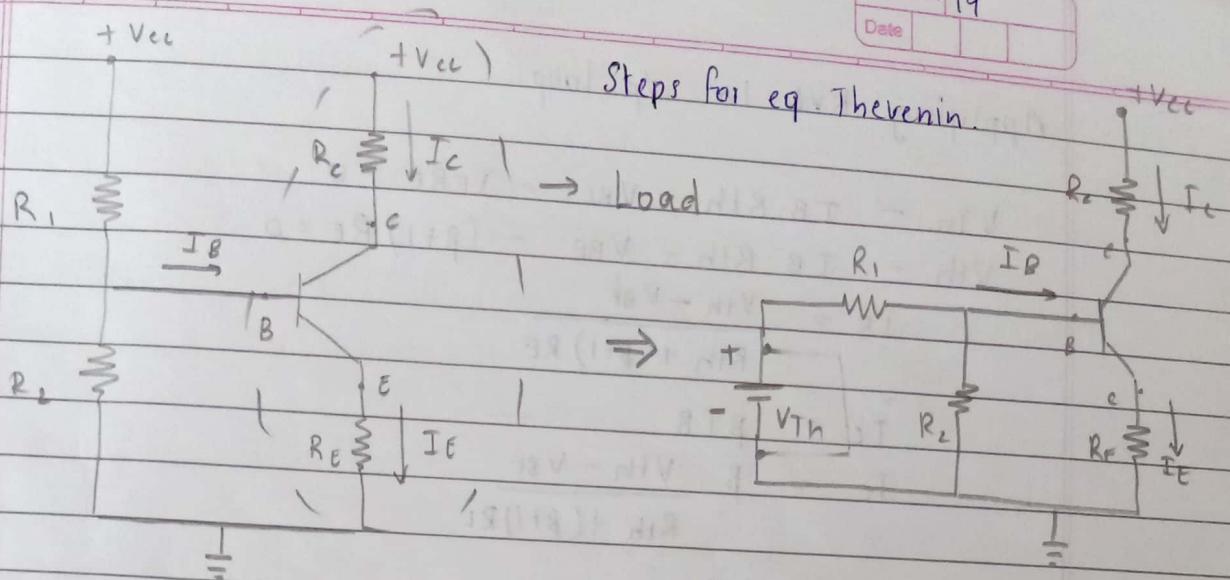
$R_1$  and  $R_2$  acts as potential divider  
 $\Rightarrow$  fixed voltage to base

If  $I_c \uparrow$  due to change in temp° or  $B$ ,  $I_{ET} \uparrow$ , voltage drop across  $R_E \uparrow \Rightarrow V_{BE}$ . Due to reduc° in  $V_{BE}$ ,  $I_B$  and  $I_c \downarrow$ .  
 $\Rightarrow$  negative feedback exists in emitter bias circuit.

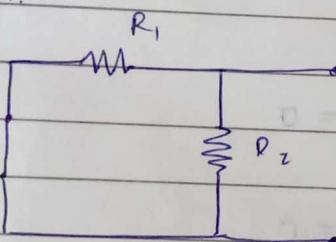
Circuit analysis (use of Thevenin's theorem).



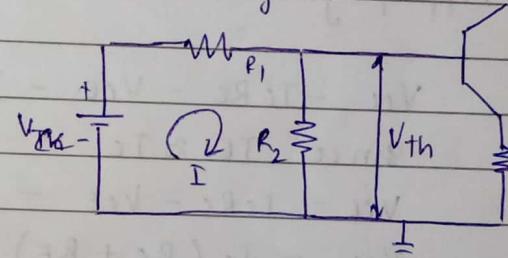
Eq. Thevenin of V.D.B.



$R_{Th}$ :



Voltage  $V_{Th}$ :



source : open ckt short

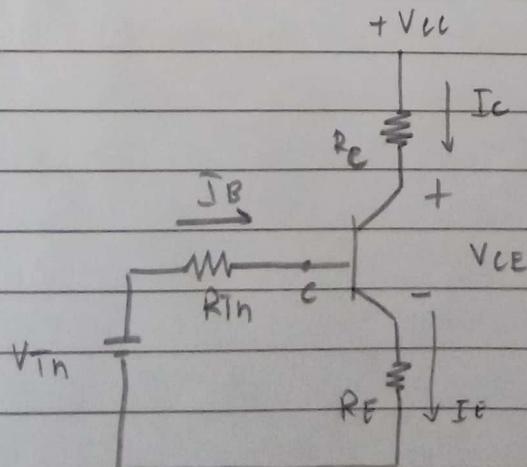
load : open

$R_1$  and  $R_2$  in parallel

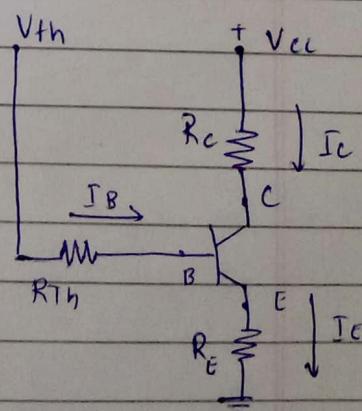
$$I = \frac{V_{CC}}{R_1 + R_2}$$

$R_{Th} : R_1 || R_2$

$$= \frac{R_1 R_2}{R_1 + R_2} \quad V_{Th} = I R_2 = \frac{R_2 V_{CC}}{R_1 + R_2}$$



Emitter Bias ckt



Applying KVL in i/p loop:

$$V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

$$V_{Th} - I_B R_{Th} - V_{BE} - (\beta + 1) R_E = 0$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E}$$

$$I_C = \beta I_B$$

$$I_C = \beta \frac{V_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E}$$

$$R_{Th} \ll (\beta + 1) R_E$$

Applying KVL in o/p loop.

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

since  $I_E \approx I_C$

$$V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0$$

$$V_{CC} - I_C (R_C + R_E) - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Advantages of voltage divider configurations

- $\beta$  independant of  $I_C$ .

# COMPARISON OF CONFIGURATIONS

Parameters	C-B	C-E	C-C
I/p resistance	Very low	Low	High
O/p resistance	Very High	High	Low
Current gain	$\alpha_{dc} = \frac{I_C}{I_C} < 1$	$\beta = \frac{I_C}{I_B}$ high	$1 + \beta_{dc}$ very high
Voltage gain	Medium	Highest	Lowest
Power gain	Medium	High	Medium

**h Parameters or Hybrid parameters.**

For CB configuration

Input Impedance ( $h_{ib}$ )

- ratio of change in input voltage ( $V_{BE}^{EB}$ ) to change in input current ( $I_E$ ) at a constant output voltage ( $V_{CB}$ )

$$h_{ib} = \left. \frac{\Delta V_{EB}}{\Delta I_E} \right|_{V_{CB} \text{ const}}$$

- determined from i/p characteristics.

### Output admittance $h_{ob}$

- ratio of change in current  $I_c$  to change in  $\frac{\text{output}}{\text{input}}$  current  $I_E$ , voltage  $V_{CB}$  at constant base  $I_B$ .

$$h_{ob} = \frac{\Delta I_c}{\Delta V_{CB}} \quad | I_B = \text{const}$$

- determined from output characteristics of diode

### Forward current gain $h_{fb}$

- ratio of change collector current  $I_c$  to input current  $I_E$ ,  $V_{CB}$  constant

$$h_{fb} = \frac{\Delta I_c}{\Delta I_E} \quad | V_{CB} \text{ const}$$

- determined from o/p characteristics

### Reverse Voltage gain $h_{rb}$

- ratio of change in input voltage  $V_{EB}$  to output voltage  $V_{CB}$ ,  $I_E$  const.

$$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}} \quad | I_E = \text{const}$$

- determined from i/p characteristics.

## Configuration

C.B.

hi

$$\frac{\Delta V_{EB}}{\Delta I_E} \frac{x}{4}$$

ho

$$\frac{\Delta V_{EE}}{\Delta V_{CB}} \frac{4}{x}$$

hf

$$\frac{4}{x}$$

hr

cht

$$\frac{x}{4}$$

C.E

$$\frac{\Delta V_{EB}}{\Delta I_B} \frac{2x}{4}$$

$$\frac{\Delta I_C}{\Delta V_{CE}} \frac{4}{x}$$

$$\frac{4}{x}$$

$$\frac{x}{4}$$

Determined  
from.

I/p for=const O/p. for=C O/p for=C I/p for=const

Input for  
CB.

$$hi \left. \begin{array}{l} \\ \end{array} \right\} V_{CB} \text{ const}$$

$$ho \left. \begin{array}{l} \\ \end{array} \right\} I_E \text{ const}$$

$$hf \left. \begin{array}{l} \\ \end{array} \right\} I/p \text{ charac}$$

$$hf \left. \begin{array}{l} \\ \end{array} \right\} O/p \text{ charact.}$$

CE.

$$hi \left. \begin{array}{l} \\ \end{array} \right\} V_{CE} \text{ const}$$

$$ho \left. \begin{array}{l} \\ \end{array} \right\} I_B \text{ const}$$

$$hf \left. \begin{array}{l} \\ \end{array} \right\} I/p \text{ charact}$$

$$hf \left. \begin{array}{l} \\ \end{array} \right\} O/p \text{ charact.}$$

$$I/p \text{ charac} = \frac{x}{4}$$

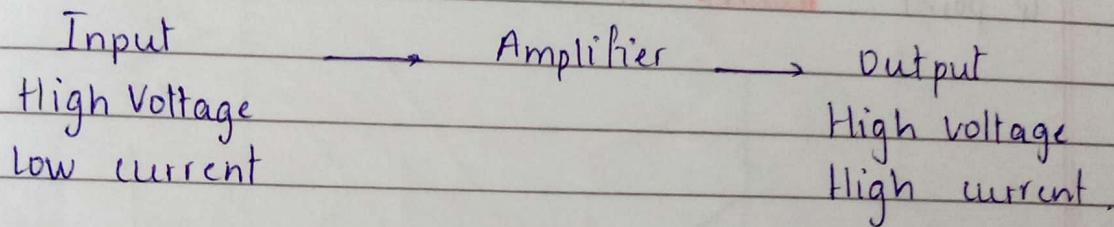
$$O/p \text{ chara} = \frac{4}{x}$$

## POWER AMPLIFIER

An amplifier receives some input signal  $\rightarrow$  larger version as output.

Small signals amplifiers: voltage amplifiers

Large signals amplifiers: power amplifiers.



Power amplifiers are directly connected to load.

Main features:

- circuit's power efficiency
- power amp: bulky
- capable of handling large power
- power transistor required
- o/p impedance matching with load.

Classification :

Class A  $\rightarrow$  Centre of load line

Class B  $\rightarrow$  Cutoff region

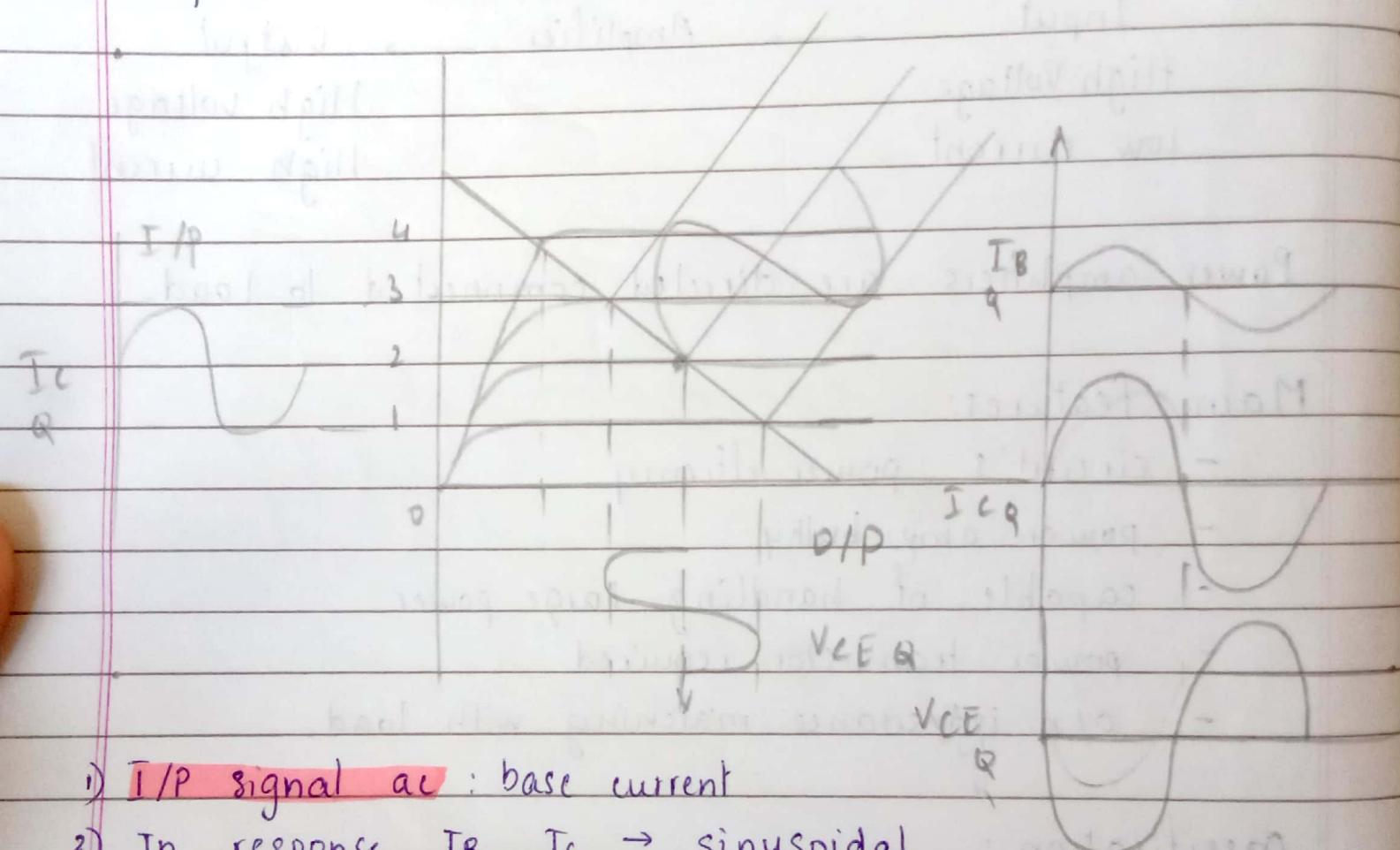
Class C  $\rightarrow$  Below cut off region

Class A  $\rightarrow$  Above cut off

# Class A power amplifier

Power amplifier which conducts for full cycle duration of input ac signal is called class A amplifier.

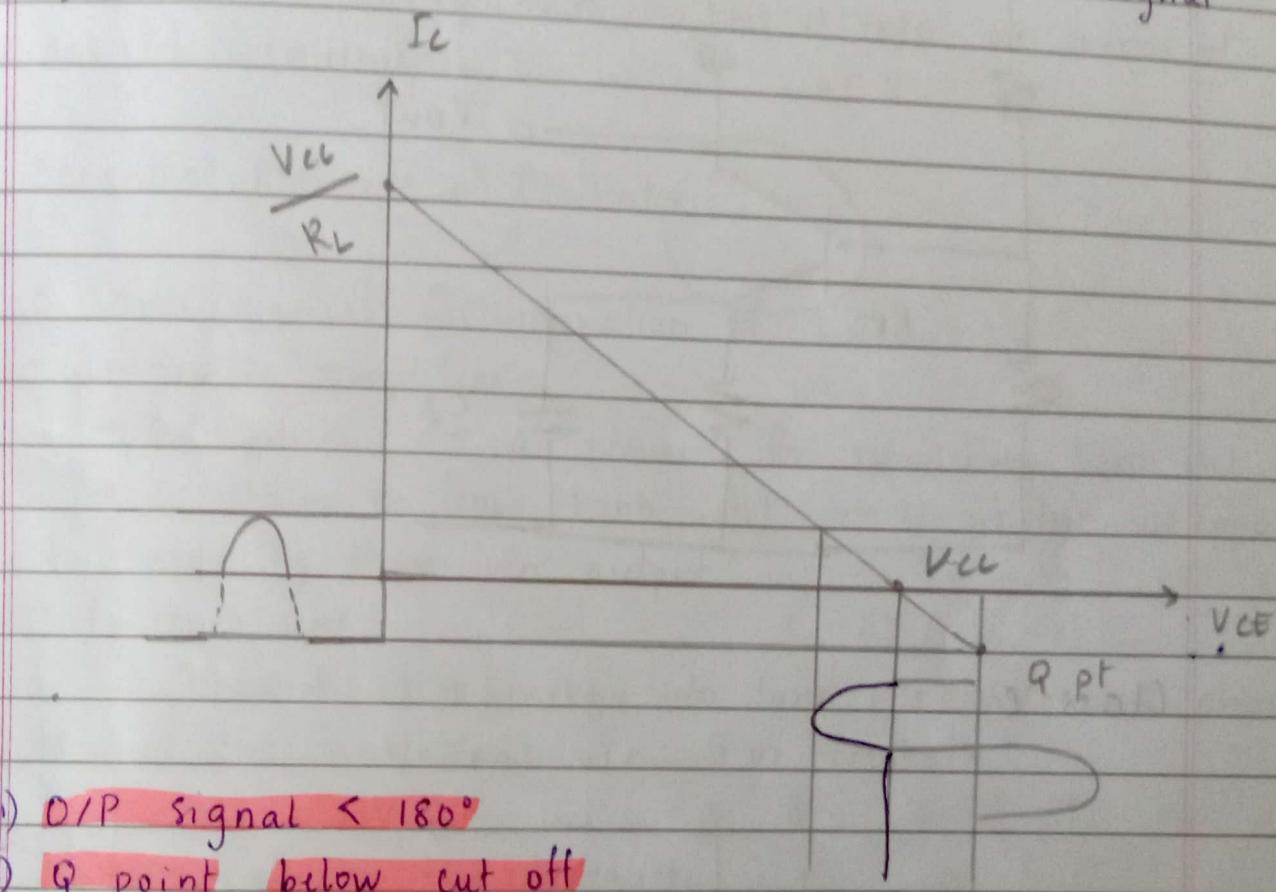
Q point : centre of load line ( $I_C$  vs  $V_{CE}$ )



- 1) I/P signal ac : base current
- 2) In response  $I_B$   $I_C \rightarrow$  sinusoidal  
 $I_C$  in phase  $I_B$
- 3) In response  $I_C$   $V_{CE} \rightarrow$  sinusoidal  
 $V_{CE}$   $I_C$  out of phase  $180^\circ$
- 4) In Active region
- 5) No distortion
- 6) Less efficiency
- 7)  $\eta : 25\% \text{ to } 50\%$

## Class C amplifiers.

Power amplifier is a class c if output is obtained for less than half a cycle period of ac signal.



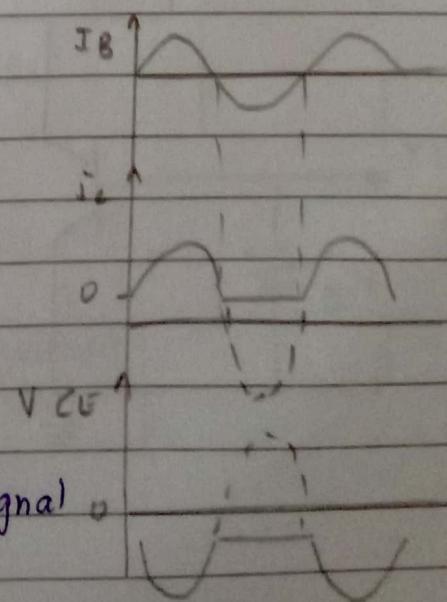
- 1) O/P signal  $< 180^\circ$
- 2) Q point below cut off
- 3) Heavy distortion.  
hence not used as A.F amplifier
- 4) Very high efficiency  
Highest .95

Advantages:

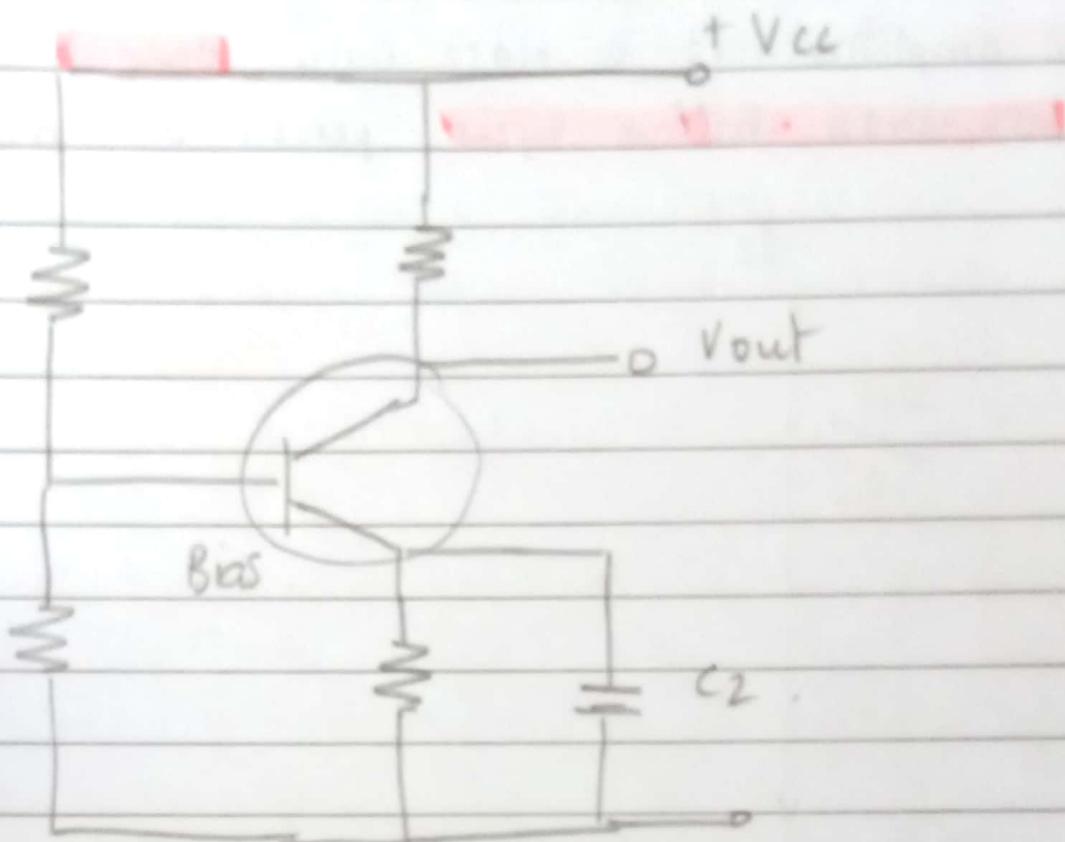
- Low power loss
- High efficiency

Disadvantages

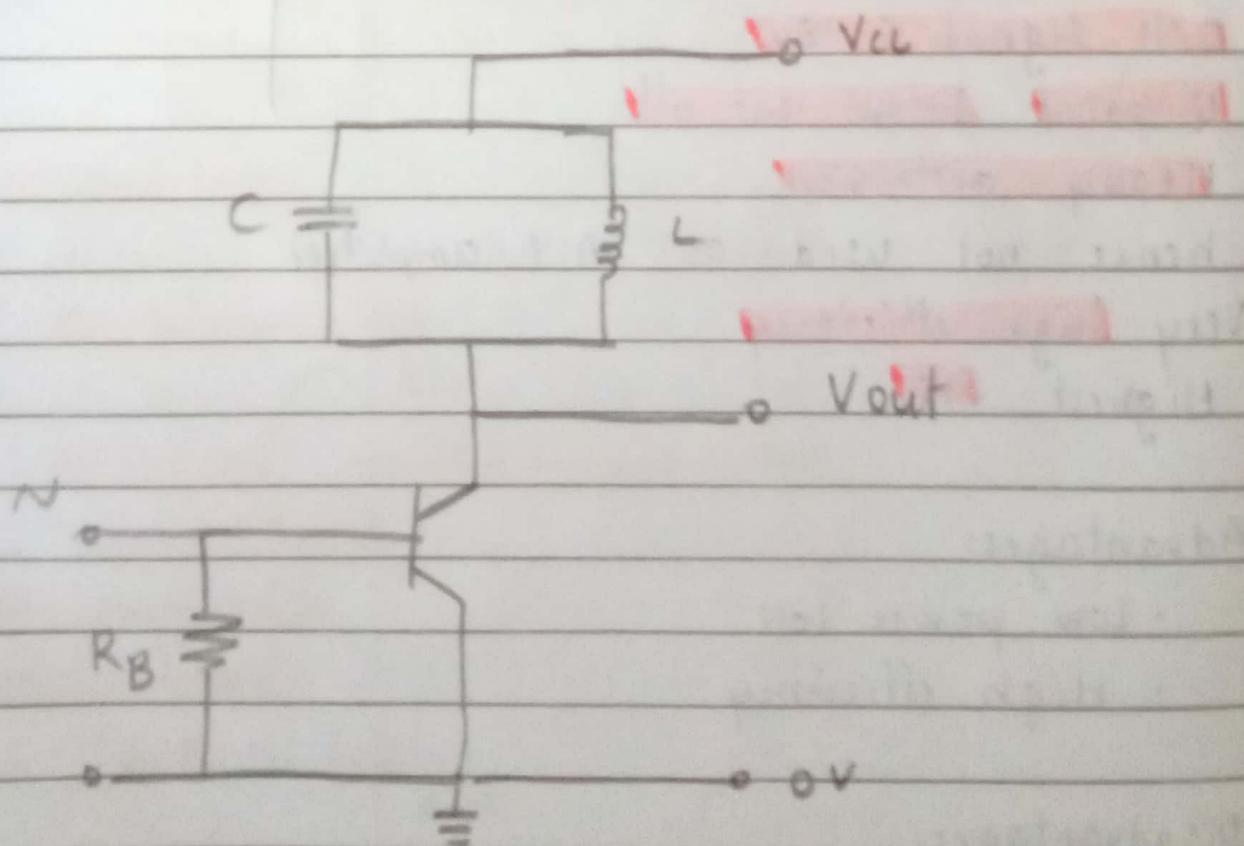
- Heavily distorted o/p signal



Class A



Class C



## OSCILLATOR

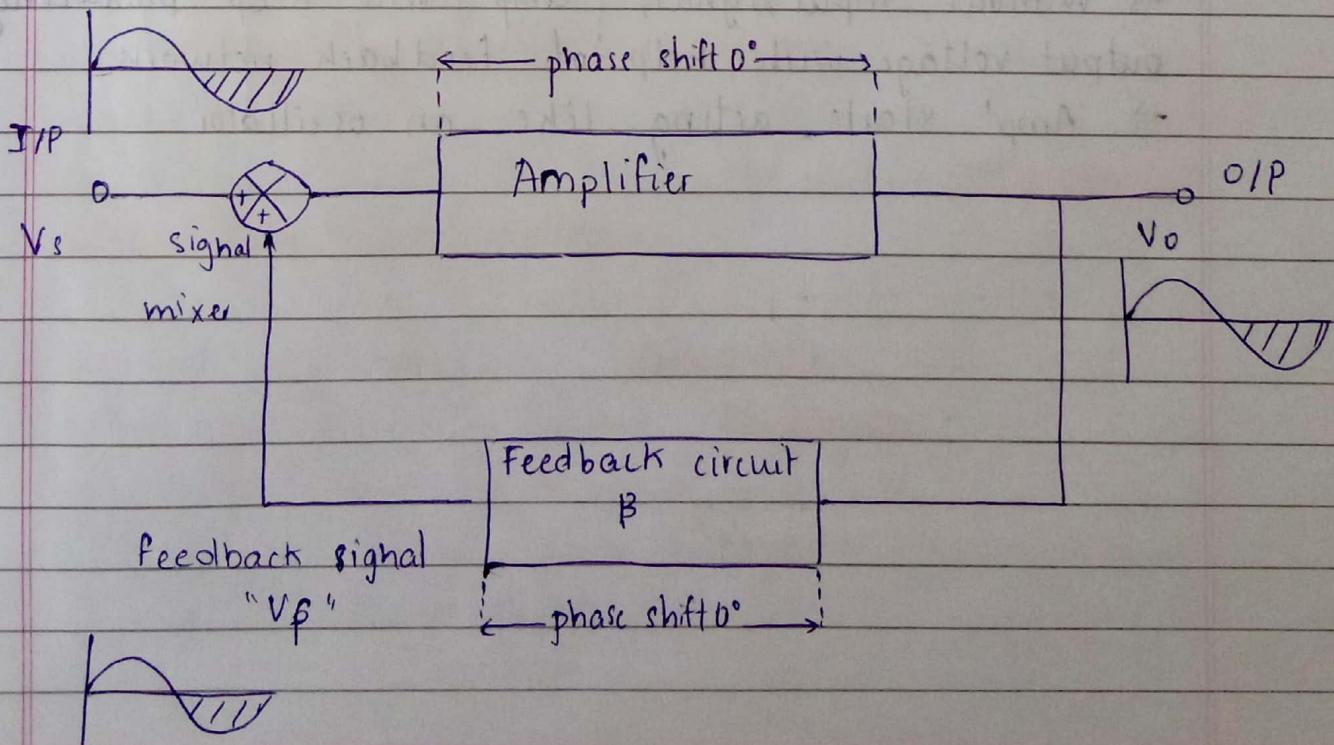
Electric device that generates sinusoidal oscillations of desired frequency.

Receives DC energy and changes it into ac energy of desired frequency.

### Essential Elements of Oscillator

- Tank circuit (combination of L and C)
- Transistor amplifier
  - DC power → AC power for supplying tank ckt
  - oscillations from tank ckt → transistor as input to amplify them in output
- Feedback ckt
  - supplies o/p energy to tank ckt in correct phase to aid the oscillations i.e. +ve feedback.

### Principle of positive feedback.



Oscillator: amp' with +ve feedback

→ part of o/p is fed back through feedback ck. in phase with original i/p signal

Here, amp' assumed as non inverting.

(1)  $V_f = \beta V_o$ , where  $\beta$ : feedback factor

Amplifier gain with feedback:

(2)  $A_F = \frac{A}{1 - A\beta}$ , where  $A$  = open loop gain of amp'

Conclusion:

1)  $A\beta > 0$

$(1 - A\beta) < 1$

$\therefore A_F > A$  Positive feedback will ↑ amp' gain

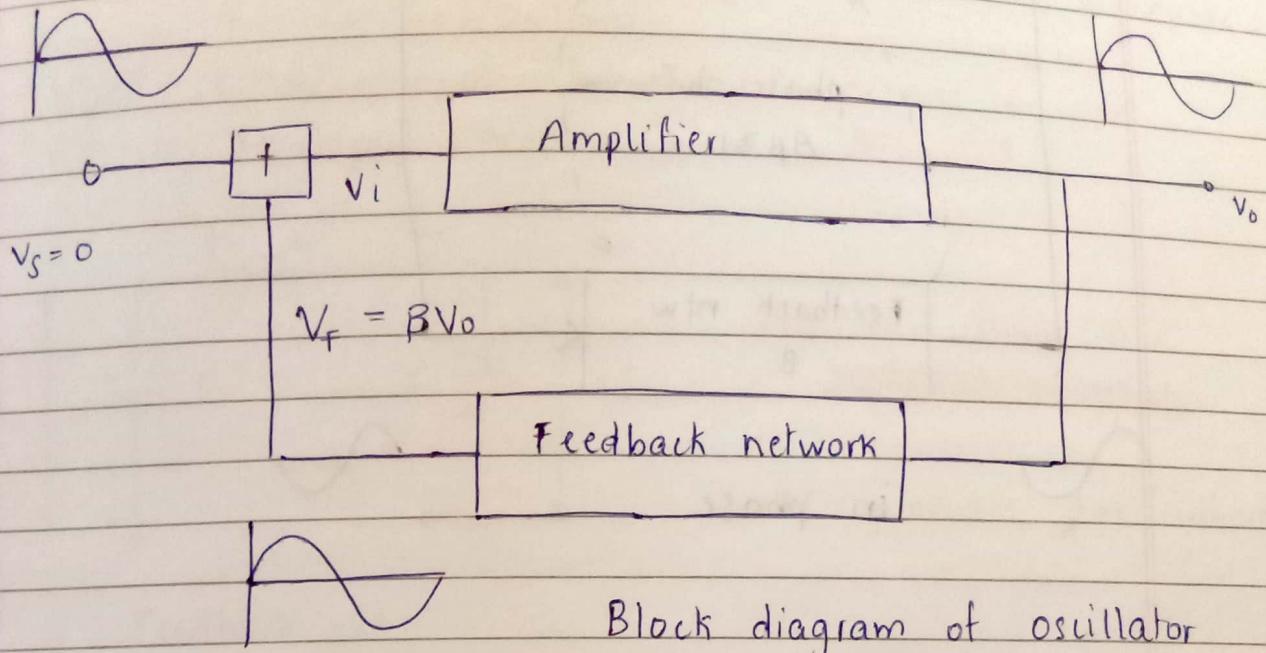
2) If  $\beta \uparrow$  with  $A = \text{const}$  then  $A_F \uparrow$ .

and at a particular value of  $\beta$ ,  $A_F = \infty$

⇒ Without input signal, amp' will keep producing output voltage with help of feedback network.

⇒ Amp' starts acting like an oscillator

## Barkhausen Criteria



For oscillator ckt, no input signal, hence feedback signal  $V_F$  should be sufficient to maintain oscillations.

Statement of Barkhausen criteria.

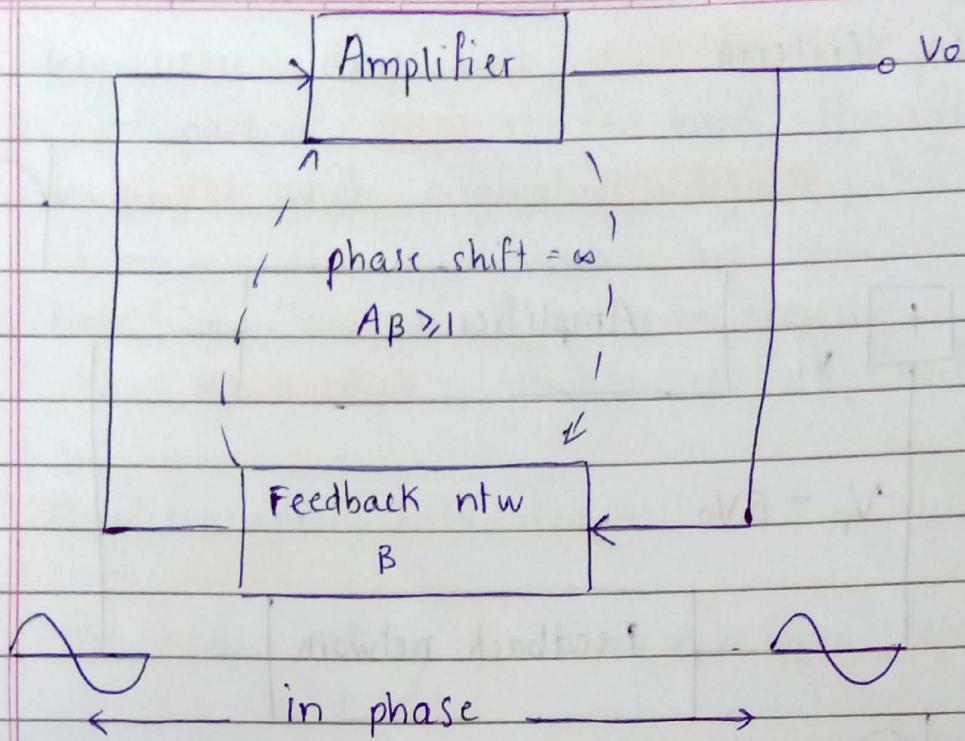
An oscillator will operate at that freq for which the total phase shift introduced, as the signal proceeds from input terminal, through amp' and F.ckt and back again to input precisely  $0^\circ$  or  $360^\circ$  or integral multiple of  $360^\circ$ .

At oscillator frequency,  $|A\beta| \geq 1$

This product is called loop gain

A: Open loop gain voltage

$\beta$ : Feedback factor



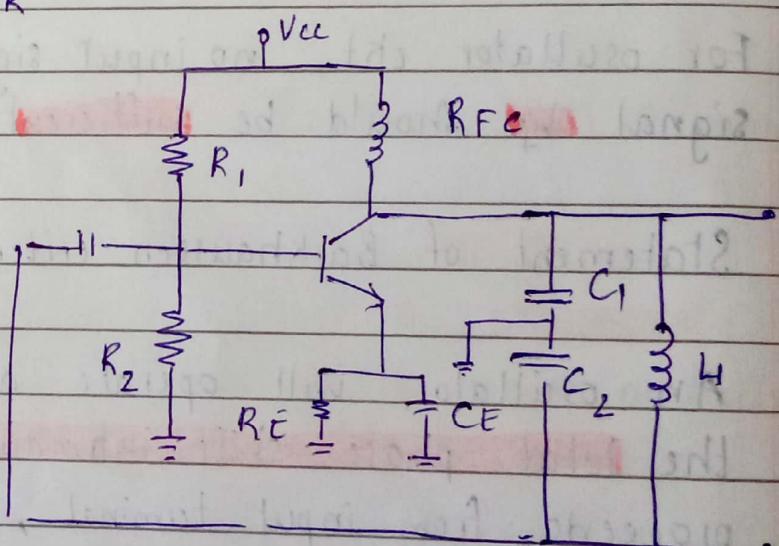
### COLPITT'S OSCILLATOR

Tank ckt:

- use 2 Cs

across a L

- centre of 2 Cs  
is tapped



Frequency of  $\omega$ :

$$\omega = \frac{1}{2\pi \sqrt{LC}}$$

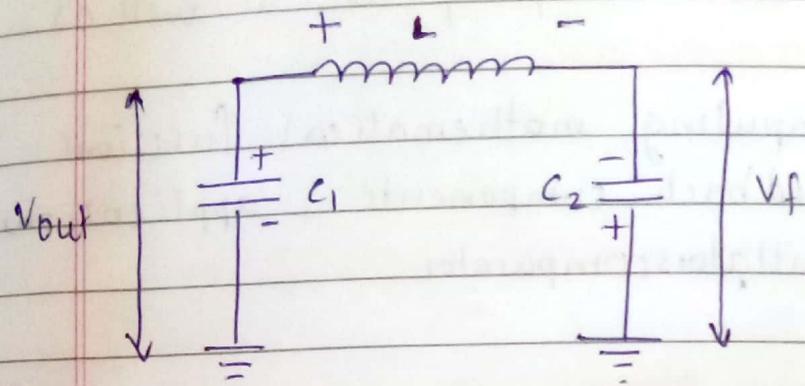
$$C_T = \frac{C_1 C_2}{C_1 + C_2}$$

$C_1 - C_2 - L$  : also a feedback ckt that produces phase shift of  $180^\circ$

Working:

CKT  $\rightarrow$  ON,  $C_1$  and  $C_2$  charged, capacitor discharge through  $L \rightarrow$  oscillations.

$V_{out}$  is developed between  $G$  across  $C_1$  and  $V_f$  is developed across  $C_2$ .



$V_f$  and  $V_{out}$  are  $180^\circ$  out of phase.

$V_f$  provides +ve feedback

Feedback ckt.

Transistor produced  $180^\circ$  phase shift and then further another phase shift of  $180^\circ$  is produced by  $C_1 - C_2$  voltage divider

$\Rightarrow$  undamped oscillations

Feedback factor:

$$\beta = \frac{V_f}{V_{out}} = \frac{X C_2}{X C_1} = \boxed{\frac{C_2}{C_1}}$$

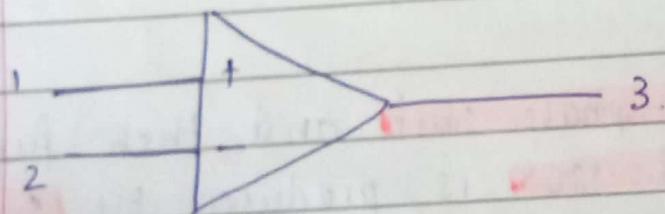
- Circuit
- Frequency formula
- Working: Feedback ckt explanation
- Feedback factor

## OPERATIONAL AMPLIFIER

OP amp:

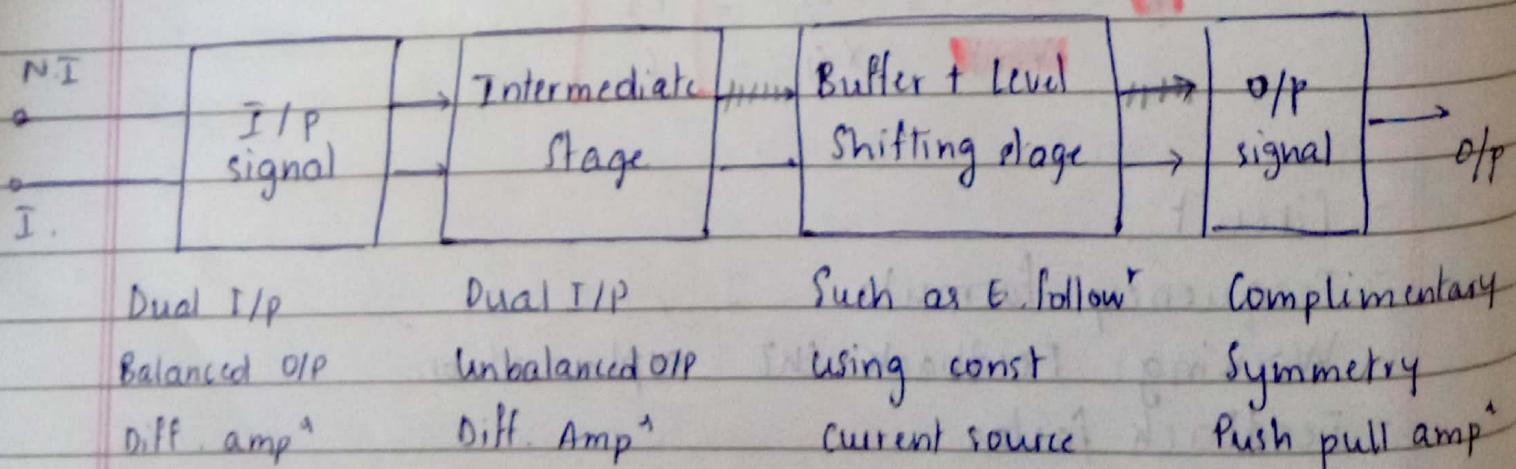
- very high gain differential amplifier with ↑ input impedance and ↓ output impedance.
- can be used to amplify dc as well as ac signal.
- designed for computing mathematical functions.
- + of external feedback components, applications are active filters, oscillators, comparator.

Basic opamp



single ended input, when one is connected to input and other is connected through ground.

Block diagram of op amp.



Function of differential amplifier is to amplify difference between two inputs signals.

#### 1) Input stage

- dual i/p, balanced o/p diff. amp<sup>2</sup>
- provides most of voltage gain of amp<sup>2</sup>.
- establishes i/p resistance of op amp.

#### 2) Intermediate stage

- another diff. amp<sup>2</sup>
- dual i/p, unbalanced o/p diff. amp<sup>2</sup>
- driven by output of first stage

#### 3) Buffer + Level shifting stage

- dc voltage at the output of Inter-stage is  $\neq$  ground potential
- level shifting circuit is used after 2nd stage to shift dc level at output of 2nd stage  $\rightarrow 0$  w.r.t ground
- I/p impedance  $\uparrow \rightarrow$  prevents loading of high gain stage.

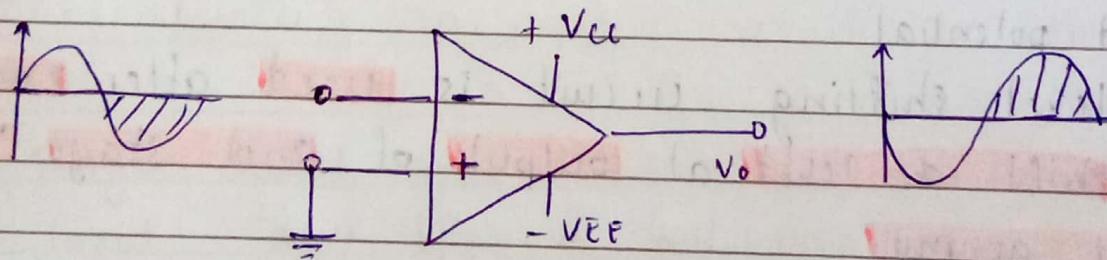
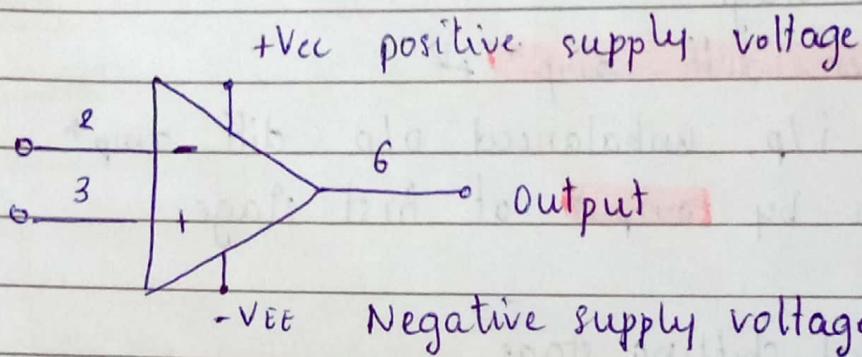
#### 4) Push Pull amplifier output stage.

- provides low impedance
- $\uparrow$  output voltage swing (magnitude of voltage)
- $\uparrow$  current supply capability of op amp
- o/p voltage should swing w.r.t to ground
- the amp<sup>2</sup> is provided with both positive and negative supply.

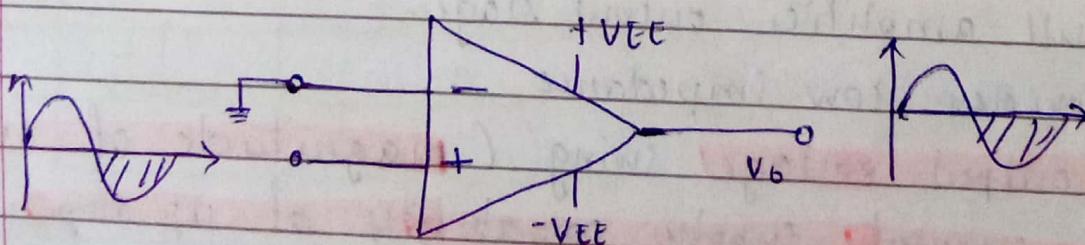
Advantages of op amp over conventional amp.

- smaller size
- reduced cost
- less power consumption
- higher reliability
- easy to replace

Symbols and terminal

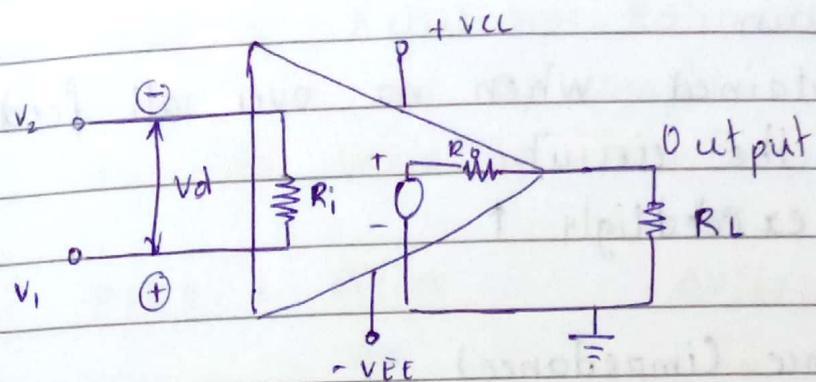


Input signal applied to negative terminal  
⇒ Inverting.



Input signal applied to positive terminal  
⇒ Non inverting.

## Equivalent circuit of OPAMP



$R_i$  = input impedance } **Open loop parameters**  
 $R_o$  = output impedance }

$A_v$  = Open loop gain

- $R_i$  should be **infinite**, practically not possible so it must be very high
- $R_o$  should be **0**, practically not possible, it should be as low as possible
- $A_v$  should be **infinite**, practically not possible it should be as high as possible

$$V_o = A_v \times V_d$$

$$A_v = \frac{V_o}{V_d} = \frac{V_o}{V_1 - V_2}$$

$$V_o = A_v \times (V_1 - V_2)$$

$$V_d = \frac{V_o}{A_v} = \frac{10 \text{ V}}{2 \times 10^5} = 50 \mu\text{V}$$

We need small differential input voltage  $V_d$  to obtain max possible output voltage.

## Characteristics of OP AMP.

### Open loop gain:

- gain obtained when no over all feed back is used in the circuit
- can be exceedingly ↑

### Input resistance. (Impedance)

- determines loading of previous stage
- observed by voltage source between 2 terminals

### Output impedance

- finite series resistance

### Bandwidth.

- frequency range over which the voltage gain of op amp > 70.7% of its max output value.

### Common Mode Rejection Ratio (CMRR)

when 2 i/p voltages  $V_1$  and  $V_2$  are equal, in that case, the output of op amp should be 0

2 input terminals are tied together to one input terminal voltage, output = 0

→ This configuration is also known as common mode rejection ratio

$$PSRR \quad CMRR = \frac{AV}{(dB)} \quad A_{cm}$$

Av: open loop gain

A<sub>cm</sub>: common mode gain

$$= 20 \log_{10} \left[ \frac{AV}{A_{cm}} \right]$$

CMRR: ability to reject common mode signal.

Power Supply Rejection Ratio (PSRR)

- change in an op-amp's input offset voltage ( $V_{ios}$ ) due to variation in the supply voltage.

$$PSRR = \frac{\Delta V_{ios}}{\Delta V}$$

$\Delta V_{ios}$ : Change in input offset voltage

$\Delta V$ : Change in supply voltage.

Degree of dependence of

output due to changes in

Slew rate:

power supply rate.

The maximum rate at which the op amp output of op amp can change with change in ip.

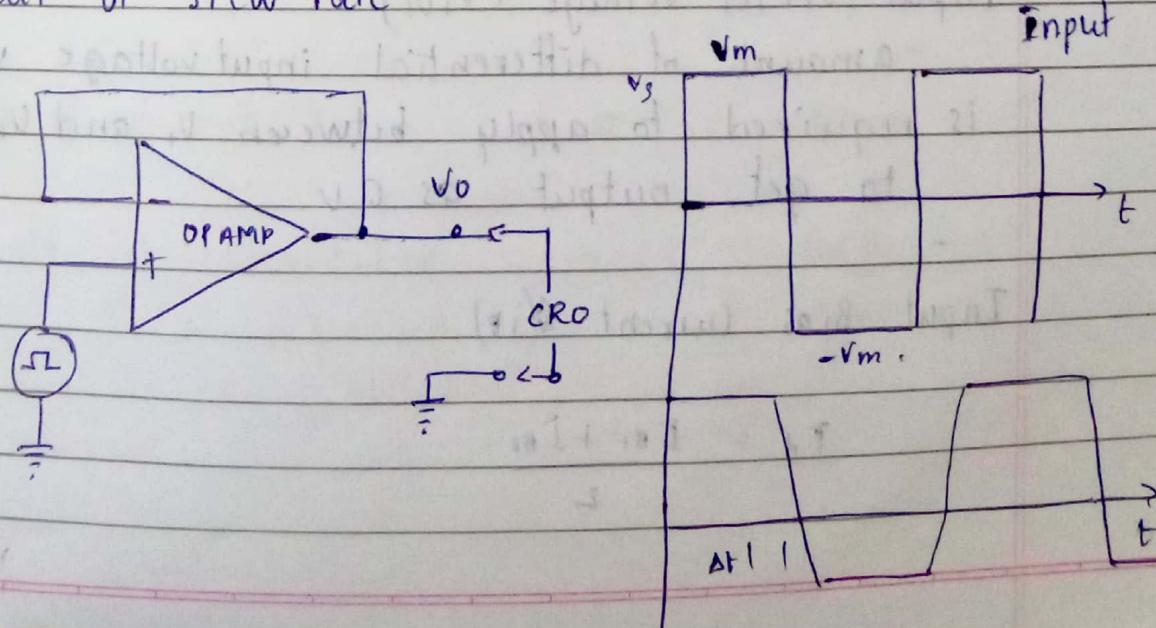
Unit: V/ $\mu$ s

For THT, it's 0.5V/ $\mu$ s.  $\Rightarrow$  cannot use for higher applicat°

Slew rate depends upon how fast the capacitor can charge or discharge.

Value of Slew rate does not change even if output is positive or negative.

Circuit of slew rate



$$\boxed{\text{Slew rate} = \frac{\Delta V_o}{\Delta t}}$$

Frequency and amplitude will affect output

Effect of slew rate on sinusoidal signals

$$V_s = \text{sin wave}$$

$$V_s = V_m \sin \omega t$$

$$V(t) = V_m \sin \omega t$$

$$\frac{dV}{dt} = V_m \times \omega \times \cos(\omega t)$$

Differentiating on both sides.

$$\left| \frac{dV}{dt} \right| = V_m \times 2\pi f \leq SR$$

$$SR \geq V_m \times 2\pi f$$

$\Rightarrow$  ensured that there is no distortion in the output.

$$\boxed{f_{\text{max}} = \frac{SR}{2\pi V_m}}$$

max freq for which the amplifier produces an undistorted output.

Input offset voltage ( $V_{ios}$ )

- amount of differential input voltage which is required to apply between  $V_1$  and  $V_2$  to get output as 0 V

Input Bias Current ( $I_B$ )

$$I_B = \frac{I_{B1} + I_{B2}}{2}$$

Input offset current ( $I_{ios}$ ):

- defined as difference of both current flowing into inverting and non inverting.

Characteristics of Ideal and Practical op amp

Open loop voltage gain  $A_{OL}$       I P  
 $\infty 2 \times 10^5$

Input impedance  $R_i$       I P  
 $\infty 2 M\Omega$

Output impedance  $R_o$       I P  
 $0 75 \Omega$

offset voltage  $V_{ios}$       I P  
 $0 2 mV$

Bandwidth      I P  
 $\infty 1 MHz$

CMRR      I P  
 $\infty 90 dB$

Slew rate      I P  
 $\infty 0.5 V/\mu s$

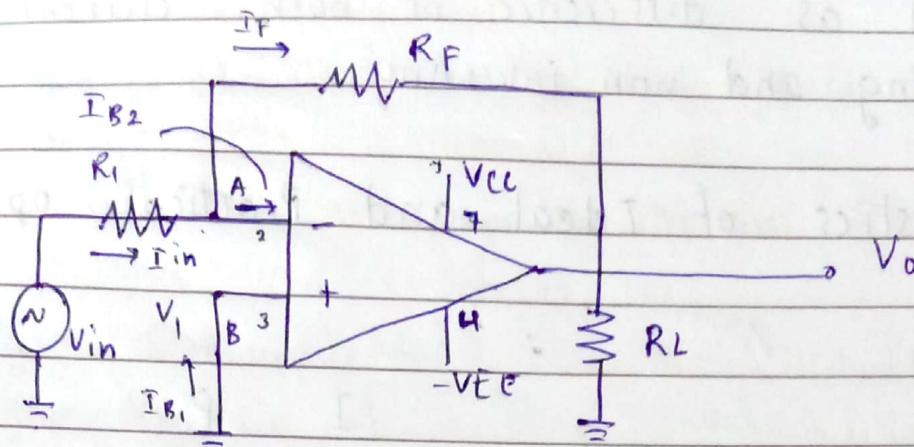
PSRR      I P  
 $0 150 \mu V$

Input bias current  $I_B$       I P  
 $0 50 nA$

Input off set current  $I_{ios}$       I P  
 $0 6 nA$

# CLOSED LOOP CONFIGURATIONS

## Inverting Amplifier



Applying KCL at node A

$$I_{in} = I_{B1} + I_f \quad \text{--- (1)}$$

Since it's an open loop op amp,

$R_i$  is very large hence current = 0

$$I_{B1} = I_{B2} = 0$$

$$I_{in} = I_f \quad \text{--- (2)}$$

$$\frac{V_{in} - V_2}{R_1} = \frac{V_2 - V_o}{R_f} \quad \text{--- (3)}$$

We know the open loop gain  $A_{OL} = \infty$

$$A_{OL} = V_o \times (V_1 - V_2)$$

$$(V_1 - V_2) = \frac{V_o}{\infty} = 0$$

$$V_1 - V_2 = 0$$

$V_1 = 0$  because connected to ground

$V_2 = 0$  also at ground potential

$\Rightarrow$  Virtual ground

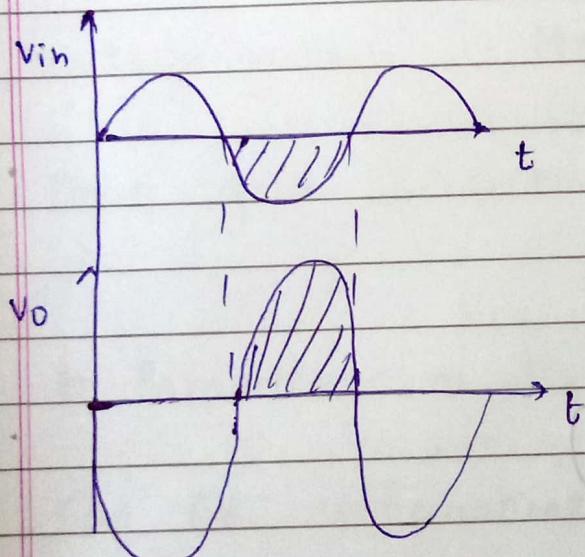
$$\frac{V_{in}}{R_1} = \frac{-V_o}{R_F}$$

$$V_o = -\frac{R_F}{R_1} V_{in} \quad \text{--- (5)}$$

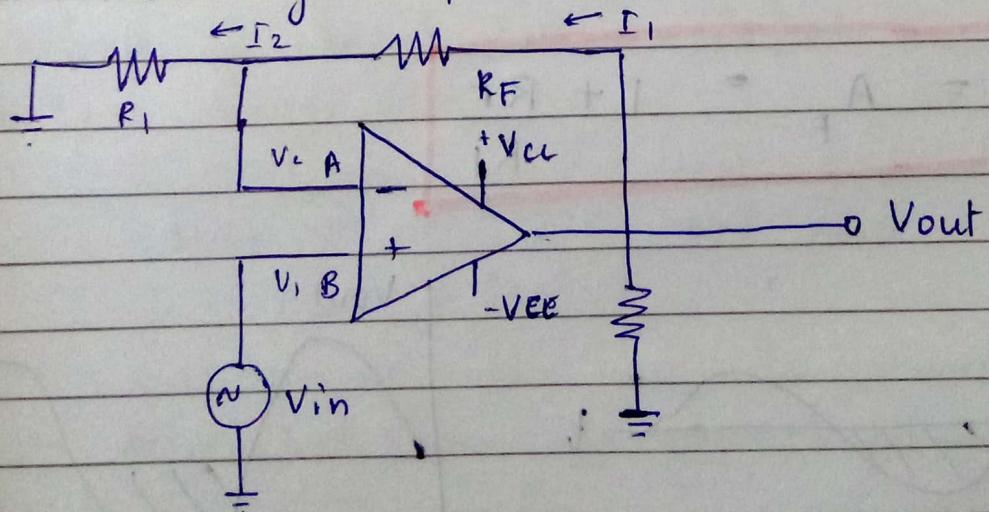
$$\frac{V_o}{V_{in}} = \frac{-R_F}{R_1}$$

$$A_{ot} = \frac{-R_F}{R_1} \quad \text{--- (6)}$$

Waveforms of inverting amplifier



Non inverting amplifier



# Applying KCL at node A

$$I_1 = I_2$$

$$I_1 = \frac{V_o - V_2}{R_F} \quad \text{--- (1)}$$

$$I_2 = \frac{V_A - 0}{R_1} \quad \text{--- (2)}$$

$$V_A = V_B = V_{in}$$

Virtual ground

$$\frac{V_o - V_A}{R_F} = \frac{V_A}{R_1}$$

$$\frac{V_o - V_{in}}{R_F} = \frac{V_A}{R_1}$$

$$\frac{V_o}{R_F} = \frac{V_{in}}{R_F} + \frac{V_{in}}{R_E}$$

$$\frac{V_o}{R_F} = V_{in} \left( \frac{1}{R_F} + \frac{1}{R_E} \right)$$

$$\frac{V_o}{V_{in}} = R_F \left( \frac{R_1 + R_F}{R_1 R_F} \right)$$

$$\boxed{\frac{V_o}{V_{in}} = A_F = 1 + \frac{R_F}{R_1}}$$

