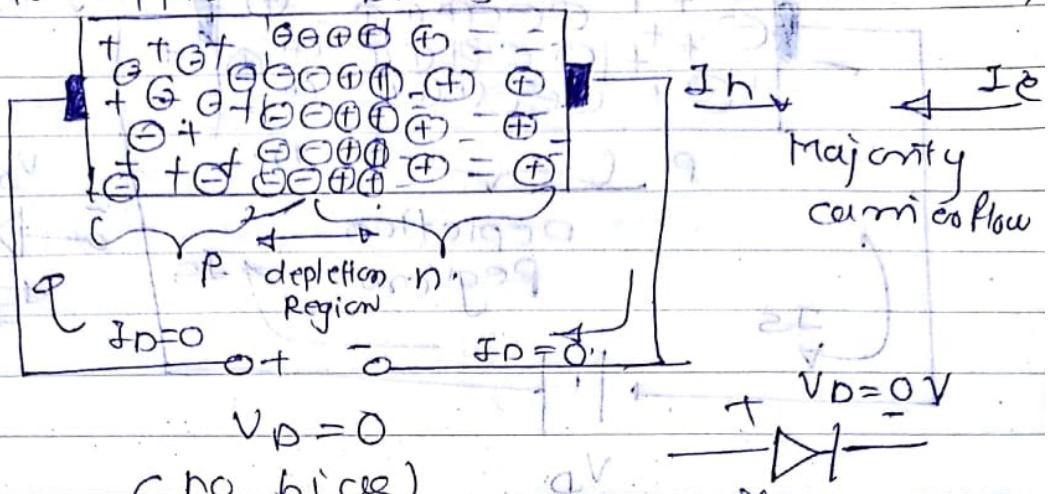


Minority carrier flow

## Semiconductor diode

① No applied bias.



(no bias)

switch behavior to read  $I_D = 0mA$ .

When two pieces of p-type and n-type are joined, the electron-hole pairs of the junction will combine, resulting in a lack of free carriers near the junction.

This is called a depletion region. Due to the "depletion" of free carriers in the region, it acts as an insulator.

The diagram shows the depletion region.

The region where no carriers are present is called a depletion region. Due to the "depletion" of free carriers in the region, it acts as an insulator.

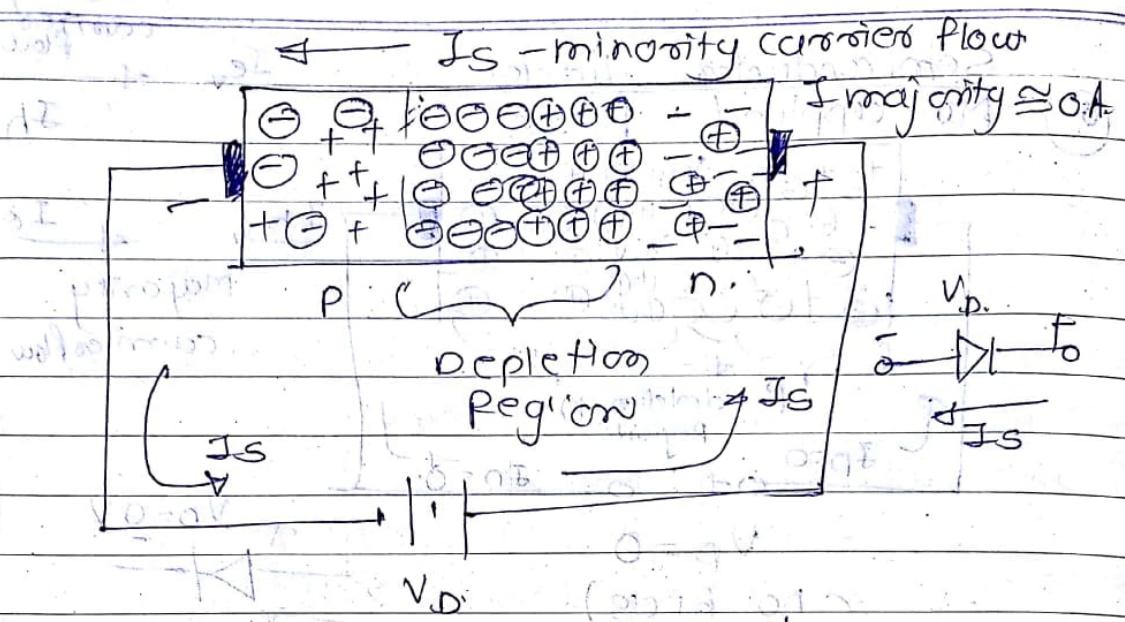
Reverse Bias: If an applied voltage is zero volts and the resulting current is  $0A$ , much like a resistor.

positive terminal is connected to the n-type material & negative terminal is connected to p-type material.

Reverse bias condition ( $V_D < 0V$ )

Positive terminal is connected to the n-type material & negative terminal is connected to p-type material as shown in the diagram.

Note that the positive terminal is connected to the n-type material & negative terminal is connected to the p-type material.

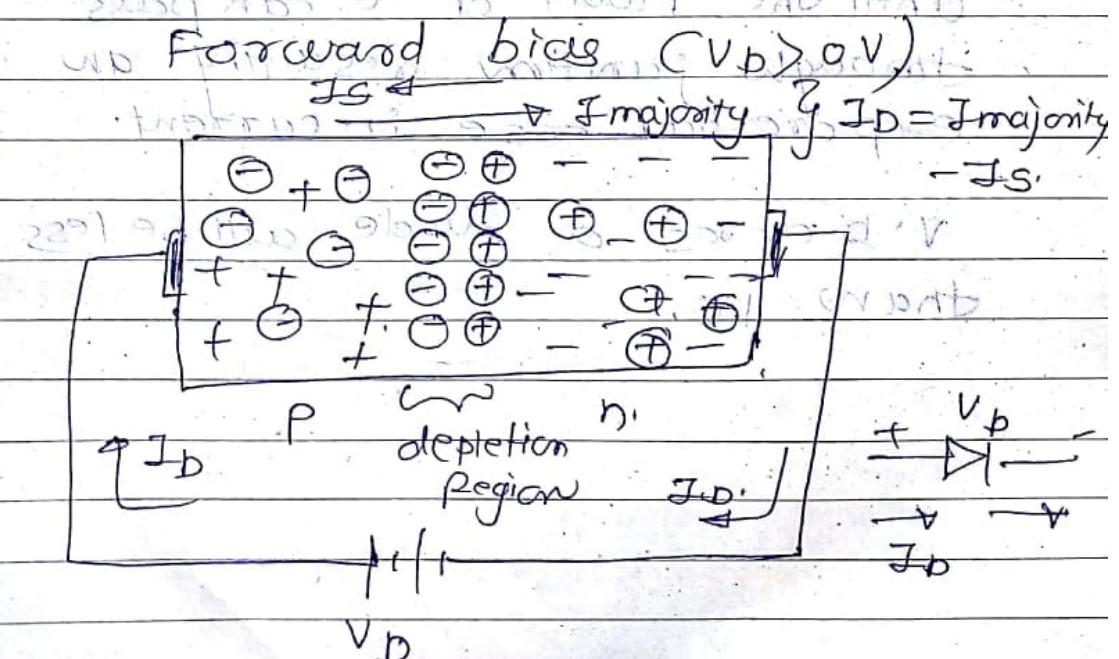
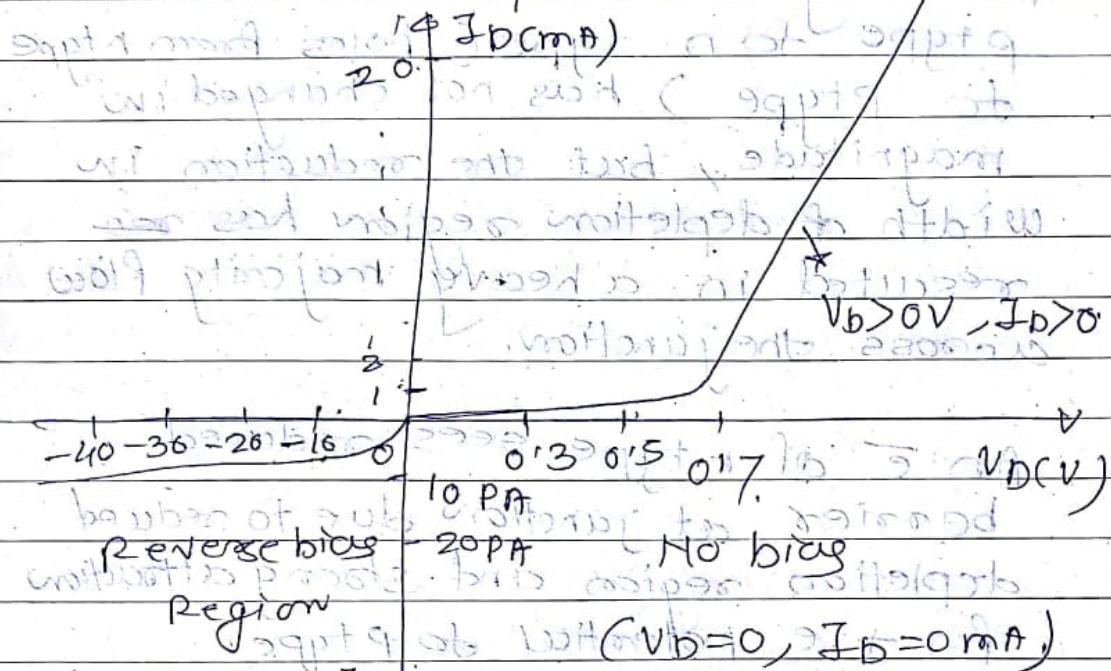


The number of uncovered positive ions in the depletion region of the n-type material will increase due to the large number of free electrons drawn to the positive potential of the applied voltage.

For similar reasons, the number of uncovered negative ions will increase the increase in p-type material. The net effect, therefore, is widening of the depletion region. This widening of depletion region will establish too great a barrier for the majority carriers to overcome, effectively reducing the majority carrier flow to zero as shown.

The number of minority carriers, however entering the depletion region will not change, resulting in minority carrier flow. Vectors of the same magnitude as indicated in case 1.

Reverse bias -  $V_B < 0$   
 Forward bias -  $V_B > 0$   
 The current exists under reverse bias condition is called reverse saturation current  $I_S$  in diode at zero  
 Saturation means it reaches its maximum level quickly and does not change significantly with  $V_B$  in reverse bias potential.



1906 ~~1906~~ - Triode by Fleming. ①  
1930 = tetrode and pentode

## Bipolar junction transistor.

A bipolar junction transistor is a three terminal semiconductor device in which the operation depends on the interaction of both majority and minority carriers and hence the name Bipolar \*

(Bell Laboratory) Dr Bardeen, Pr Brattain

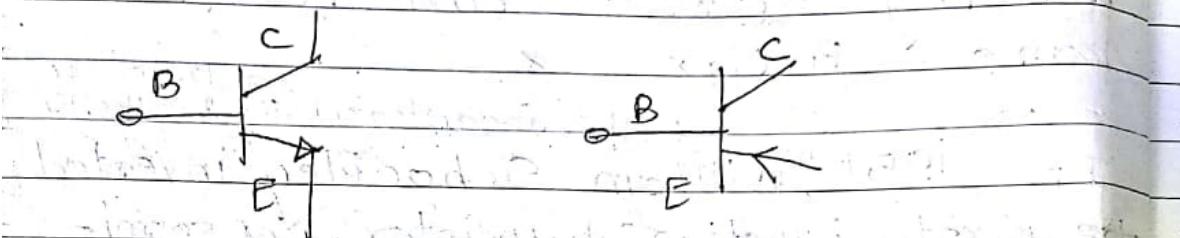
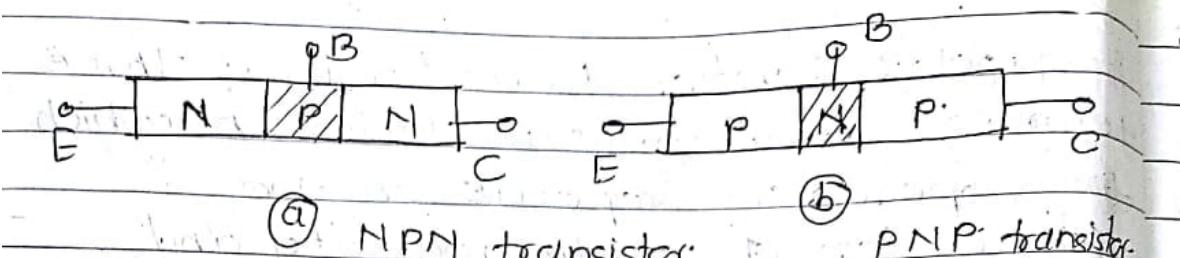
In 1951 Dr William Shockley invented the first junction transistor, a semiconductor device that can amplify electronic signals such as radio and television signals.

It is essential ingredient of every electronic circuit from the simplest amplifier or oscillator to the most elaborate digital computer. Thus a proper understanding of transistor is very important. active filters, multivibrators, op-amp

Before transistor, the amplification was achieved by using vacuum tubes as an amplifier. Nowadays, vacuum tubes are replaced by transistor because of the following advantages of transistors.

- Low operating voltage
- Higher efficiency
- Small size and ruggedness
- Does not require any filament power

## Construction



The BJT consists of a silicon (or germanium) crystal in which thin layer of N type silicon is sandwiched between two layers of P type silicon. This transistor is referred to as PNP.

Alternatively, in a NPN transistor, a layer of P type material is sandwiched between two layers of N type material.

Three portions of the transistor are emitter, base and collector.

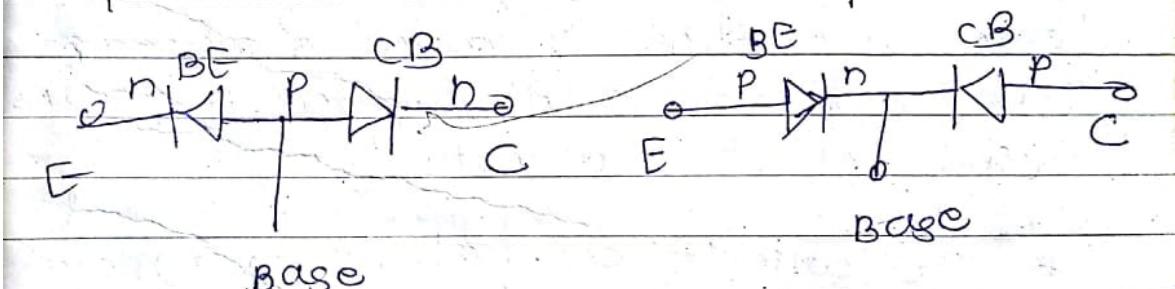
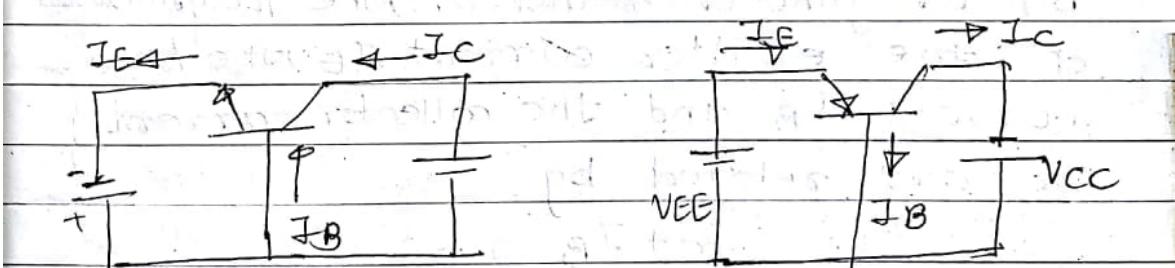
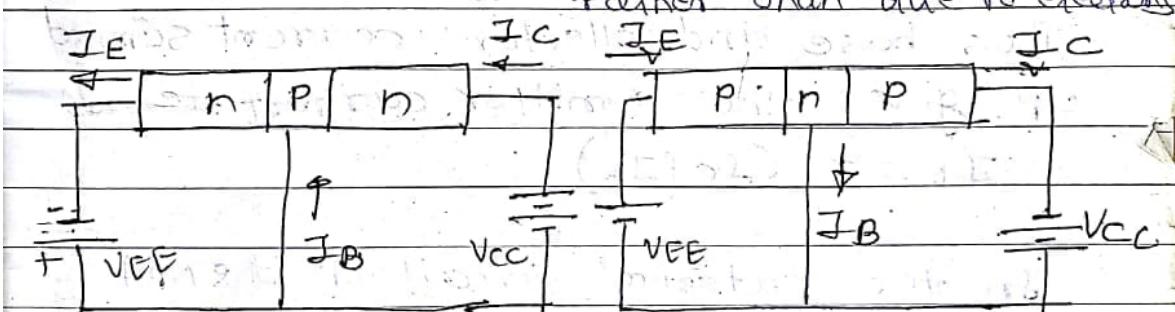
The arrow on the emitter specifies the direction of current flow when EB (emitter base) junction is forward biased.

(3)

Emitter is heavily doped so that it can inject a large number of charge carriers into the base.

Base is lightly doped and very thin. It passes most of the injected charge carriers from the emitter into the collector. Collector is moderately doped.

\* Current directions refers to conventional flow of current (i.e. due to hole) rather than due to electrons.



\* BJT is active device. amplification in the transistor is achieved by passing input current signal from a region of low resistance to a region of high resistance. This concept of transfer of resistance has given the name TRANSFER RESISTOR (TRANSISTOR).

## Operation of NPN transistor

As shown in Fig forward bias is applied to the emitter base junction. It causes a lot of electrons from emitter region to crossover to the base region.

As the base is lightly doped with P type impurity, the number of holes in the base region is also very small. Hence a few electrons combine with holes to constitute a base current  $I_B$ . The remaining electrons (more than 95%) crossover into the collector current  $I_C$ .

(Crosses  
reverse biased)

Thus base and collector current summed up gives the emitter current i.e.

$$I_E = I_C + I_B$$

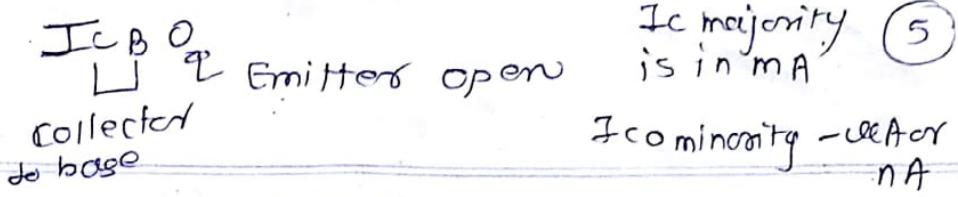
In the external circuit of the NPN bipolar junction transistor, the magnitudes of the emitter current  $I_E$ , the base current  $I_B$  and the collector current  $I_C$  are related by

$$I_E = I_C + I_B$$

(Base current is of order of microamperes as compared to milliamperes for emitter and collector currents)

\* The collector current however comprises two components—the majority and the minority carriers. The minority current component is called the leakage current  $I_{CBO}$ .

$$I_C = I_{C \text{ majority}} + I_{CBO \text{ minority}}$$



### Operation of PNP transistor:

Forward bias is applied to EB junction of PNP transistor. It causes a lot of holes from emitter region to crossover to the base region. As the base is lightly doped with N type impurities, the number of electrons in the base region is very small and hence the number of holes combined with electrons in the N type base region is also very small. Hence a few holes combined with electrons to constitute a base current  $I_B$ . The remaining holes (more than 95%) crossover into the collector region to constitute a collector current  $I_C$ . Thus one collector current and base current when summed up gives the emitter current i.e  $I_E = -(I_C + I_B)$

In the external circuit of PNP bipolar junction transistor, the magnitudes of  $I_B$ ,  $I_C$  and  $I_E$  are related by

$$I_E = I_C + I_B \quad \text{①}$$

Reverse saturation current  $I_{C0}$  or  $I_{cBO}$ :

- It is the current flowing through reverse biased collector base junction i.e collector to base leakage current with emitter open. A magnitude of  $I_{cBO}$  is negligible compared to  $I_E$ .

$$I_E = I_C + I_B \quad \text{--- } \textcircled{1}$$

This equation gives the fundamental relationship between the currents in a bipolar transistor circuit.

Also this fundamental equation shows that there are current amplification factors  $\alpha$  and  $\beta$  in common base transistor configuration and common emitter transistor configuration respectively for static (dc) currents and for small changes in currents.

Large signal current gain ( $\alpha$ ) of a common base transistor is defined as the ratio of the negative of the collector current increment to the emitter current change from cut-off ( $I_E = 0$ ) to  $I_E$ .

$$\alpha = - \frac{(I_C - I_{CBO})}{I_E} \quad \text{--- } \textcircled{2}$$

or

$$\alpha_{ac} = \frac{\partial I_C}{\partial I_E} \quad \text{V_{ce} = constant}$$

Where the  $I_{CBO}$  (or  $I_{CO}$ ) is the reverse saturation current flowing through reverse biased collector-base junction i.e. the collector to base leakage current with emitter open. As the magnitude of  $I_{CBO}$  is negligible when compared to  $I_E$ , the above expression can be written as.

$$\alpha = \frac{I_C}{I_E} \quad \text{--- } \textcircled{3}$$

(7)

since  $I_C$  and  $I_E$  are flowing in opposite directions,  $\alpha$  is always positive

Typical value of  $\alpha$  ranges from 0.90 to 0.995.

Also  $\alpha$  is not constant but varies with emitter current  $I_E$ , collector voltage  $V_{CB}$  and temperature.

for CB current gain  $< 1$   
 CE current gain high (20 to few hundreds)

\* \* back from ~~next page~~ Transistor currents  
 $I_E = I_C + I_B \rightarrow (1)$   
 $I_C = \alpha_{dc} I_E \rightarrow (2) \quad \text{fig (a)}$

$\alpha_{dc} = \frac{I_C}{I_E}$ , emitter to collector  
 common base  $\alpha_{dc}$  current gain  
 Numerically  $\alpha_{dc}$  is 0.96 to 0.995  
 so  $I_C \approx I_E$

CB junction is reverse biased, very small reverse saturation current  $I_{CBO}$  flows. Collector to base leakage current very small hence ignored.

put eqn (1) into eqn (2)

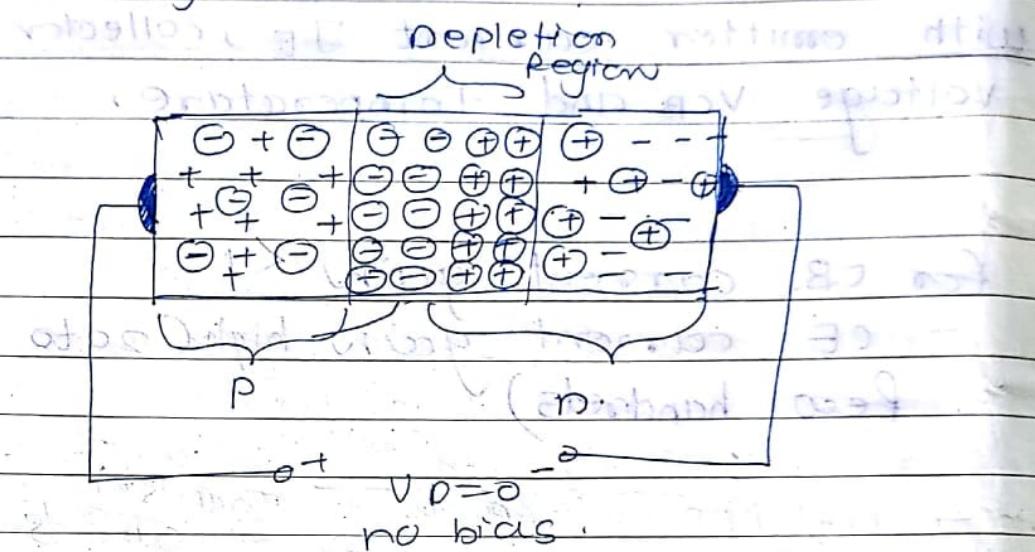
$$I_C = \alpha_{dc}(I_C + I_B) \rightarrow (3)$$

which gives  $I_C = \frac{\alpha_{dc} I_B}{1 - \alpha_{dc}} \rightarrow (4)$

$$I_C = \beta_{dc} I_B \rightarrow (5) \quad \text{where } \beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} \rightarrow (6)$$

Where  $\beta_{dc}$  is base to collector current gain or ratio of collector current to base current.  
 $\beta_{dc} = I_C / I_B$  from eqn 5 Typically  $\beta_{dc}$  ranges from 25 to 300

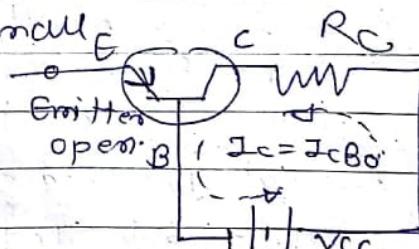
Depletion Region → When two common emitter P and N materials are combined, the joined, electrons and holes in current will combine, resulting in a lack of free carriers in the region near the junction, as shown.



only particles displayed in this region are the positive and negative ions remaining once the free carriers have been absorbed.

$I_{CBO}$  is negligibly small  
 $\therefore I_C \approx \alpha_{dc} I_E$

$$\alpha_{dc} = \frac{I_E}{I_C}$$



$I_{CBO}$   
 $\downarrow$  open  
 Collector to Emitter  
 base current

$I_{CBO}$  is collector to base leakage current with  
 Open emitter

## BJT configuration.

When transistor is to be connected in a circuit, one terminal is used as input terminal, the other terminal is used as an output terminal and the third terminal is common to the input and output. Depending upon the input, output and common terminal, transistor can be connected in three configurations. They are:

CB - common base configuration.

CE - common Emitter configuration.

CC - common collector configuration.

CB - common Base configuration.

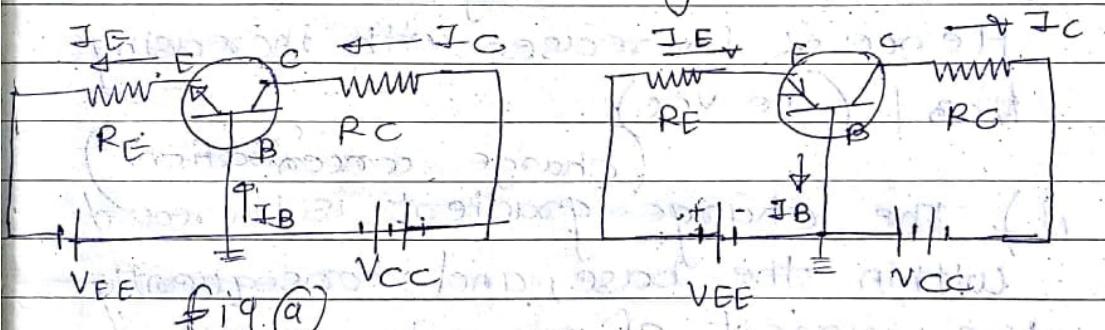


fig. @

This is also called grounded base configuration. In this configuration, emitter is input terminal, collector is the output terminal and base is the common terminal.

$$I_C = \alpha_{dc} I_E + I_{CBO}$$

\* \* \* see back page

Reverse saturation current  $I_{CBO}$  is temperature sensitive and doubles for every  $10^\circ C$  rise in temperature.

where  $\alpha_{dc} = \frac{I_C}{I_E}$  = CB short cct, amplification factor.

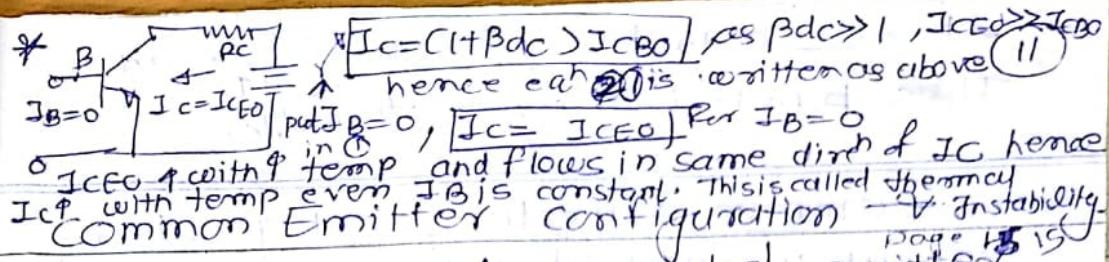
\* when  $I_E (Z/P) = 0 \text{ mA}$ ,  $I_C = I_{CBO}$ .

## Early effect or base width modulation

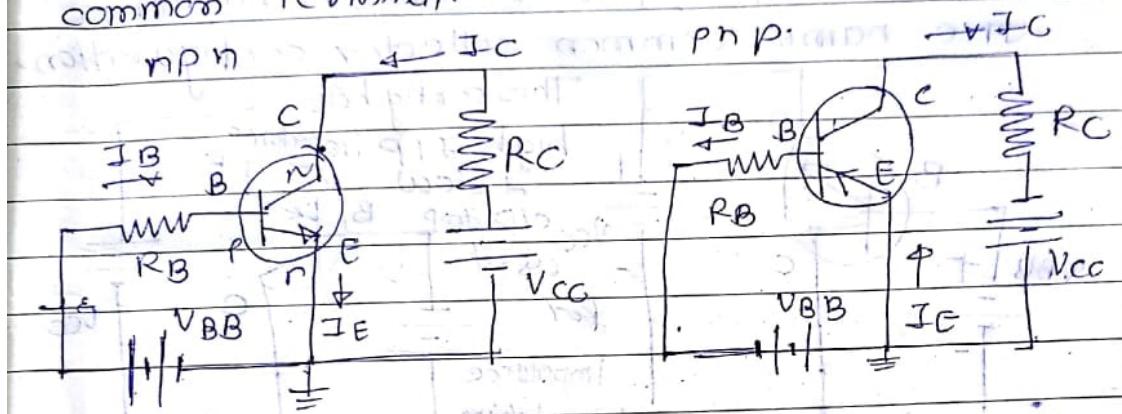
As the collector voltage  $V_{CC}$  is made to increase the reverse bias, the space charge width between collector and base tends to increase, with the result that the effective width of the base decreases. This dependency of base-width on collector-to-emitter base voltage is known as the early effect. This decrease in effective width has three consequences.

- i) There is less chance for recombination within the base region,  $I_B$  hence  $I_C$ . Hence  $\alpha$  increases with increasing  $V_{CB}$  (ie  $V_{CE}$ ).  
(charge concentration)
- ii) The charge gradient is increased within the base, and consequently the current of minority carriers injected across the emitter junction increases. (because of less recombination)
- iii) For extremely large voltages, the effective base-width may be reduced to zero, causing voltage breakdown in the transistor. This phenomenon is called the punch through.

A large current will flow to generate excessive heat to damage the transistor.



This is also called (grounded) emitter configuration. In this configuration base is the input terminal, collector is the output terminal and the emitter is the common terminal.



Bias voltage  $V_{BB}$  forward biases the base-emitter junction and  $V_{CC}$  is used to reverse bias the collector-base junction.

(This eqn is derived from  $I_C = \beta_{dc} I_B + I_{CEO}$ )

$$I_C = \beta_{dc} I_B + [1 + \beta_{dc}] I_{CEO} \quad (1)$$

$$\text{where } \beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} \quad (2)$$

The term  $(\beta_{dc} + 1) I_{CEO}$  is the reverse leakage current in common emitter configuration. It is designated as  $I_{CEO}$ .

$$I_{CEO} = (1 + \beta_{dc}) I_{CB0} \quad (3)$$

Neglecting  $I_{CB0}$  we have

$$I_C = \beta_{dc} I_B \quad \text{and} \quad I_E = I_B + I_C = (1 + \beta_{dc}) I_B \quad (4)$$

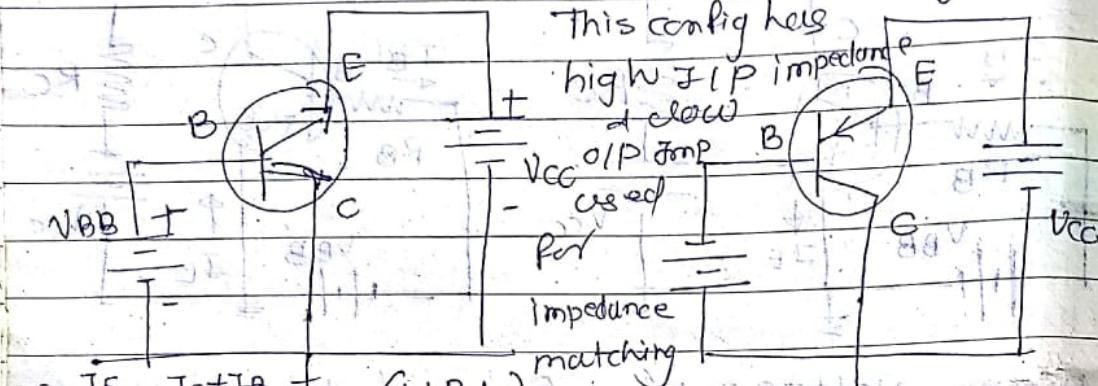
$I_{CEO}$  collector to emitter current when base is open

$$I_f \alpha_{dc} = 0.99 \text{ then } \beta_{dc} = \frac{0.99}{1-0.99} = 99$$

Thus  $\beta_{dc}$  is much higher than  $\alpha_{dc}$ .

### Common collector configuration.

Input is applied between base and collector, and the o/p is taken from emitter and collector. Here collector of the transistor is common to both input and output circuits, and hence the name common collector configuration.



$$r_{oJIP} = \frac{V_{CC}}{I_B} = \frac{I_C + I_B}{I_B} = (1 + \beta_{dc})$$

Comparison of Transistor Configuration

Sr No	Config	JIP	OIP	CE	CC
01	JIP Resistance	Very low ( $< 10^{-2}$ )	Low ( $10^2$ )	High ( $500k\Omega$ )	High ( $500k\Omega$ )
02	OIP Resistance	Very high ( $> 1M\Omega$ )	High ( $10^4 k\Omega$ )	Low ( $50\Omega$ )	Low ( $50\Omega$ )
03	JIP Current	$I_E$	$I_B$	$I_B$	$I_B$
04	OIP Current	$I_C$	$I_C$	$I_E$	$I_E$
05	JIP Voltage applied	Emitters & collector w.r.t. base	Base & emitter	Base & collector	Base & collector
06	OIP Voltage	base	collector & emitter	Emitters & collector	Emitters & collector
07	Current amplification factor	$\alpha_{dc} = \frac{I_C}{I_E}$	$\beta_{dc} = \frac{I_C}{I_B}$	$\frac{I_E}{I_B} = \gamma_{dc}$	
08	current gain less than 1	High ( $20$ to $200$ )	High ( $20$ to few hundreds)	High ( $20$ to few hundreds)	
09	Voltage gain	Medium ( $150$ )	Medium ( $50$ )	Low ( $1$ )	
10	Applications phase shift	As a JIP stage of multistage amplifier	For audio signal amplification	for impedance matching	No.

Relationship b/w  $\alpha_{dc}$  &  $\beta_{dc}$ .

$$\alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}} \text{ and } \beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}} \quad | \quad \gamma_{dc} = (1 + \beta_{dc})$$

13

Why CE configuration is widely used in amplifier circuits?

Ans. →

- ① The CE config is the only config which provides both voltage as well as current gain greater than unity. In case of CB config current gain is less than unity and in case of CC config voltage gain is less than unity. The power gain is a product of voltage gain and current gain. CE config provides voltage gain nearly equal to voltage gain provided by CB config (Voltage gain is maximum in CB) & current gain nearly equal to current gain provided by CC config (current gain is maximum in CC).

Thus the power gain of CE config is much greater than the power gain provided by the other two configurations (Voltage gain in CC and current gain in CB are less than unity).

- ② In CE circuit the ratio of o/p resistance to input resistance is small, may range from 10 to 100. This makes the config. an ideal for coupling between various transistor stages. However, in other connections, the ratio of o/p resistance to I/P resistance is very large.

## Transistor Applications → ① Amplifiers

- ② Switching circuits
- ③ Oscillators
- ④ Waveshaping circuits
- ⑤ Logic circuits
- ⑥ Timers and multivibrators
- ⑦ Delay circuits

Large and hence coupling becomes highly insufficient due to large mismatch of resistance.

## Operating Point:

Region of operation	Emitter Base Junction	Collector Base Junction
(as a openswitch) <u>Cut off</u>	Reverse Biased	Reverse Biased
Active (amp)	Forward Biased	Reverse Biased
Saturation (as a closeswitch)	Forward Biased	Forward Biased

## Operating Regions and Bias conditions:

In order to operate transistor in the desired region we have to apply external dc voltages of correct polarity and magnitude to the two junctions of the transistor. This is nothing but the biasing of the transistor.

Because dc voltages are used to bias the transistor, biasing is known as dc biasing of the transistor.

When we bias a transistor we establish a certain current and voltage conditions for the transistor. These conditions are known as operating conditions or dc operating point or quiescent point.

④ This  $\beta$  temp of CB junction. Transistor has negative resistor temp coeff of resistivity, hence reduces resistance. Reduced resistance will increase  $I_c$  further.

The operating point shifts with changes in transistor parameters such as  $\beta$ ,  $I_{CO}$  and  $V_{BE}$ .

As the transistor parameters are temp dependent, the operating point also varies with changes in temperature.

For every  $10^\circ\text{C}$  rise in temp,  $I_{CO}$  doubles itself. When  $I_{CO}$  increases,  $I_c$  increases significantly. This causes power dissipation in CB junction to increase and hence to make  $I_{CO}$  increase. This will cause  $I_c$  to increase further and the process becomes cumulative which will lead to thermal runaway that will destroy the transistor.

\* In addition, the quiescent operating point can shift due to temperature changes and transistor can be driven into the region of saturation.

\* To establish the operating point in the active region, compensation techniques are needed.

\* The collector is normally made larger in size than the emitter in order to help dissipate the heat developed at the collector junction.

$\beta$  - increases with  $\beta$  in temp

$V_{BE}$  - decreases about  $2.5 \text{ mV}$  per degree Celsius increase in temp

$I_{CO}$  - doubles for every  $10^\circ\text{C}$  rise in temp

## Stability Factor (S)

The extent to which the collector current  $I_C$  is stabilised with varying  $I_{CO}$  is measured by stability factor  $S$ .

It is defined as rate of change of collector current  $I_C$  with respect to the collector-base leakage current  $I_{CO}$ . Keeping both the currents  $I_B$  &  $I_C$  constant at  $\beta I_B$ .

$$WOS = \frac{dI_C}{dI_{CO}} = \frac{\beta dI_C}{\beta dI_{CO}} = \frac{dI_C}{dI_{CO}} \text{ const} \quad \text{v1}$$

CE amp

$$I_C = \beta I_B + (1+\beta) I_{CO} \quad \text{v2}$$

$$\frac{dI_C}{dI_{CO}} = \frac{\beta dI_B}{dI_{CO}} + (1+\beta) \frac{dI_{CO}}{dI_{CO}} = (1+\beta) \quad \text{v3}$$

$$\left( \frac{1-\beta dI_B}{dI_C} \right) = (1+\beta)$$

$$S = \frac{1+\beta}{1-\beta \left( \frac{dI_B}{dI_C} \right)} \quad \text{v3}$$

From eqn (3) it is clear that factor  $S$  should be as small as possible to have better thermal stability.

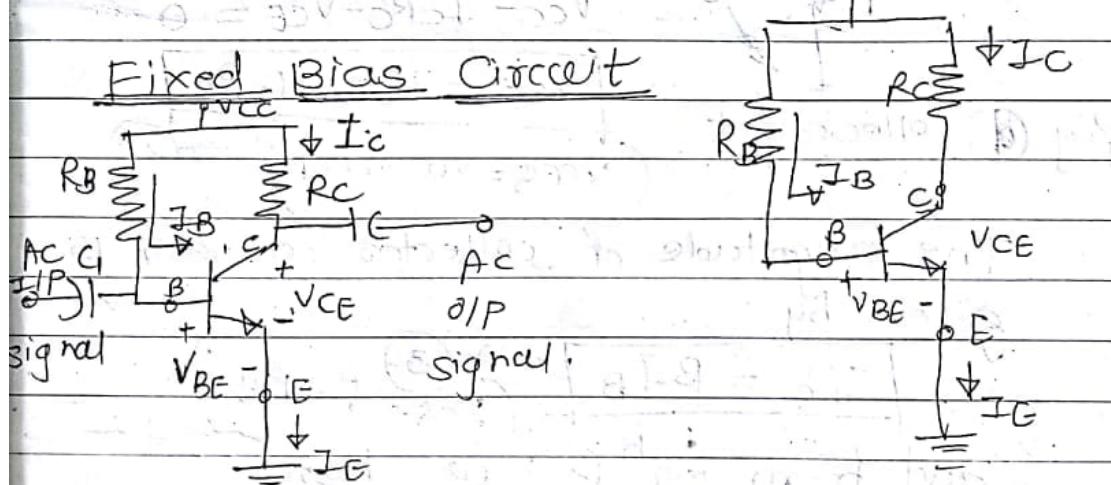
(17)

stability factor  $s'$  &  $s''$  $s'$  is defined as the rate of change of  $I_C$  with  $V_{BE}$  keeping  $I_{CO} + \beta$  constant

$$s' = \frac{\partial I_C}{\partial V_{BE}} = \frac{\partial I_C}{\partial V_{BE}} \rightarrow (4) \quad I_{CO} + \beta \text{ constant}$$

 $s''$  is defined as the rate of change of  $I_C$  with respect to  $\beta$  keeping  $I_{CO} + V_{BE}$  constant

$$s'' = \frac{\partial I_C}{\partial \beta} = \frac{\partial I_C}{\partial \beta} \rightarrow (5) \quad I_{CO} + V_{BE} \text{ constant}$$



(a) Fixed Bias circuit (b) DC eq v of fig (a)

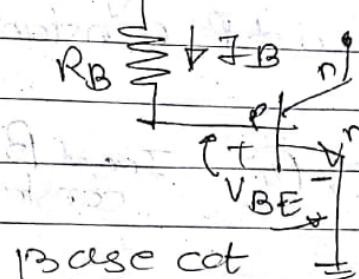
It is the simplest dc bias config.

For the dc analysis we can replace capacitor with an open circuit because the reactance of capacitor for dc is

$$X_C = \frac{1}{2\pi f_C} = \frac{1}{2\pi f(0)C} = \infty$$

## Circuit Analysis

(a)  $V_{CC}$



Base circuit as shown  
in Fig. (3)

Apply KVL

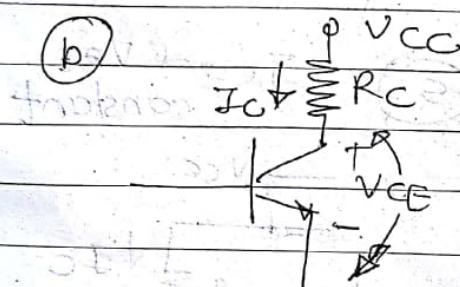
base cat

$$V_{CC} - I_B R_B - V_{BE} = 0$$

fig (3)

$$\begin{cases} I_B = \frac{V_{CC} - V_{BE}}{R_B} \\ (I_{BG}) \end{cases} \rightarrow 1$$

(b)



Applying KVL

fig (4) collector cat.

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$\begin{cases} V_{CE} = V_{CC} - I_C R_C \\ (V_{CG} = V_{CC} - I_C R_C) \end{cases} \rightarrow 2$$

The magnitude of collector current is given by

$$\begin{cases} I_C = \beta I_B \\ (I_{CG} = \beta I_B) \end{cases} \rightarrow 3$$

and from eq. (2) we have

$$\begin{cases} I_C = \frac{V_{CC} - V_{CE}}{R_C} \\ \end{cases} \rightarrow 4$$

It is important to note that since the base current is controlled by the value of  $R_B$  and

$I_c$  is related to  $I_B$  by a constant  $\beta$ , the magnitude of  $I_c$  is not a function

(19)

of resistance  $R_C$ . changing  $R_C$  to any level will not affect the level of  $I_B$  or  $I_C$  as long as we remain in the active region of the device. However change in  $R_C$  will change the value of  $V_{CE}$ .

$$V_{CE} = V_C - V_E \quad , V_C = \text{Collector Voltage}$$

→ (5)  $V_E = \text{Emitter Voltage}$

$$\text{Hence } V_B = V_E \quad , V_B = \text{Base voltage}$$

→ (6)  $V_E = \text{Emitter Voltage}$

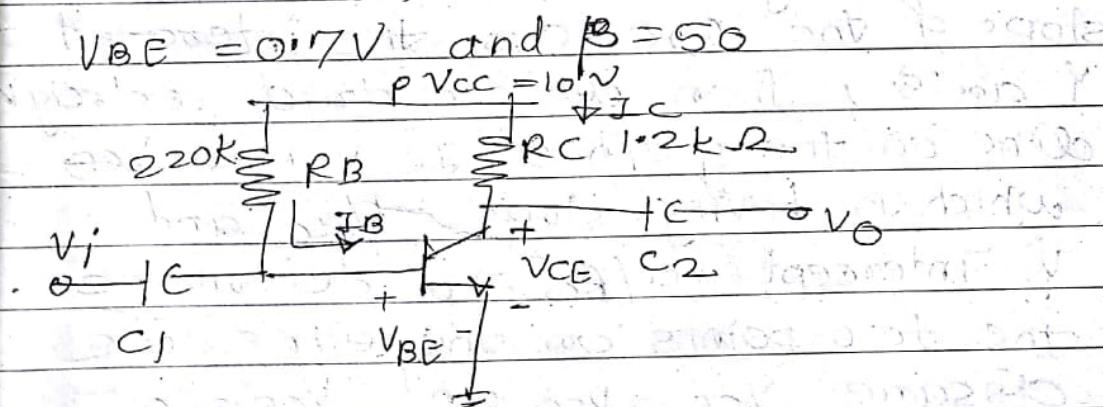
Hence  $V_E = 0$

$$V_{BE} = V_B \quad → (7)$$

$$V_{CE} = V_C \quad → (8)$$

problem

For the circuit shown in Fig calculate  $I_B$ ,  $I_C$ ,  $V_{CE}$ ,  $V_B$ ,  $V_C$  and  $V_{BC}$ . Assume  $V_{BE} = 0.7\text{V}$  and  $\beta = 50$



$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{10 - 0.7}{220 \times 10^3} = 42.27 \mu\text{A}$$

$$I_C = \beta I_B = 50 \times 42.27 \times 10^{-6} = 2.1135 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C = 10 - 2.1135 \times 10^{-3} \times 1.2 \times 10^3 = 7.4638 \text{ V}$$

$$V_B = V_{BE} = 0.7$$

$$V_C = V_{CE} = 7.4638 \text{ V}$$

$$V_{BC} = V_B - V_C = 0.7 - 7.4638 \\ = -6.7638$$

The negative voltage  $V_{BC}$  indicates that base-collector junction is reverse biased.

### Load Line Analysis

For fixed bias set

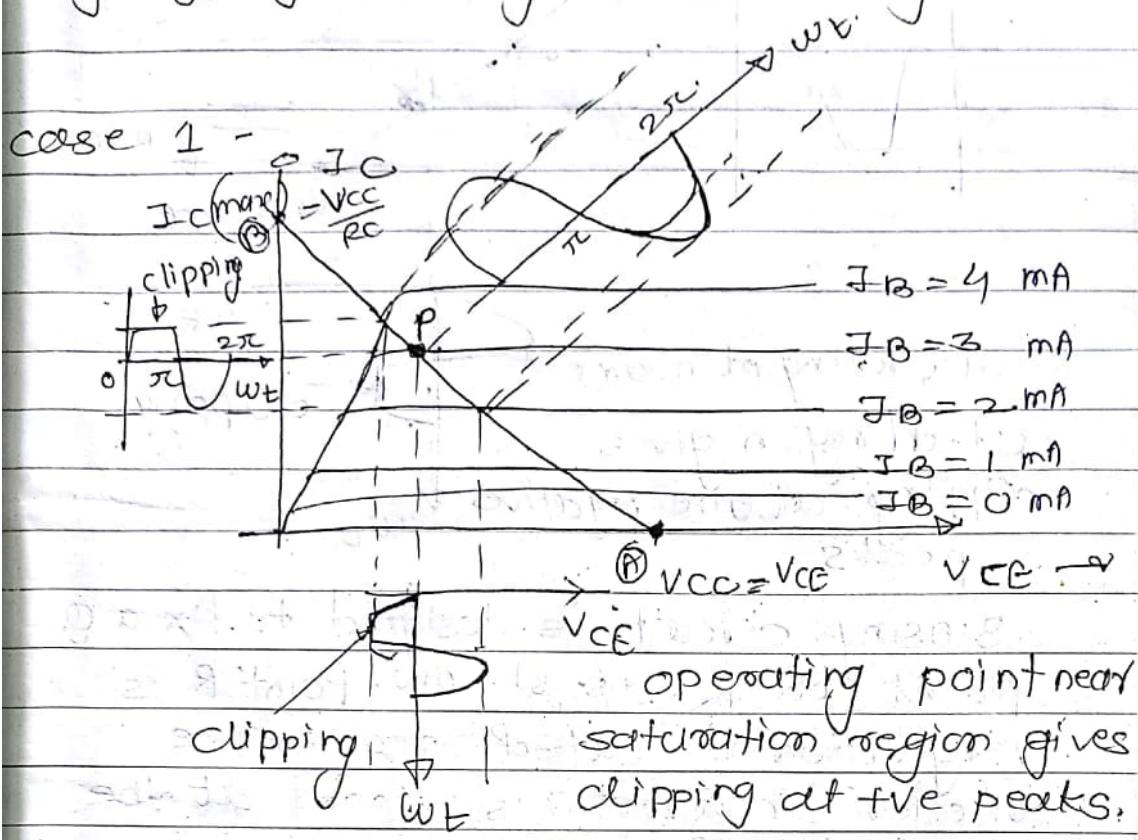
$$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC}}{R_C} - \left[ \frac{1}{R_C} \right] V_{CE}$$

$$= -\left[ \frac{1}{R_C} \right] V_{CE} + \frac{V_{CC}}{R_C}$$

By comparing this equation with straight line eq<sup>n</sup>  $y = mx + c$  where  $m$  is the slope of the line &  $c$  is the intercept on  $y$  axis, then we can draw a straight line on the graph of  $I_C$  versus  $V_{CE}$  which is having slope  $-1/R_C$  and  $y$  intercept  $V_{CC}/R_C$ . To determine the two points on the line we assume  $V_{CE} = V_{CC}$  and  $V_{CE} = 0$ .

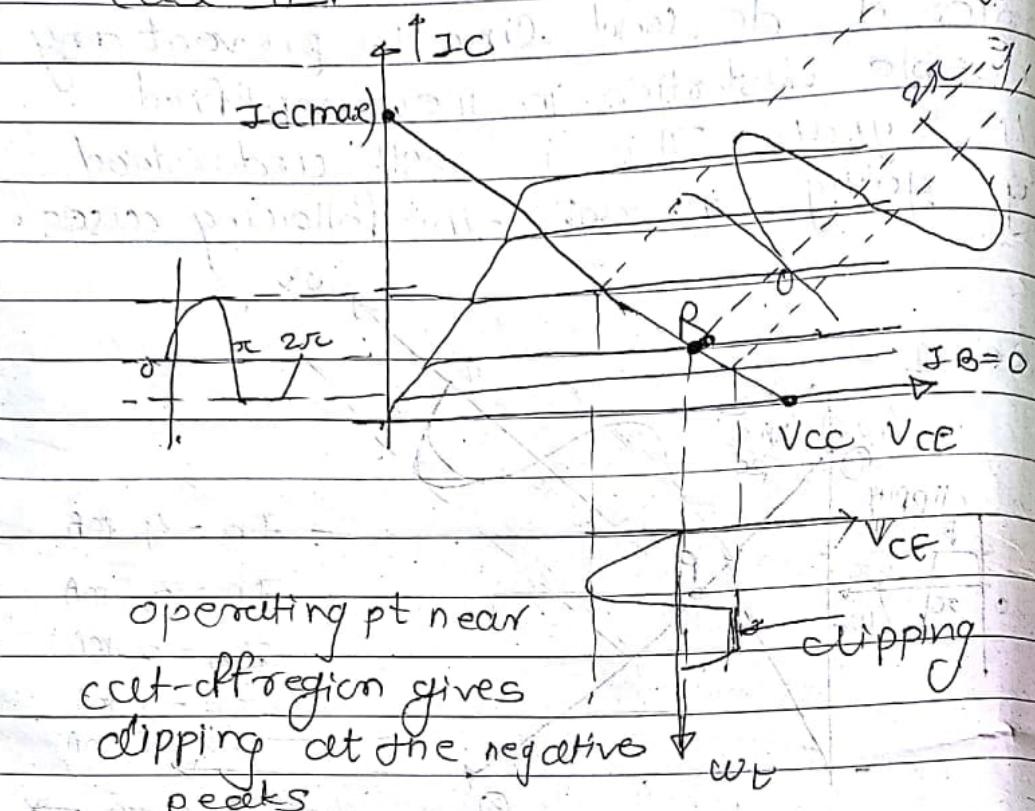
- (a) when  $V_{CE} = V_{CC}$ ;  $I_C = 0$  & we get pt (a)
- (b) when  $V_{CE} = 0$ ;  $I_C = V_{CC}/R_C$  & we get pt (b)

the Q point should be selected at the center of dc load line to prevent any possible distortion in the amplified O/P signal. This is well understood by going through the following cases.



Biasing circuit is designed to fix a Q. point at point P, as shown. Point P is very near to the saturation region. As shown collector current is clipped at the positive half cycle, so even though base current varies sinusoidally, collector current is not a clean sinusoidal waveform. i.e. distortion is present at the output. Therefore point P is not a suitable operating point.

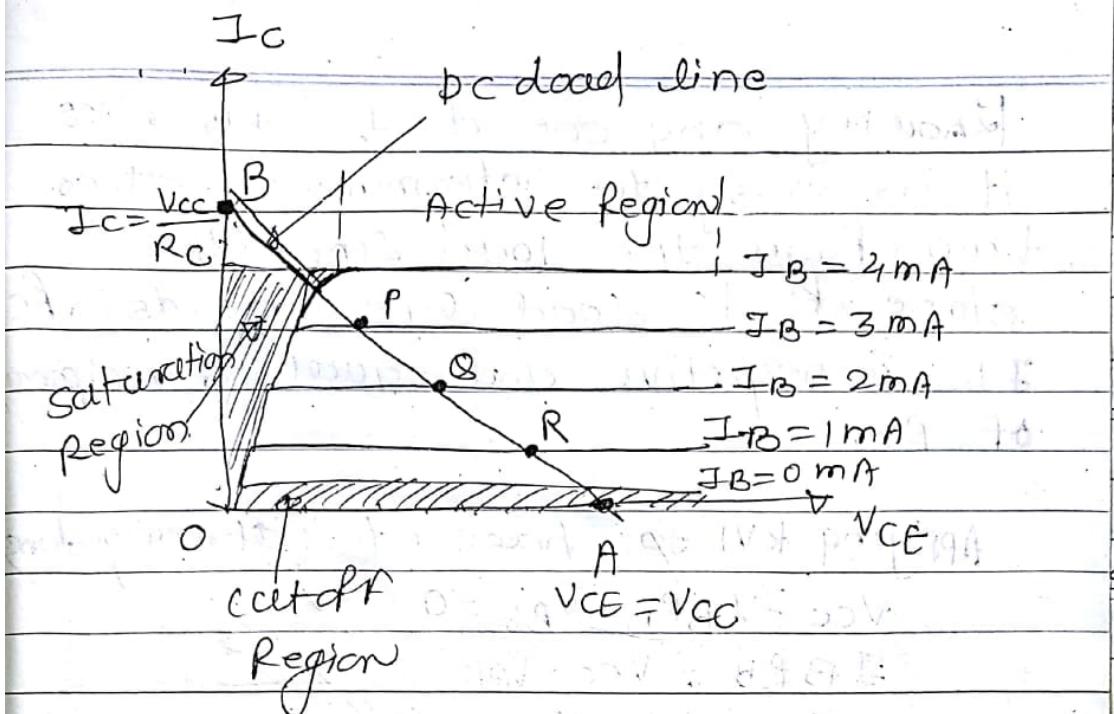
case II.



operating pt near  
cut-off region gives  
clipping at the negative  
peaks

Biasing circuit is designed to fix a Q.  
point at R<sub>9</sub> as shown. Point R is  
very near to cut-off region. The  
collector current is clipped at the  
negative half cycle so pt R is also  
not a suitable operating point.

Case 3 \* Biasing circuit is designed to  
fix a Q point at point Q as shown.  
The o/p signal is sinusoidal waveform,  
without any distortion.



common emitter o/p cht with dc load line

Above fig shows the o/p cht of a common emitter config with pts A+B and the line drawn b/w them.

The line drawn b/w pts A+B is called dc load line.

The dc word indicates that only dc conditions are considered i.e. IP signal is assumed to be zero.

The dc load line is a plot of  $I_c$  versus  $V_{CE}$ . For given value of  $R_C$  and a given level of  $V_{CC}$ . Thus it represents all collector current levels and corresponding collector-emitter voltages that can coexist in the circuit.

Knowing any one of  $I_C$ ,  $I_B$  or  $V_{CE}$  it is easy to determine the other two from the load line. The slope of dc load line depends on  $R_C$ . It is negative and equal to reciprocal of  $R_C$ .

Applying KVL to base col (already done)

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B R_B = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

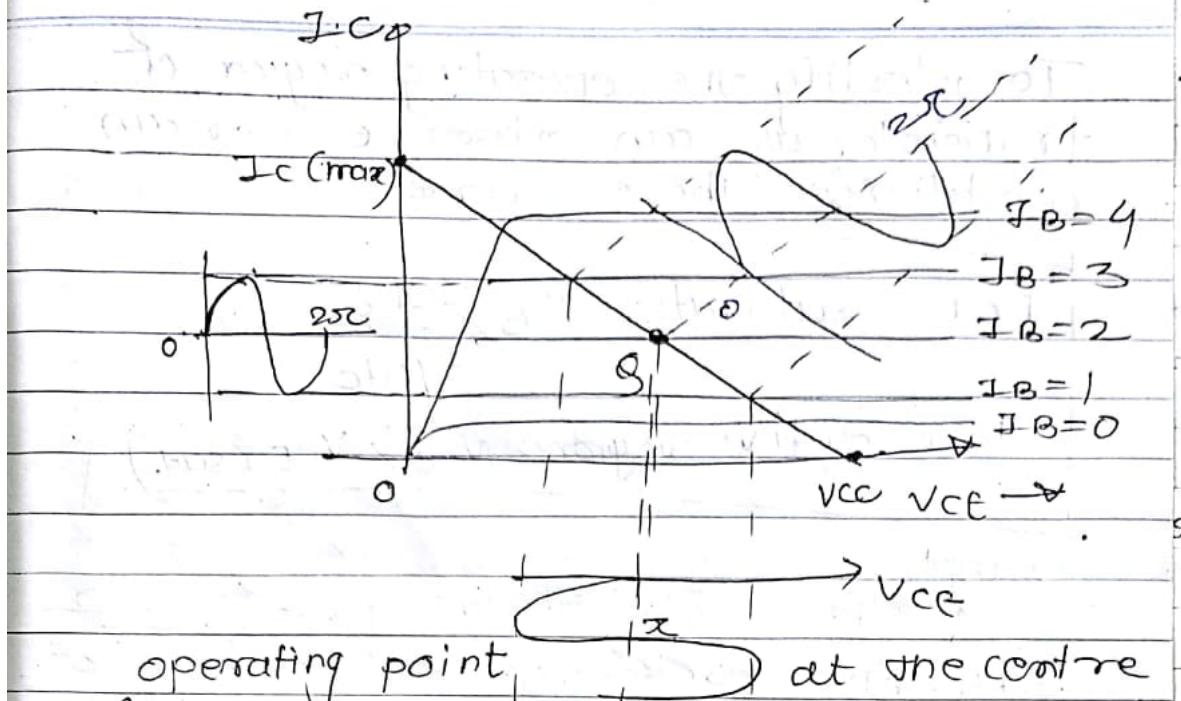
The intersection of curves of different values of  $I_B$  with dc load line gives different operating points. For different values of  $I_B$ , we have different intersection points (quiescent point or Q point) such as as P, Q + R.

### Selection of operating point

Operating point can be selected at different positions on the dc load line: near saturation region, near cut-off region or at the center, ie in the active region.

The selection of operating point will depend on its application.

When transistor is used as an amplifier,



operating point  
at the centre  
of active region is most suitable

### Typical junction voltages and conditions for operating Region

Following table shows typical junction voltages for cut off, active and saturation regions for n-p-n silicon & Germanium transistors. For p-n-p transistors we have to reverse the polarities of voltages given in table.

Transistor	$V_{CE}(\text{sat})$	$V_{BE}(\text{sat})$	$V_{BE}(\text{active})$	$V_{BE}(\text{cut off})$	$V_{BE}$
Si	0.2 V	0.8 V	0.7 V	0 V	cat in 0.5 V
Ge	0.1 V	0.3 V	0.2 V	-0.1 V	0.1 V

Table - Typical Junction voltages

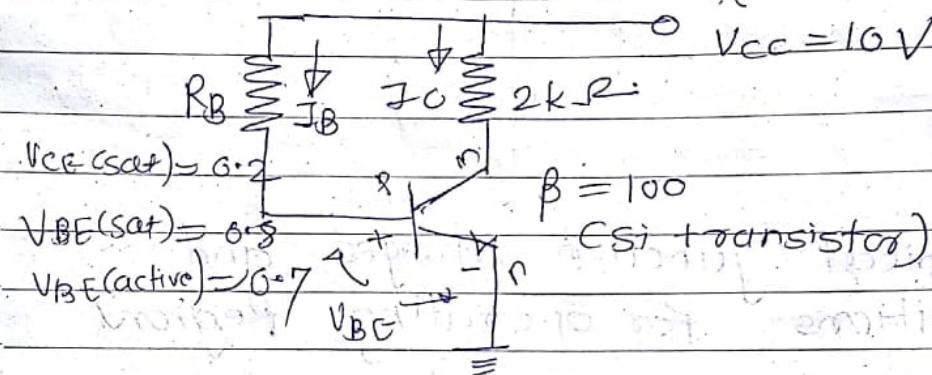
To identify the operating region of transistor we can observe certain conditions. These are

$$\text{For saturation } I_B > \frac{I_C}{\beta_{dc}}$$

$$\text{For active region } V_{CE} > V_{CE(\text{sat})}$$

Example:

In the circuit shown  $R_B = 300\text{k}\Omega$  and  $R_E = 150\text{k}\Omega$ , calculate  $I_B$ ,  $I_{Ct}$  and  $V_{CE}$  and determine region of operation.



Solution i)  $R_B = 300\text{k}\Omega$

Since base emitter junction is not reverse biased, we can say that transistor is not in cut off region.

Assume transistor is operating in an active region.

Applying KVL around base loop we get

$$V_{CC} = I_B R_B + V_{BE}$$

$$10 = I_B \times 300 \times 10^3 + 0.7$$

$$I_B = \frac{9.3}{300 \times 10^3} = 0.031\text{mA}$$

$$I_B = 31 \mu A$$

In active region  $I_C = \beta I_B$

$$I_C = 100 \times 31 \mu A$$

$$I_C = 3.1 \text{ mA}$$

Now applying KVL around collector loop we get.

$$V_{CD} = I_C R_C + V_{CE} - 3 = 32 V$$

$$10 = 3.1 \times 10 + 2 \times 10 + V_{CE}$$

$$V_{CE} = 10 - 6.2 = 3.8 V$$

$$V_{CE} = 3.8 V$$

Collector to base junction is reverse biased and we can say that our assumption that transistor is in active region is satisfied. Justified.

$$R_B = 150 k\Omega + (10 \times 10) \Omega = 101 \Omega$$

Base emitter junction is not reverse biased, we can say that transistor is not in cutoff region. Assume transistor is in an active region.

KVL around base loop we get

$$V_{CC} = I_B R_B + V_{BE}$$

$$10 = I_B \times 150 \times 10^{-3} + 0.7$$

$$I_B = 9.3 / 150 \times 10^{-3} = 0.062 \text{ mA} = 62 \mu A$$

$$I_B = 62 \mu A$$

In active region.

$$I_C = \beta I_B$$

$$I_C = 100 \times 62 \times 10^{-6} \text{ mA}$$

$$\boxed{I_C = 6.2 \text{ mA}}$$

Now apply KVL around collector loop

$$V_{CC} = I_C R_C + V_{CE} \quad (V_{CE} > V_{C-E})$$

$$10 = 6.2 \times 10^3 \times 2 \times 10^3 + V_{CE} \quad \begin{matrix} \text{Collector voltage} \\ \text{is forward biased} \end{matrix}$$

$$V_{CE} = 10 - 12.4 = -2.4 \text{ V} \quad \begin{matrix} V_C \text{ is reverse} \\ \text{biased} \end{matrix}$$

It is important to note that collector voltage has to be +ve or zero. Hence our assumption that transistor is in active region is wrong and it is in saturation region.

Applying KVL around base loop we get

$$V_{CC} = I_B R_B + V_{BE} (\text{sat})$$

$$10 = I_B (150 \times 10^3) + 0.8$$

$$I_B = \frac{9.2}{150 \times 10^3} = 61.33 \text{ nA}, I_B = 61.33 \text{ nA}$$

Applying KVL around collector loop

$$V_{CC} = I_C R_C + V_{CE} (\text{sat})$$

$$10 = I_C (2 \times 10^3) + 0.2$$

$$I_C = \frac{9.8}{2 \times 10^3} = 4.9 \text{ mA}$$

$$\boxed{I_C = 4.9 \text{ mA}}$$

To justify transistor is in saturation

$$I_B > \frac{I_C}{\beta}, \frac{I_C}{\beta} = \frac{4.9 \times 10^3}{100} = 49 \text{ nA}$$

$$I_B = 61.33 \mu A \Rightarrow I_C \text{ ie } 49 \mu A$$

Hence our assumption that transistor is in saturation is justified.

### Advantages of Fixed Bias Circuit

- ① Simple circuit which uses very few components.
- ② The operating point can be fixed anywhere in the active region of characteristics simply changing the value of  $R_B$ . Thus it provides maximum flexibility in the design.

### Disadvantages of fixed bias circuit

- ① This circuit does not provide any check on the collector current which increases with the rise in temperature, i.e. thermal stability is not provided by this circuit so operating point is not maintained.

$$I_C = \beta I_B + I_{CEO}$$

- ② Since  $I_C = \beta I_B$  and  $I_B$  is already fixed;  $I_C$  depends on  $\beta$  which changes unit to unit and shifts the operating point.

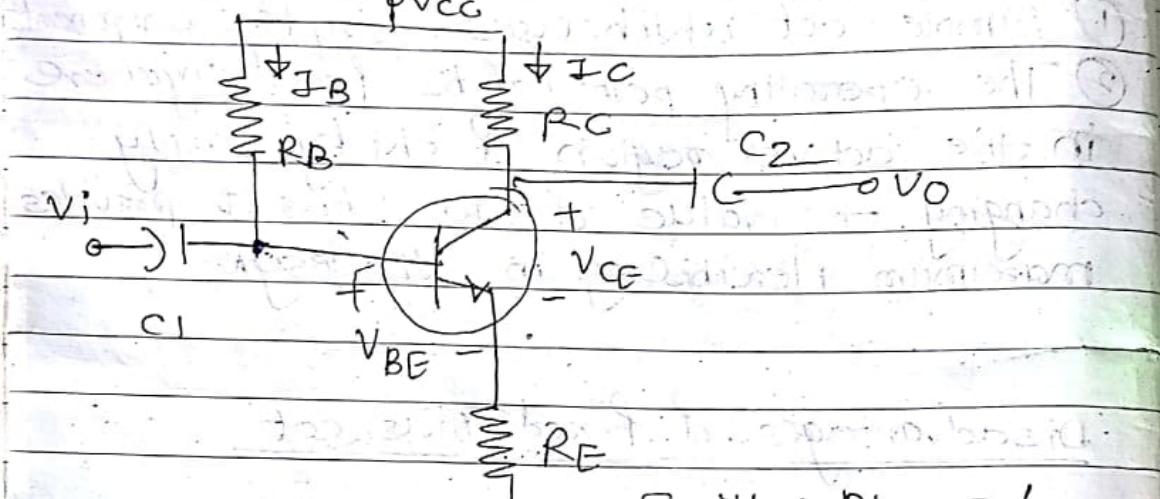
Thus stabilization of operating point is very poor in the fixed bias circuit.

$$V_B - V_{BE} - I_E R_E = 0$$

$$V_{BE} = V_B - I_E R_E$$

## Emitter stabilized Biased circuit

To improve the stability of the biasing circuit over the fixed bias circuit, the emitter resistance is connected in the biasing set. Such biasing circuit is known as emitter bias circuit as shown.



Emitter Bias circ.

Circuit Analysis

as  $V_{BE} = \frac{V_B - V_E}{R_E + R_B}$   $\therefore V_{BE} = \frac{V_B - V_E}{R_E + R_B}$

$I_B = \frac{V_{CC} - V_B}{R_B}$   $\therefore I_B = \frac{V_{CC} - V_B}{R_B + R_E}$

$V_B = V_{CC} - I_B R_B$   $\therefore I_B = \frac{V_{CC} - V_B}{R_B + R_E}$

$V_{BE} = V_{CC} - V_B - I_E R_E$   $\therefore I_E = \frac{V_{CC} - V_B - V_E}{R_E + R_B}$

$R_B + R_E$

Applying KVL to the base circuit we get

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \quad \text{--- Eqn 1}$$

$$\text{We have, } I_E = (1 + \beta) I_B \quad \text{--- Eqn 2}$$

put ② in eqn ①  $\therefore (I_E = \frac{I_C + I_B}{\beta + 1})$

$$(I_E = \frac{I_C + I_B}{\beta + 1}) = I_B (\beta + 1)$$

$$= I_B (\beta + 1)$$

$$V_{CC} - I_B R_B - V_{BE} - (1 + \beta) I_B R_E = 0$$

$$V_{CC} - V_{BE} = I_B R_B + (1 + \beta) I_B R_E$$

- ① Due to increase in temp  $I_C \propto I_E$
- ② As  $I_E$   $\downarrow$  Voltage drop across  $R_E$   $V_{BE} \uparrow$  (31)
- ③  $\uparrow V_{BE}$   $\downarrow$ . This will reduce value of  $I_B$  & therefore increased collector will be reduced
- $V_{CC} - I_B R_E = V_{CE}$  Thus stabilization  
 $I_B = \frac{V_{CC} - V_{BE}}{R_E + (1+\beta)R_E}$  of a pt tankies  
 place.

$$I_B = \frac{V_{CC} - V_{BE}}{R_E + \beta R_E} \quad \because \beta \gg 1$$

This expression for bias current at Q point is  $I_B \approx$ .

Note that the only difference b/w the eqn for  $I_B$  and that obtained for fixed bias config is the term  $\beta R_E$ .

$$I_C = \beta_{dc} I_B$$

$$V_B = V_{BE} + V_E \quad \text{or} \quad V_{CC} - I_B R_E$$

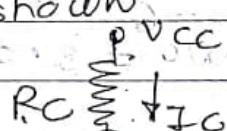
$$\text{since } V_E = I_E R_E$$

$$V_B = V_{BE} + I_E R_E$$

$$V_{BE} = V_B - I_E R_E$$

collector Circuit

We now consider the collector circuit as shown



apply KVL to collector cat

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CC} - I_C R_C - V_E - I_E R_E = 0$$

$$V_{CE} = V_{CC} + I_C R_C - I_E R_E$$

$$V_E = I_E R_E$$

$$V_{CE} = V_C - V_E$$

$$V_C = V_{CC} - I_C R_C$$

$$V_{CC} - I_C R_C - V_{CE} + (I_C + I_B) R_E = 0$$

$$V_{CC} - I_C (R_C + R_E) - V_{CE} - I_B R_E = 0$$

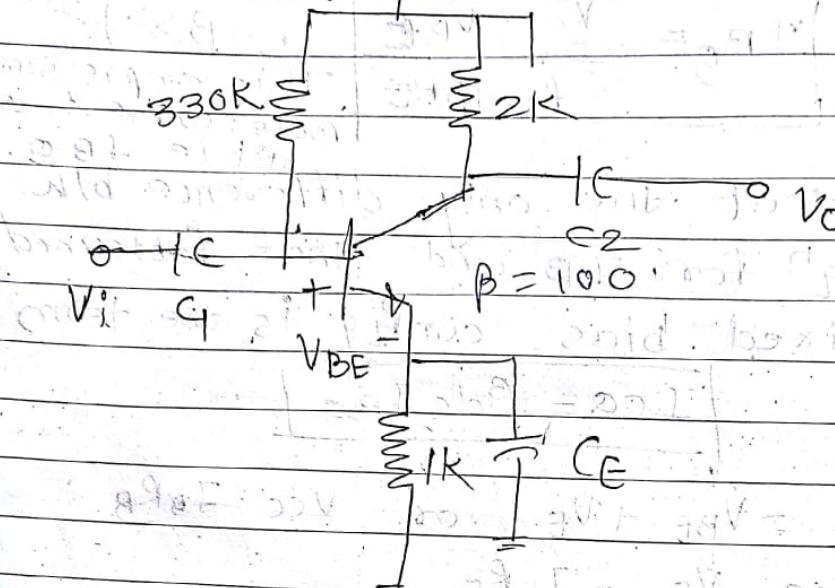
$$V_{CE} = V_{CC} - I_C (R_C + R_E) - I_B R_E \quad \text{as } V_{CC} \gg I_B R_E$$

$$\therefore V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Q For the circuit shown calculate  $I_B$ ,  $I_C$ ,

$V_{CE}$ ,  $V_C$ ,  $V_E$ ,  $V_B$  and  $V_{BC}$ . Assume  $\beta = 100$

$$V_{CC} = 15V$$



solution

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{15 - 0.7}{330 \times 10^3 + (1 + 100) \times 10^3} A$$

$$= 3.317865429 \times 10^{-5} A$$

$$\boxed{I_B = 33.18 \mu A}$$

$$I_C = \beta I_B = 100 \times 33.18 \times 10^{-3} = 3.317865429 \times 10^{-2} A$$

$$\boxed{I_C = 3.318 \text{ mA}}$$

$$I_E = I_B + I_C = 3.351044084 A$$

$$\boxed{I_E = 3.351 \text{ mA}}$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$= 15 - 3.318 \times 10^3 \times 2 \times 10^3 - 3.351 \times 10^3 \times 10^3$$

$$\boxed{V_{CE} = 5V}$$

$$V_C = V_{CC} - I_C R_C = 15 - 3.318 \times 10^3 \times 2 \times 10^3$$

$$\boxed{V_C = 8.364V}$$

$$V_E = I_E R_{E\text{eq}} = 3.35 \times 10^3 \times 1 \times 10^3$$

$$V_E = 3.351V$$

$$\text{Now } V_B = V_E + V_{BE} = 3.351 + 0.7$$

$$V_B = 4.051V$$

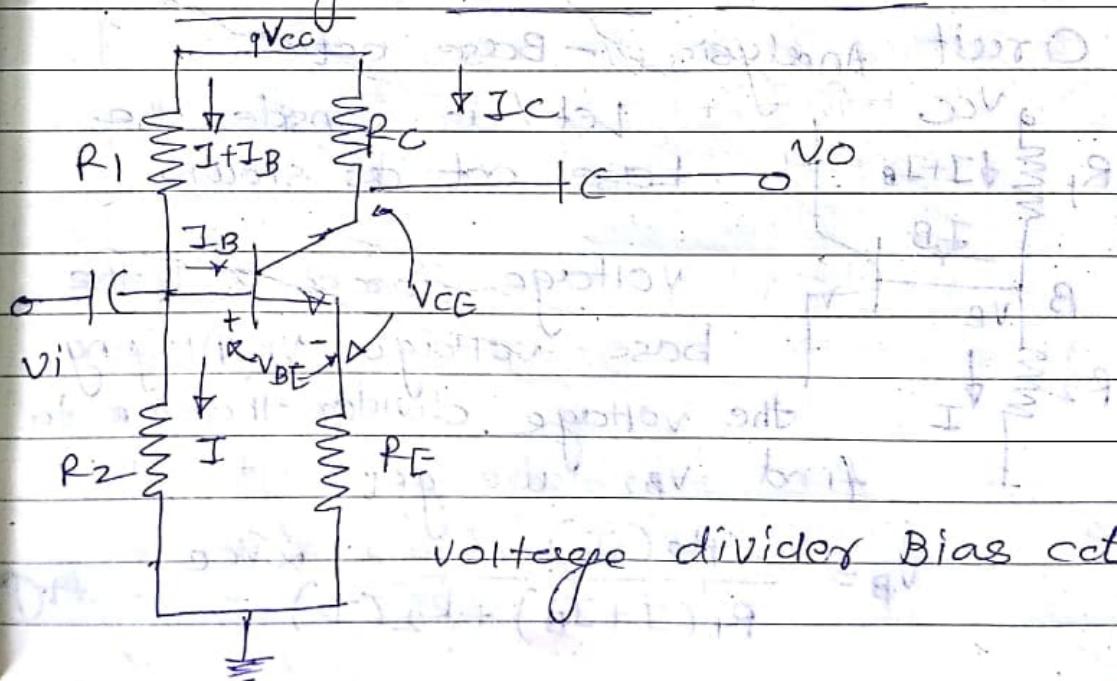
$$V_{BC} = V_B - V_C = 4.051 - 8.364$$

$$V_{BC} = -4.313V$$

Stability Improvement

The addition of emitter resistance,  $R_E$  in the emitter bias circuit provides improved stability, that is the d.c. bias currents and voltages remain closer to where they were set by the circuit against the changes in temperature and transistor  $\beta$  (beta).

### Voltage Divider Biased

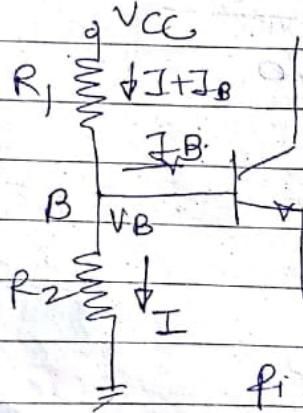


In this collector biasing is provided by three resistors:  $R_1$ ,  $R_2$  &  $R_E$ . The resistors  $R_1$  and  $R_2$  act as a potential divider giving a fixed voltage to point B which is base.

If the collector current increases due to change in temperature or change in  $\beta$ , the emitter current  $I_E$  also increases and the voltage drop across  $R_E$  increases, reducing the voltage difference between base and emitter ( $V_{BE}$ ) due to reduction in  $V_{BE}$ , base current  $I_B$  and hence collector current  $I_C$  also reduces. Therefore, we can say that negative feedback exists in the emitter bias circuit.

This reduction in collector current  $I_C$  compensates for the original change in  $I_C$ .

Circuit Analysis - Base circuit



Let us consider the base circuit as shown

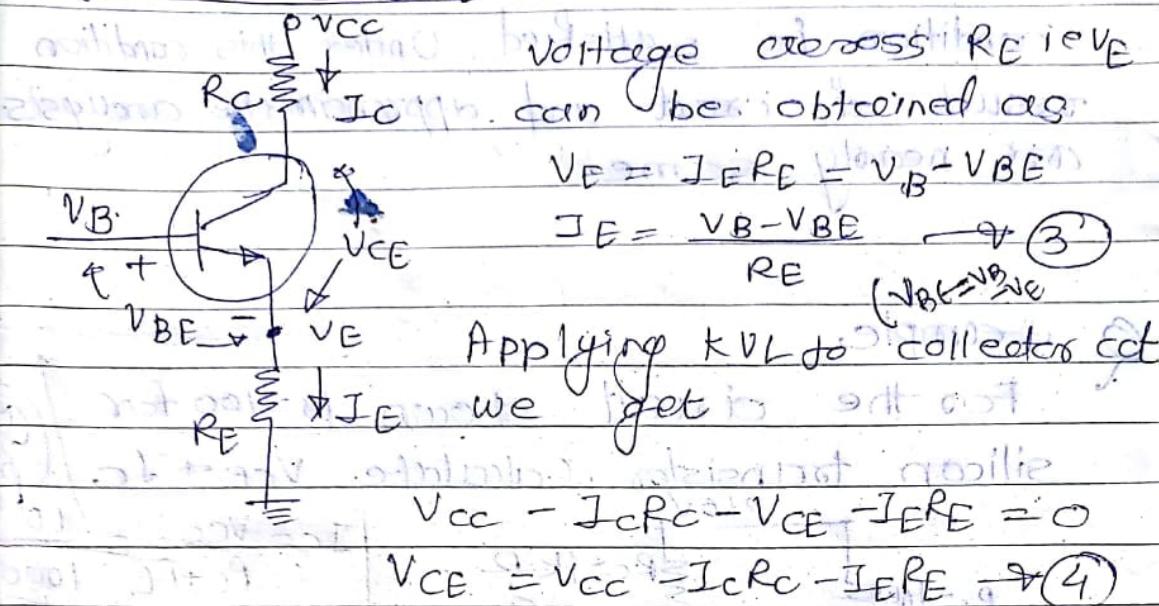
voltage across  $R_2$  is the base voltage  $V_B$ . Applying the voltage divider theorem to find  $V_B$ , we get

$$V_B = \frac{R_2(I)}{R_1(I+I_B) + R_2(I)} \times V_{CC} \quad (1)$$

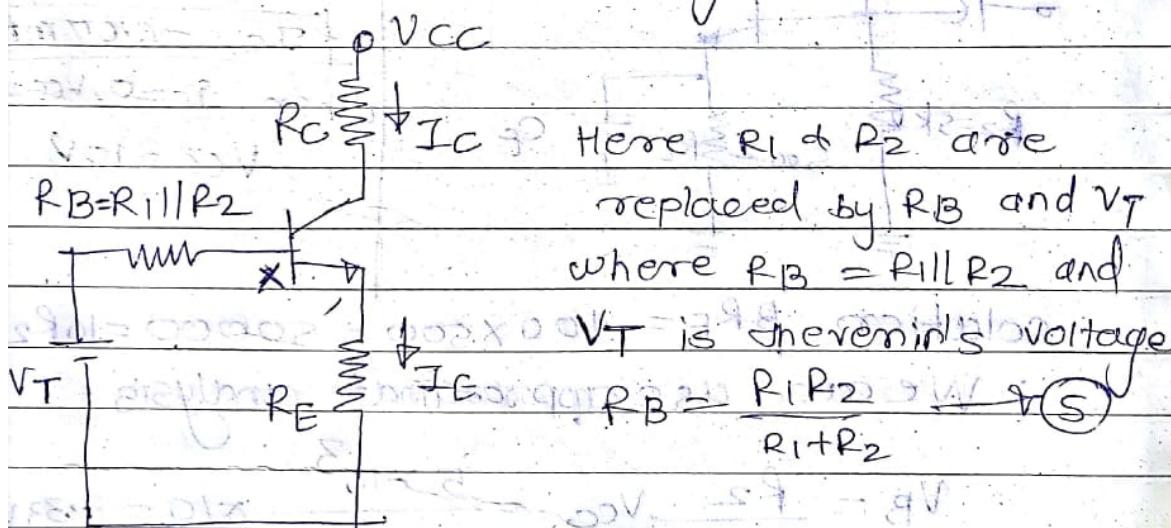
$$V_B = \frac{R_2}{R_1 + R_2} \times V_{CC} \quad \rightarrow (2)$$

$\because I \gg I_B$

Collector circuit



Simplified col of voltage divider bias



Thevenin's eq col for voltage divider Bias base circuit

$$V_T = I_B R_B + V_{BE} + I_E R_E \quad \rightarrow (6)$$

$$= V_{BE} + (R_B + R_E) I_B + I_C R_E \quad \therefore I_E = I_C + I_B$$

$$V_{BE} = V_T - (R_B + R_E) I_B - I_C R_E \quad \rightarrow (7)$$

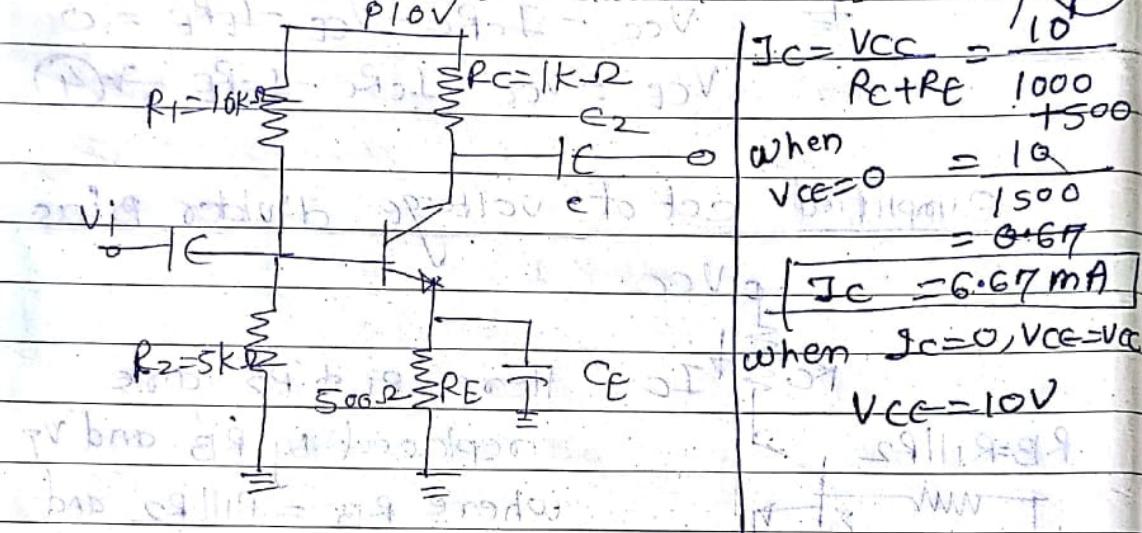
We can use simplified/approximate analysis when

$$\beta R_E \gg 10R_2$$

condition is satisfied. Under this condition results of exact and approximate analysis are nearly same.

Q Example

For the circuit shown,  $\beta = 100$  for silicon transistor. Calculate  $V_{CE}$  &  $I_C$ .



$$I_C = \frac{V_{CC}}{R_E + R_F} = \frac{10}{1000 + 500}$$

$$\text{when } V_{CE} = 0 = 1A$$

$$= 0.67$$

$$I_C = 0.67 \text{ mA}$$

$$\text{when } I_C = 0, V_{CE} = V_{CC}$$

$$V_{CE} = 10V$$

$$\text{solution. } \beta R_E = 100 \times 500 = 50000 = 10R_2$$

We can use approximate analysis.

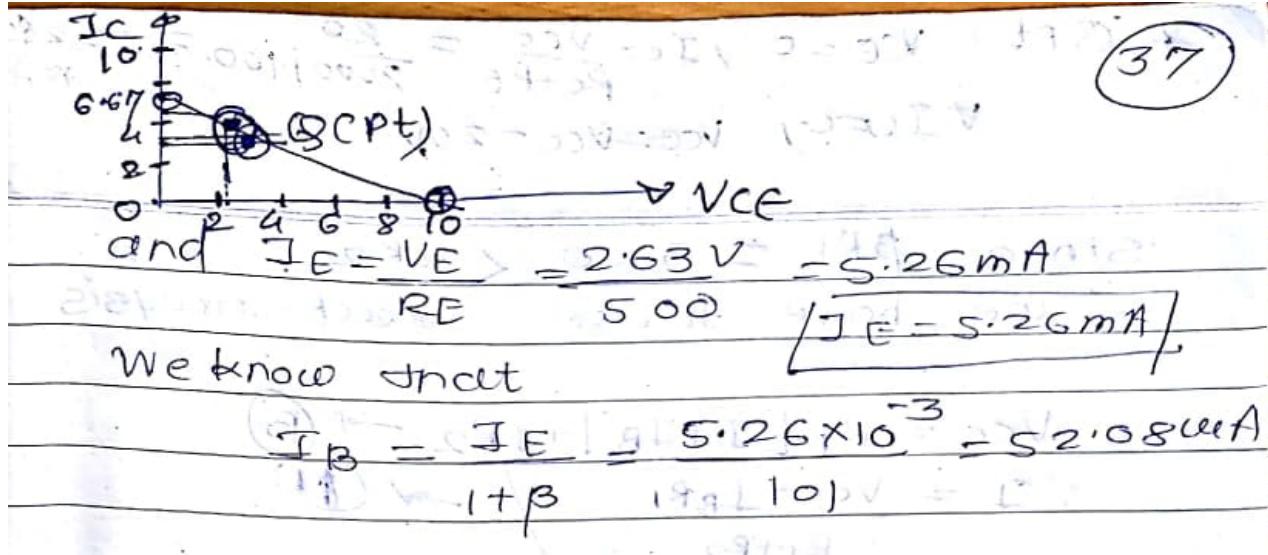
$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{5 \times 10^3}{(10 + 5) \times 10^3} \times 10 = 3.33 \text{ V}$$

$$V_B = 3.33 \text{ volt}$$

$$\text{We can know that } V_E = V_B - V_{BE} = 3.33 - 0.67 = 2.63 \text{ V}$$

$$= 3.33 - 0.67 = 2.63 \text{ V}$$

$$V_E = 2.63 \text{ V}$$



$$I_B = 0.04 \text{ mA}$$

$$\text{and } I_C = \beta I_B = 100 \times 0.04 = 4 \text{ mA}$$

$$I_C = 4 \text{ mA}$$

applying KVL to collector circuit we get

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

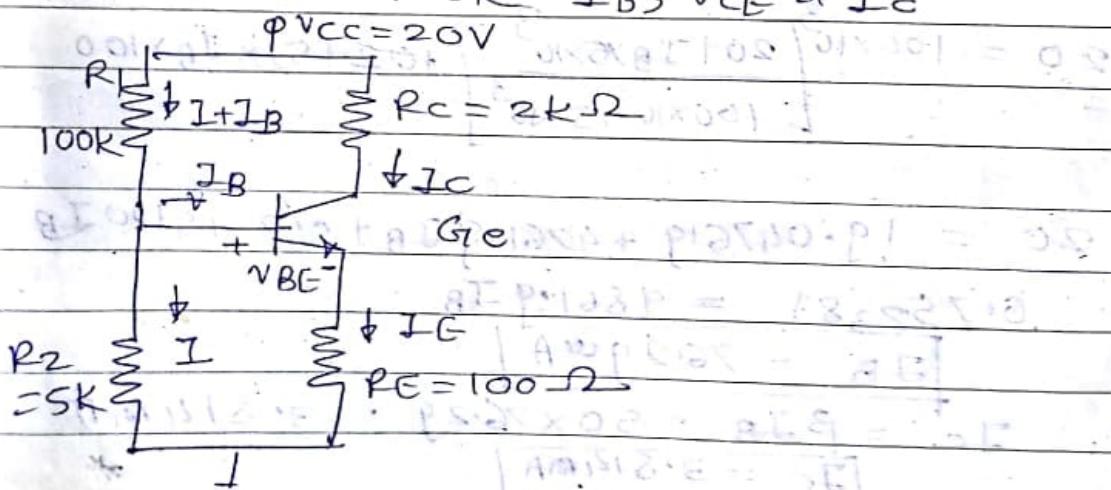
$$= 20 - 4 \times 2 - 4 \times 500 = 2.162 \text{ V}$$

$$V_{CE} = 2.162 \text{ V}$$

$$(I_C, V_{CE}) \Rightarrow I_C = 4 \text{ mA}, V_{CE} = 2.162 \text{ V}$$

For the circuit shown,  $V_{CC} = 20V$ ,  $R_C = 2k\Omega$ ,

$\beta = 50$ ,  $V_{BE\text{act}} = 0.2V$ ,  $R_1 = 100k\Omega$ ,  $R_2 = 5k\Omega$  &  $R_E = 100\Omega$ , calculate  $I_B$ ,  $V_{CE}$  &  $I_C$ .



$$* \text{ Q Pt, } V_{CE} = 0, I_C = \frac{V_{CC}}{R_C + R_E} = \frac{20}{2000 + 100} = 9.52 \text{ mA}$$

$$\& I_C = 0, V_{CE} = V_{CC} = 20V$$

Since  $R_E \approx 5000 < 10R_2$

$\therefore$  we have to use exact analysis

$$V_{CC} = R_1 [I + I_B] + I R_2 \rightarrow (B)$$

$$I = \frac{V_{CC} - I_B R_1}{R_1 + R_2} \rightarrow (1)$$

$$V_{CC} = R_1 [I + I_B] + V_{BE} + I_E R_E \rightarrow (A)$$

(KVL base cat. (bottom))

$$\rightarrow I R_2 + I_E R_E + V_{BE} = 0$$

$$I_E R_E + V_{BE} = I R_2$$

We know that

$$I_E = I_B + I_C = I_B + \beta I_B \text{ put in (A)}$$

$$\therefore V_{CC} = R_1 [I + I_B] + V_{BE} + I_B (1 + \beta) R_E$$

put value of  $I$  from eqn (1) in above

$$V_{CC} = R_1 \left[ \frac{V_{CC} - I_B R_1 + I_B}{R_1 + R_2} + V_{BE} + (1 + \beta) I_B R_E \right]$$

$$= R_1 \left[ \frac{V_{CC} - I_B R_1 + I_B R_1 + I_B R_2}{R_1 + R_2} + V_{BE} + (1 + \beta) I_B R_E \right]$$

$$= R_1 \left[ \frac{V_{CC} + I_B R_2}{R_1 + R_2} + V_{BE} + (1 + \beta) R_E I_B \right]$$

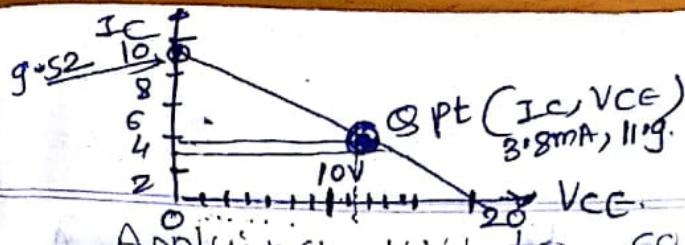
$$20 = 100 \times 10 \left[ \frac{20 + I_B \times 5 \times 10^3}{100 \times 10^3 + 5 \times 10^3} + 0.2 + 5 \times I_B \times 100 \right]$$

$$20 = 19.047619 + 4761.9 I_B + 0.2 + 500 I_B$$

$$6.752381 = 9861.9 I_B$$

$$I_B = 76.29 \mu A$$

$$I_C = \beta I_B = 50 \times 76.29 = 3.814 \text{ mA}$$



(39)

Applying KVL to collector cat we get

$$V_{CC} = I_C R_C + V_{CE} + I_B R_E$$

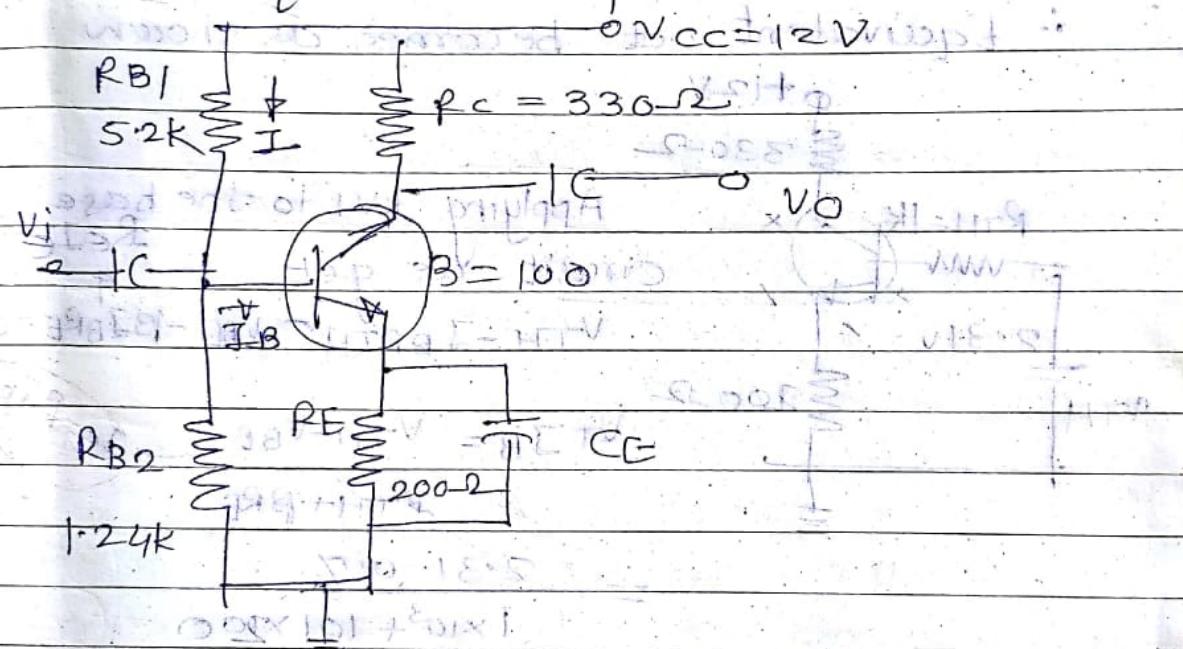
$$= I_C R_C + V_{CE} + (1+B) I_B R_E$$

$$V_{CE} = V_{CC} - I_C R_C - (1+B) I_B R_E$$

$$V_{CE} = 20 - 3.814 \times 10^3 \times 2 \times 10^3 - 51 \times 76.29 \times 10^6 \times 100$$

$$V_{CE} = 11.983 \text{ V}$$

Q. For the cat shown draw dc load line for the following transistor config.  
Obtain quiescent point:



Solution - Since  $R_E = 20 \text{ k}\Omega$  and which is greater than  $10R_2$  we can use approximate analysis.

$$10R_2 = 10 \times 1.24$$

$$100 \times 1.24 - (0.5 \times 100 \times 1.24) - 8 = 12.4 \text{ k}\Omega$$

$$I = \frac{V_{CC}}{R_{B1} + R_{B2}} = \frac{12}{5.2k + 1.24k} = 1.863 \text{ mA}$$

$$\boxed{I = 1.863 \text{ mA}}$$

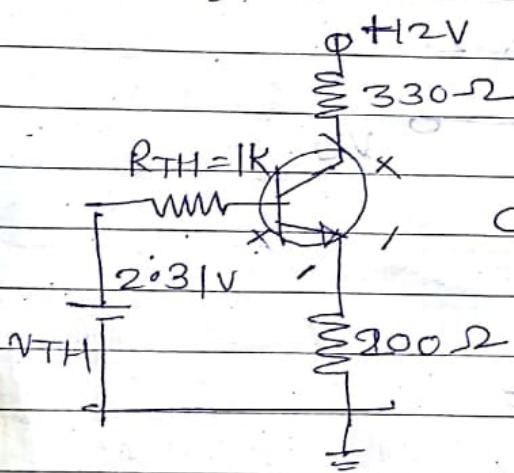
$$V_{TH} = V_{RB2} = I \times R_{B2} = 1.863 \text{ mA} \times 1.24k = 2.31 \text{ V}$$

$$\boxed{V_{TH} = 2.31 \text{ V}}$$

$$R_{TH} = R_1 || R_2 = R_{B1} || R_{B2} \\ = 5.2 \times 1.24 \times 10^6$$

$$\boxed{R_{TH} = 1 \text{ k}\Omega}$$

∴ Equivalent circuit becomes as shown



Applying KVL to the base circuit we get

$$V_{TH} - I_B R_{TH} - V_{BE} - \beta I_C R_E = 0$$

$$\beta I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + \beta R_E}$$

$$= \frac{2.31 - 0.7}{1 \times 10^3 + 101 \times 200}$$

$$\boxed{I_B = 75.94 \text{ mA}}$$

Applying KVL to collector circuit we have,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

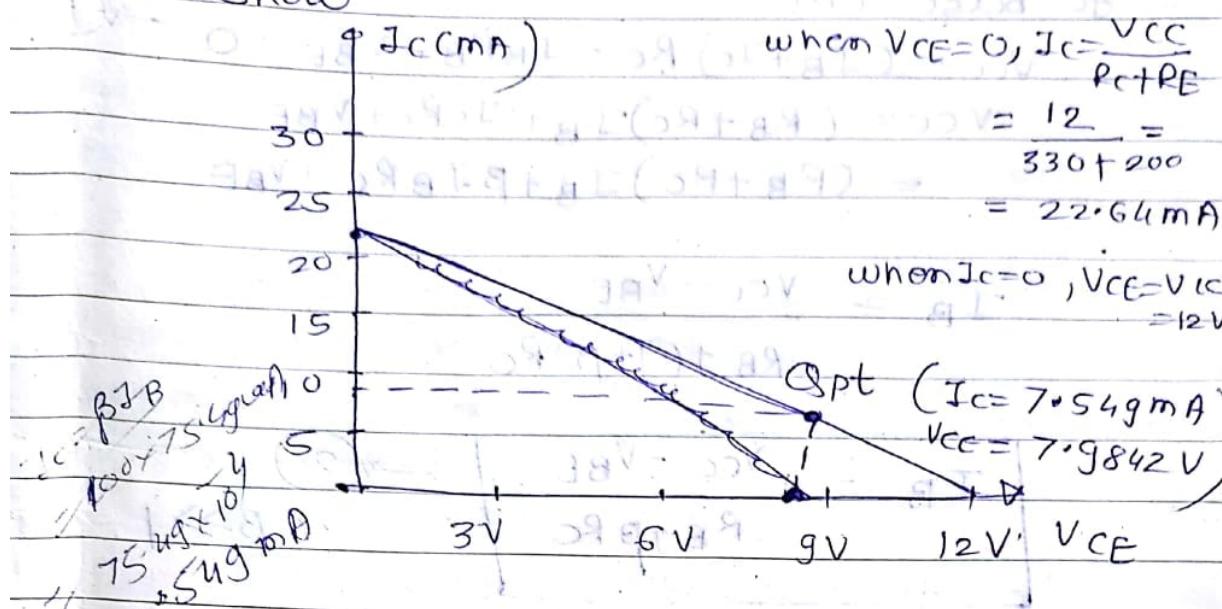
$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \rightarrow (\beta I_B R_E)$$

$$= 12 - (7.549 \times 10^3 \times 330) - 101 \times 75.49 \times 10^3 \times 200$$

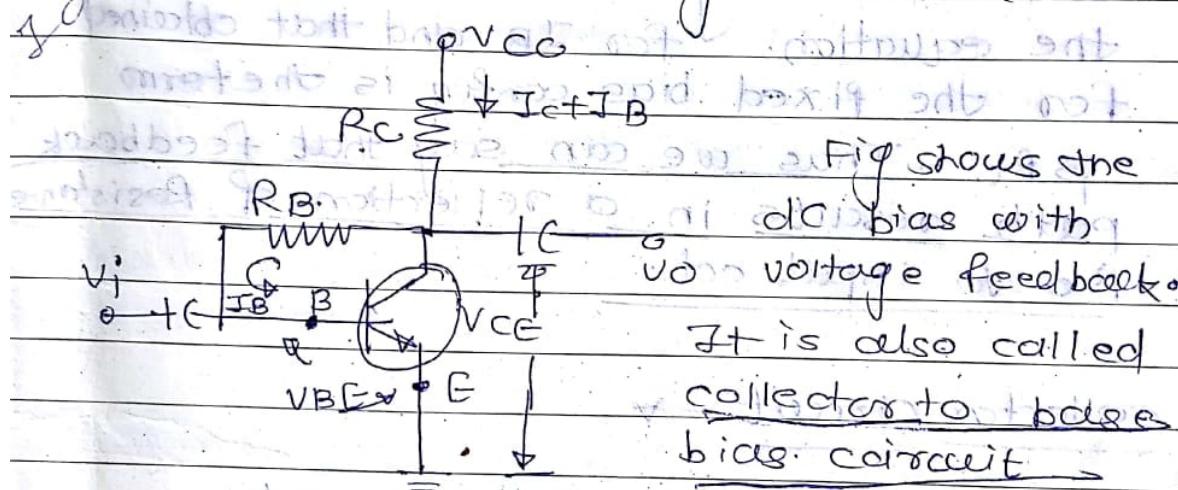
$$\boxed{V_{CE} = 7.9842 \text{ V}}$$

(41)

The DC load line for the given circuit is as shown



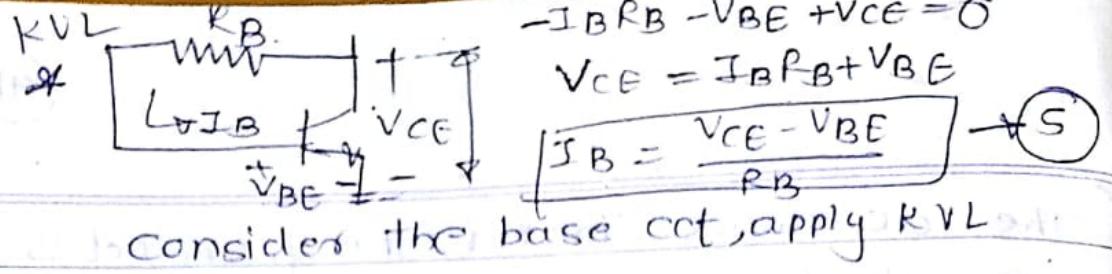
DC biasing with voltage feedback



It is an improvement over the fixed bias method. In this, the biasing resistor is connected b/w collector & base of Transistor to provide feedback path.

Thus,  $I_B$  flows through  $R_B$  and  $(I_C + I_B)$  flows through  $R_C$  (in parallel).

Now,  $I_B$  is  $\beta A$ . Opt. bias is  $\beta E$  times of  $I_C$  because  $I_C = \beta E$



consider the base cat, apply KVL

do base cat

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0 \rightarrow \textcircled{1}$$

$$V_{CC} = (R_B + R_C) I_B + I_C R_C + V_{BE}$$

$$= (R_B + R_C) I_B + \beta I_B R_C + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1 + \beta) R_C}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C} \rightarrow \textcircled{2}$$

$\beta \gg 1$

Note that only difference between the equation for  $I_B$  and that obtained for the fixed bias config is the term  $\beta R_C$ . Thus we can say that feedback path results in a reflection of resistance  $R_C$  to input cat.

collector circuit

applying KVL to collector cat

$$I_C R_C + V_{CE} - (I_C + I_B) R_C - V_{CE} = 0 \rightarrow \textcircled{3}$$

$$\therefore V_{CE} = V_{CC} - (I_C + I_B) R_C \rightarrow \textcircled{4}$$

If there is a change in  $\beta$  due to pieced variation in transistors or if

there is a change in  $\beta$  and  $I_C$  due to change in temperature, then collector current  $I_C$  tends to increase, since

$I_C = \beta I_B + I_{CEO}$ . As a result, voltage drop across  $R_C$  increases.

$T^{\Phi}, \beta_{dc} \approx I_{CO}/I_C$ ,  $I_C = I_C P_C$

$$V_{CE} \downarrow \text{as } V_{CE} = V_{CC} - (I_C + I_B) R_C \quad \text{eqn ①}$$

$$\Delta I_B \downarrow \text{as } I_B = V_{CE} - V_{BE} / R_B \quad \text{eqn ②}$$

Hence  $I_C \downarrow$  hence  $I_B \downarrow$

Since supply voltage  $V_{CC}$  is constant, due to increase in  $I_C P_C$ ,  $V_{CE}$  decreases.

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Due to reduction in  $V_{CE}$ ,  $I_B$  reduces.

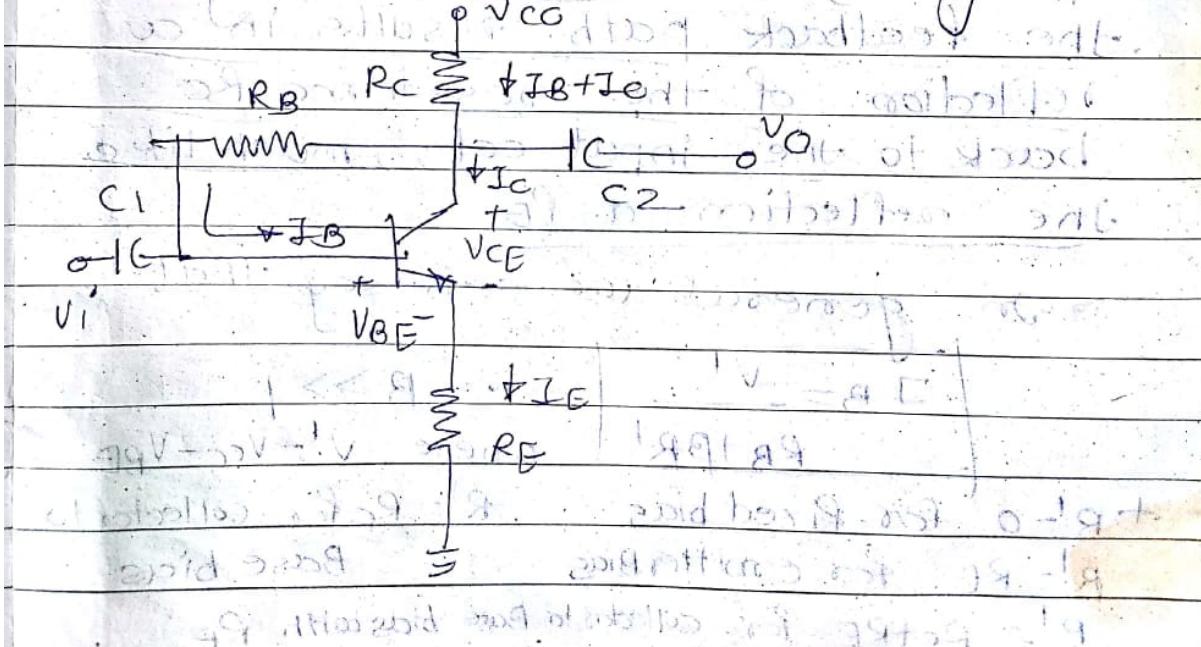
As  $I_C$  depends on  $I_B$ , decrease in  $I_B$  reduces the original increase in  $I_C$ .

$$\text{From eqn ② } I_B = \frac{V_{CC} - V_{CE}}{R_C} - I_C \text{ or from eqn ② as } \beta P, I_B$$

The result is that the circuit tends to maintain a stable value of collector current, keeping the Q point fixed.

In this circuit,  $R_B$  appears directly across input (base) and output (collector). A part of O/P is fed back to the input and increase in collector current decreases the base current. This negative feedback exists in the circuit, so this circuit is also called voltage feedback biased circuit.

Modified pebbies with (voltage) feedback



To further improve the level of stability, the emitter resistance is connected as shown

Applying KVL to base collector

$$V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} + V_{BE} = (1 + \beta) I_B R_C + I_B R_B + (1 + \beta) I_E R_E$$

$$I_B = \frac{V_{CC} + V_{BE}}{R_C + R_B + (1 + \beta)(R_E + R_C)}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

Note that the only difference b/w eqn for  $I_B$  and that obtained for fixed bias config is the term  $\beta(R_C + R_E)$ . Thus we can say that

the feedback path results in a reflection of the resistance  $R_C$  back to the input cct, much like the reflection of  $R_E$ .

In general we can say that

$$I_B = \frac{V'}{R_B + \beta R'_1}$$

where  $V' = V_{CC} - V_{BE}$

$+ R'_1 = 0$  for fixed bias  $R'_1 = R_C$  for collector to base bias

$R'_1 = R_E$  for emitter bias

Base bias

$R'_1 = R_C + R_E$  for collector to base bias with  $R_E$