

TLM 2.0Approximately Time (AT) System Example – Mixed AT System

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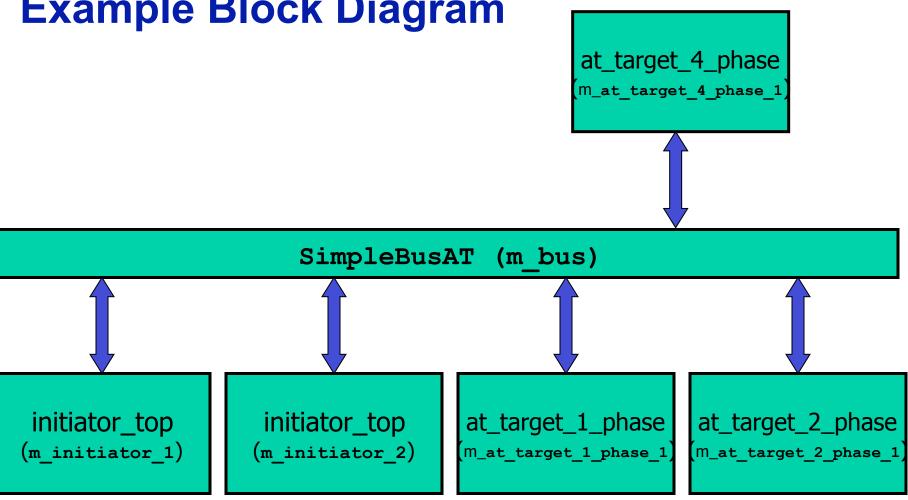
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AT System Example - Annotated Timing

- The Goal is to Illustrate:
 - Application of TLM 2.0 in a real system
 - Illustrate interoperability of different AT styles
- Possible Applications:
 - Architectural exploration
 - Early software development
 - Continued modeling with available models



Example Block Diagram





TLM 2 GP



How to run this example (Linux)

- Set SYSTEMC HOME and TLM HOME
- cd examples/tlm/at_1_phase/build-unix
- make clean
- make
- make run



How to run this example (MSVC)

- Open a explorer window on examples/tlm/at_1_phase/build-windows
- Launch at_1_phase.sln
- Select 'Property Manager' from the 'View' menu
- Under 'at_1_phase > Debug | Win32' select 'systemc'
- Select 'Properties' from the 'View' menu
- Select 'User Macros' under 'Common Properties'
- Update the 'SYSTEMC' and 'TLM' entries and apply
- Build and run



Expected Output – Target ID: 201

```
Info: traffic generator.cpp: 0 s - traffic generator thread
      Initiator: 101 Starting Traffic
Info: select initiator.cpp: 0 s - initiator thread
      Initiator: 101 starting new transaction for Addr:0x00000100
      Initiator: 101 nb transport fw (GP, BEGIN REQ, 0 s)
Info: select initiator.cpp: 0 s - initiator thread
      Initiator: 101 ACCEPTED (GP, BEGIN REQ, 0 s)
      Initiator: 101 transaction waiting end-request on backward-path
Info: at target 1 phase.cpp: 0 s - nb transport fw
      Target: 201 nb transport fw (GP, BEGIN REQ, 0 s)
Info: memory.cpp: 0 s - print
      ID: 201 COMMAND: WRITE Length: 04
      Addr: 0x0000000000000100 Data: 0x00000100
Info: at target 1 phase.cpp: 0 s - nb transport fw
      Target: 201 COMPLETED (GP, BEGIN REQ, 40 ns)
Info: select initiator.cpp: 40 ns - nb transport bw
      Initiator: 101 nb transport bw (GP, BEGIN RESP, 0 s) from Addr: 0x00000100
      Initiator: 101 target omitted end-request timing-point returning ACCEPTED
```



Expected Output – Target ID: 202

```
Info: select initiator.cpp: 0 s - initiator thread
      Initiator: 102 starting new transaction for Addr:0x10000200
      Initiator: 102 nb transport fw (GP, BEGIN REQ, 0 s)
Info: select initiator.cpp: 0 s - initiator thread
      Initiator: 102 ACCEPTED (GP, BEGIN REQ, 0 s)
      Initiator: 102 transaction waiting end-request on backward-path
Info: select initiator.cpp: 50 ns - nb transport bw
      Initiator: 102 nb transport bw (GP, END REQ, 0 s) from Addr: 0x00000200
      Initiator: 102 transaction waiting begin-response on backward path
      Initiator: 102 ACCEPTED (GP, END REQ, 0 s)
Info: at target 2 phase.cpp: 80 ns - begin response method
      Target: 202 starting response method
Info: memory.cpp: 80 ns - print
      ID: 202 COMMAND: WRITE Length: 04
      Addr: 0x0000000000000000000 Data: 0x10000200
Info: at target 2 phase.cpp: 80 ns - begin response method
      Target: 202 nb transport bw (GP, BEGIN RESP, SC ZERO TIME)
Info: at target 2 phase.cpp: 80 ns - begin response method
      Target: 202 ACCEPTED (GP, BEGIN RESP, 0 s)
Info: select initiator.cpp: 80 ns - nb transport bw
      Initiator: 102 nb transport bw (GP, BEGIN RESP, 0 s)from Addr:0x00000200
      Initiator: 102 transaction moved to send-end-response PEQ
      Initiator: 102 ACCEPTED (GP, BEGIN RESP, 0 s)
Info: select initiator.cpp: 87 ns - send end rsp method
      Initiator: 102 starting send-end-response method
      Initiator: 102 nb transport fw (GP, END RESP, 0 s)
Info: select initiator.cpp: 87 ns - send end rsp method
      Initiator: 102 COMPLETED (GP, END RESP, 0 s)
```

Expected Output – Target ID: 203 (1 of 2)

```
Info: select initiator.cpp: 1974 ns - initiator thread
      Initiator: 102 starting new transaction for Addr:0x20000200
      Initiator: 102 nb transport fw (GP, BEGIN REQ, 0 s)
Info: select initiator.cpp: 1974 ns - initiator thread
      Initiator: 102 ACCEPTED (GP, BEGIN REQ, 0 s)
      Initiator: 102 transaction waiting end-request on backward-path
Info: at target 4 phase.cpp: 1974 ns - nb transport fw
      Target: 203 nb transport fw (GP, BEGIN REQ, 0 s)
      Target: 203 ACCEPTED (GP, BEGIN REQ, 0 s)
Info: at target 4 phase.cpp: 1984 ns - end request method
      Target: 203 starting end-request method
                                                                    Address
      Target: 203 transaction moved to send-response PEQ
                                                                    modified
      Target: 203 nb transport bw (GP, END REQ, 0 s)
                                                                    by router!
Info: at target 4 phase.cpp: 1984 ns - end request method
      Target: 203 ACCEPTED (GP, END REQ, 0 s)
Info: select initiator.cpp: 1984 ns - nb transport bw
      Initiator: 102 nb transport bw (GP, END REQ, 0 s) from Addr: 0x00000200
      Initiator: 102 transaction waiting begin-response on backward path
      Initiator: 102 ACCEPTED (GP, END REQ, 0 s)
```

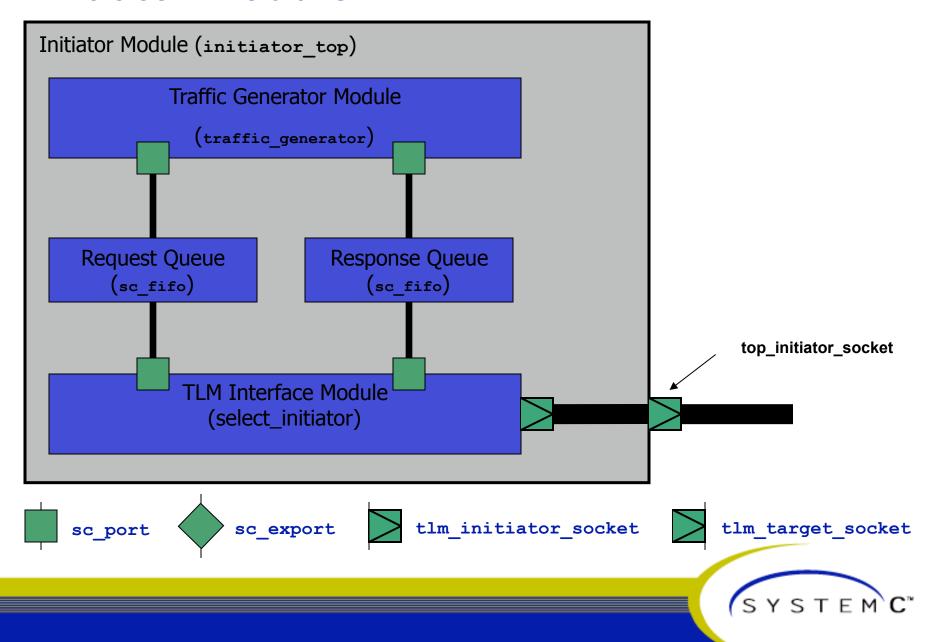
SVSTEMC

Expected Output – Target ID: 203 (2 of 2)

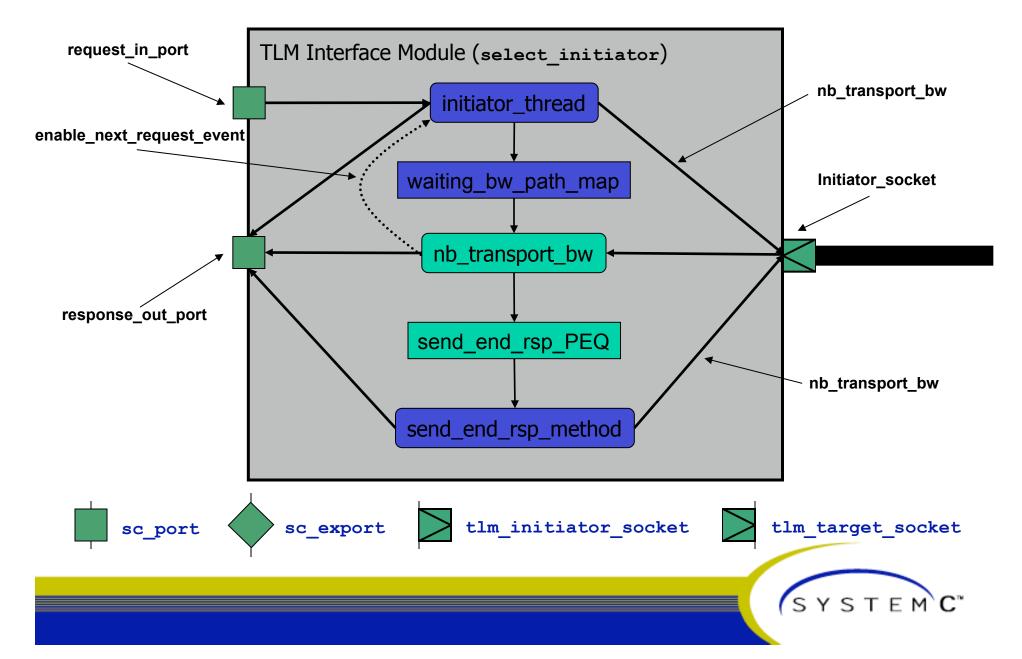
```
Info: at target 4 phase.cpp: 2014 ns - begin response method
      Target: 203 starting response method
Info: memory.cpp: 2014 ns - print
      ID: 203 COMMAND: WRITE Length: 04
      Addr: 0x00000000000000000000 Data: 0xDFFFFDFF
Info: at target 4 phase.cpp: 2014 ns - begin response method
      Target: 203 nb transport bw (GP, BEGIN RESP, SC ZERO TIME)
Info: at target 4 phase.cpp: 2014 ns - begin response method
      Target: 203 ACCEPTED (GP, BEGIN RESP, 0 s)
Info: select initiator.cpp: 2014 ns - nb transport bw
      Initiator: 102 nb transport bw (GP, BEGIN RESP, 0 s) from Addr: 0x00000200
      Initiator: 102 transaction moved to send-end-response PEQ
      Initiator: 102 ACCEPTED (GP, BEGIN RESP, 0 s)
Info: select initiator.cpp: 2021 ns - send end rsp method
      Initiator: 102 starting send-end-response method
      Initiator: 102 nb transport fw (GP, END RESP, 0 s)
Info: select initiator.cpp: 2021 ns - send end rsp method
      Initiator: 102 COMPLETED (GP, END RESP, 0 s
```



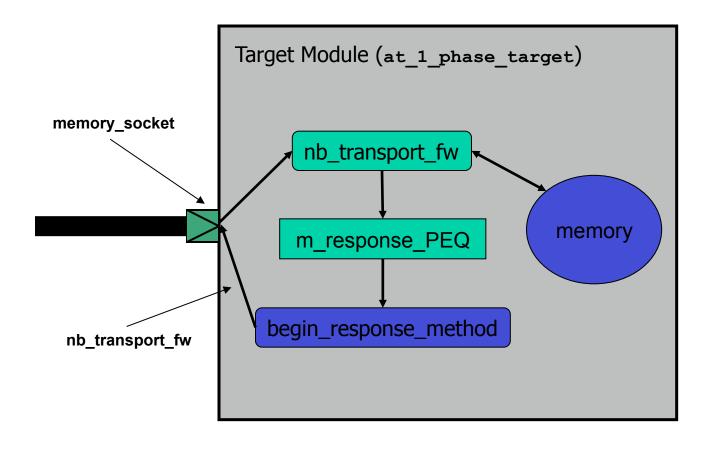
Initiator Module

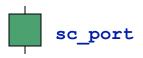


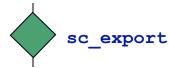
TLM Interface Module

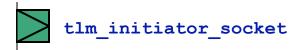


Target Module





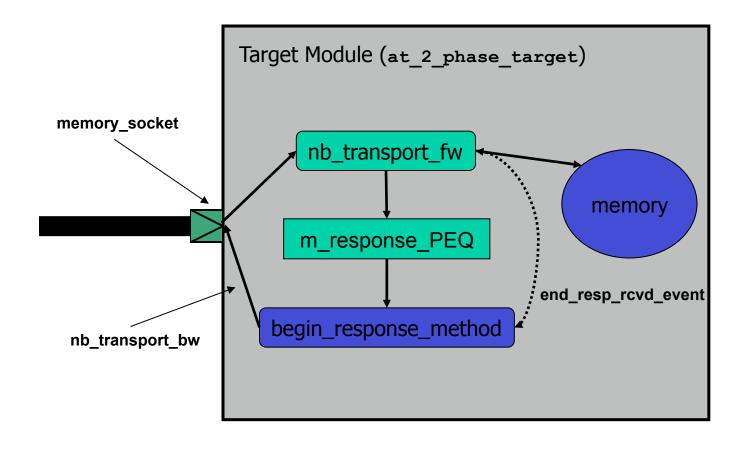






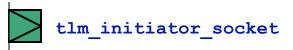


Target Module





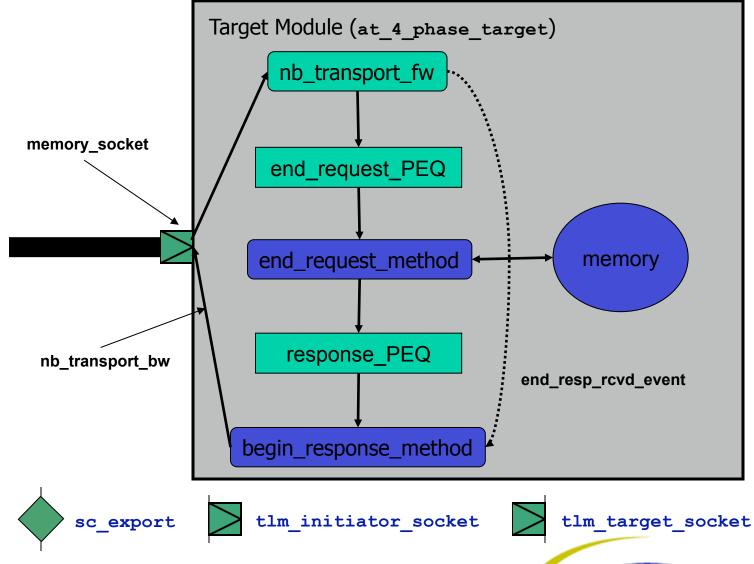








Target Module



Router Component

