1. Description

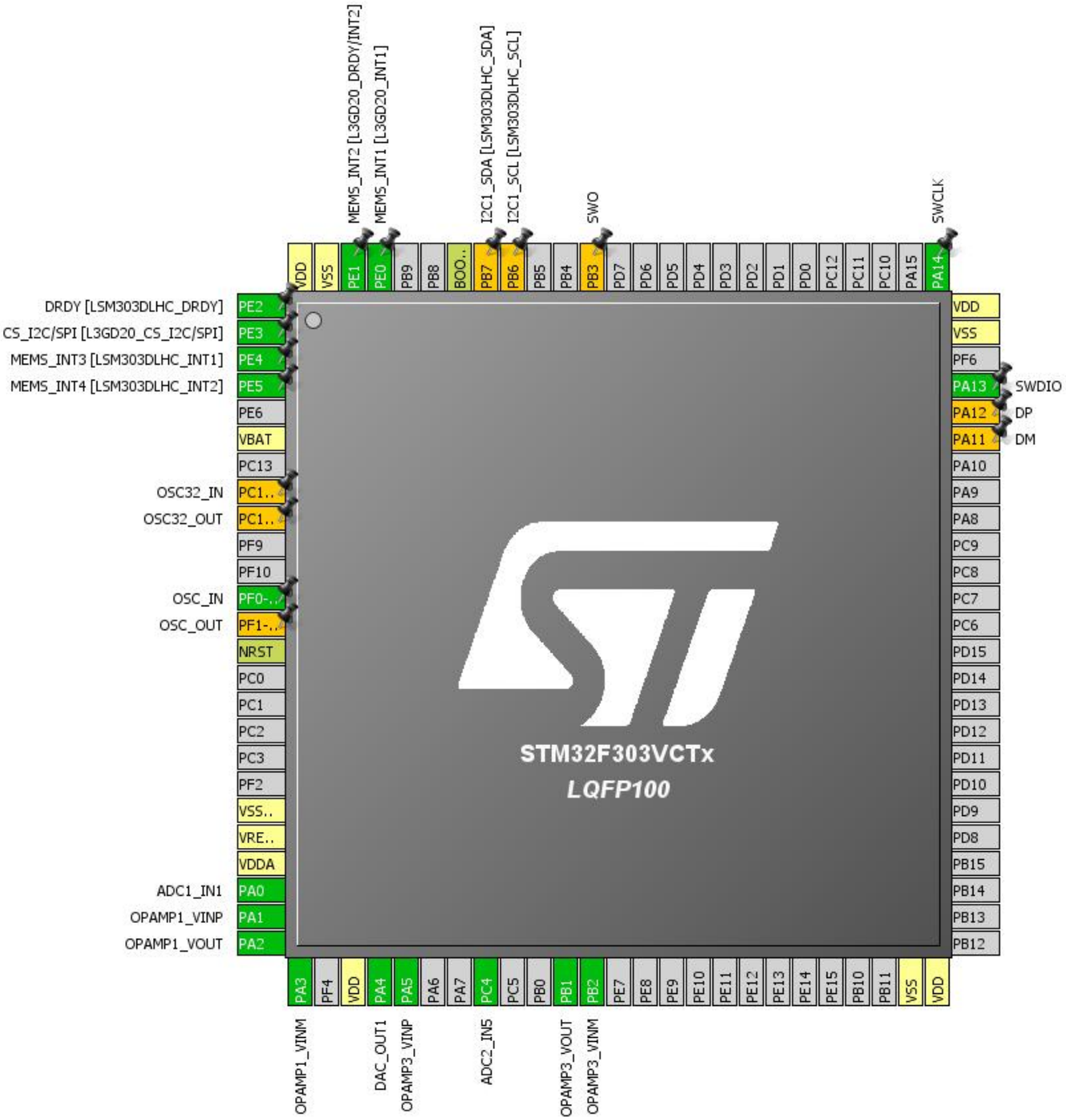
1.1. Project

Project Name	ADC_T_Ecl
Board Name	STM32F3DISCOVERY
Generated with:	STM32CubeMX 4.25.0
Date	06/04/2018

1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303VCTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



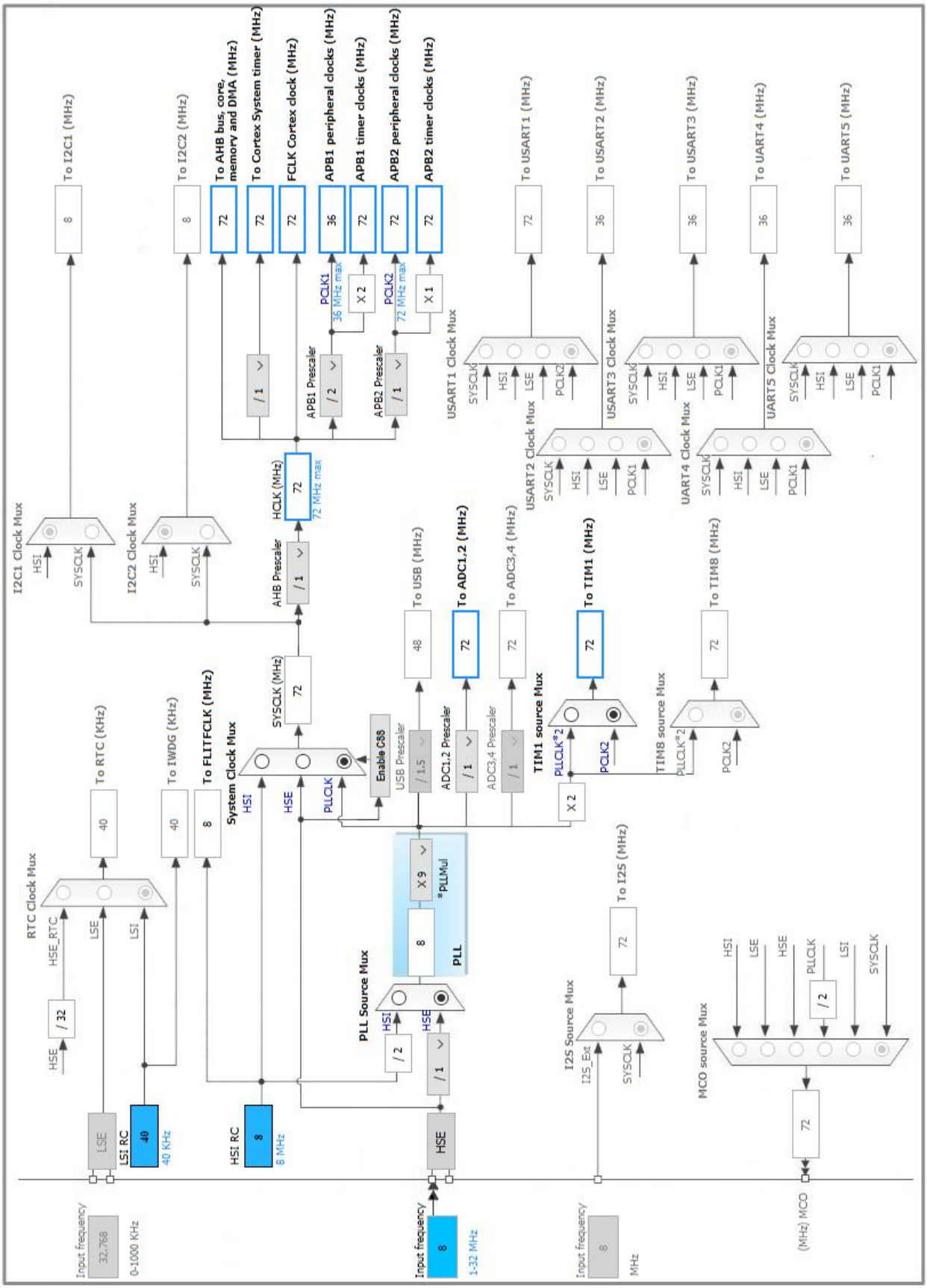
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	GPIO_EXTI2	DRDY [LSM303DLHC_DRDY]
2	PE3 *	I/O	GPIO_Output	CS_I2C/SPI [L3GD20_CS_I2C/SPI]
3	PE4	I/O	GPIO_EXTI4	MEMS_INT3 [LSM303DLHC_INT1]
4	PE5	I/O	GPIO_EXTI5	MEMS_INT4 [LSM303DLHC_INT2]
6	VBAT	Power		
8	PC14-OSC32_IN **	I/O	RCC_OSC32_IN	OSC32_IN
9	PC15-OSC32_OUT **	I/O	RCC_OSC32_OUT	OSC32_OUT
12	PF0-OSC_IN	I/O	RCC_OSC_IN	OSC_IN
13	PF1-OSC_OUT **	I/O	RCC_OSC_OUT	OSC_OUT
14	NRST	Reset		
20	VSSA/VREF-	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0	I/O	ADC1_IN1	
24	PA1	I/O	OPAMP1_VINP	
25	PA2	I/O	OPAMP1_VOUT	
26	PA3	I/O	OPAMP1_VINM	
28	VDD	Power		
29	PA4	I/O	DAC_OUT1	
30	PA5	I/O	OPAMP3_VINP	
33	PC4	I/O	ADC2_IN5	
36	PB1	I/O	OPAMP3_VOUT	
37	PB2	I/O	OPAMP3_VINM	
49	VSS	Power		
50	VDD	Power		
70	PA11 **	I/O	USB_DM	DM
71	PA12 **	I/O	USB_DP	DP
72	PA13	I/O	SYS_JTMS-SWDIO	SWDIO
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	SWCLK
89	PB3 **	I/O	SYS_JTDO-TRACESWO	SWO

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
92	PB6 **	I/O	I2C1_SCL	I2C1_SCL [LSM303DLHC_SCL]
93	PB7 **	I/O	I2C1_SDA	I2C1_SDA [LSM303DLHC_SDA]
94	BOOT0	Boot		
97	PE0	I/O	GPIO_EXTI0	MEMS_INT1 [L3GD20_INT1]
98	PE1	I/O	GPIO_EXTI1	MEMS_INT2 [L3GD20_DRDY/INT2]
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function
** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

IN1: IN1 Single-ended

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 1
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.2. ADC2

IN5: IN5 Single-ended

5.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 5
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.3. DAC

mode: OUT1 Configuration

5.3.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	**Timer 6 Trigger Out event ***
Wave generation mode	Disabled

5.4. OPAMP1

Mode: Standalone

5.4.1. Parameter Settings:

Basic Parameters:

User Trimming	Disable

5.5. OPAMP3

Mode: Standalone

5.5.1. Parameter Settings:

Basic Parameters:

User Trimming	Disable

5.6. RCC

High Speed Clock (HSE): BYPASS Clock Source

5.6.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

5.7. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.8. TIM1

Clock Source : Internal Clock

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**719 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***
Trigger Event Selection TRGO2	**Update Event ***

5.9. TIM6

mode: Activated

5.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**112 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	**Update Event ***

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN1	Analog mode	No pull up pull down	n/a	
ADC2	PC4	ADC2_IN5	Analog mode	No pull up pull down	n/a	
DAC	PA4	DAC_OUT1	Analog mode	No pull up pull down	n/a	
OPAMP1	PA1	OPAMP1_VINP	Analog mode	No pull up pull down	n/a	
	PA2	OPAMP1_VOUT	Analog mode	No pull up pull down	n/a	
	PA3	OPAMP1_VINM	Analog mode	No pull up pull down	n/a	
OPAMP3	PA5	OPAMP3_VINP	Analog mode	No pull up pull down	n/a	
	PB1	OPAMP3_VOUT	Analog mode	No pull up pull down	n/a	
	PB2	OPAMP3_VINM	Analog mode	No pull up pull down	n/a	
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	OSC_IN
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	SWDIO
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	SWCLK
Single Mapped Signals	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	OSC32_IN
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	OSC32_OUT
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	OSC_OUT
	PA11	USB_DM	Alternate Function Push Pull	No pull up pull down	**High ***	DM
	PA12	USB_DP	Alternate Function Push Pull	No pull up pull down	**High ***	DP
	PB3	SYS_JTDO-TRACESWO	n/a	n/a	**n/a**	SWO
	PB6	I2C1_SCL	Alternate Function Open Drain	Pull up	**High ***	I2C1_SCL [LSM303DLHC_SCL]
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull up	**High ***	I2C1_SDA [LSM303DLHC_SDA]
GPIO	PE2	GPIO_EXTI2	**External Event Mode with Rising edge trigger detection ***	No pull up pull down	n/a	DRDY [LSM303DLHC_DRDY]
	PE3	GPIO_Output	Output Push Pull	No pull up pull down	Low	CS_I2C/SPI [L3GD20_CS_I2C/SPI]
	PE4	GPIO_EXTI4	**External Event Mode**	No pull up pull down	n/a	MEMS_INT3 [LSM303DLHC_INT1]

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
			with Rising edge trigger detection *			
	PE5	GPIO_EXTI5	**External Event Mode with Rising edge trigger detection ***	No pull up pull down	n/a	MEMS_INT4 [LSM303DLHC_INT2]
	PE0	GPIO_EXTI0	**External Event Mode with Rising edge trigger detection ***	No pull up pull down	n/a	MEMS_INT1 [L3GD20_INT1]
	PE1	GPIO_EXTI1	**External Event Mode with Rising edge trigger detection ***	No pull up pull down	n/a	MEMS_INT2 [L3GD20_DRDY/INT2]

6.2. DMA configuration

DMA request	Stream	Direction	Priority
DAC_CH1	DMA1_Channel3	Memory To Peripheral	Low

DAC_CH1: DMA1_Channel3 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel3 global interrupt	true	0	0
PVD interrupt through EXTI line16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 interrupts	unused		
TIM1 break and TIM15 interrupts	unused		
TIM1 update and TIM16 interrupts	unused		
TIM1 trigger, commutation and TIM17 interrupts	unused		
TIM1 capture compare interrupt	unused		
Timer 6 interrupt and DAC underrun interrupts	unused		
Floating point unit interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303VCTx
Datasheet	023353_Rev13

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	ADC_T_Ecl
Project Folder	D:\Embedded LAB\ADC_Test\ADC_T_Ecl
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F3 V1.9.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report