Address	Name	Access	OCS	ECS	AGA	SAGA	Description
DFF000	BLTDDAT	ER	*	*	*	*	Blitter dest. early read (dummy address)
DFF002	DMACONR	R	*	*	*	*	Dma control (and blitter status) read
DFF004	VPOSR	R	*	*	*	*	Read vertical most sig. bits (and frame flop)
DFF006	VHPOSR	R	*	*	*	*	Read vert and horiz position of beam
DFF008	DSKDATR	ER	*	*	*	*	Disk data early read (dummy address)
DFF00A	JOY0DAT	R	*	*	*	*	Joystick-mouse 0 data (vert, horiz)
DFF00C	JOY1DAT	R	*	*	*	*	Joystick-mouse 1 data (vert, horiz)
DFF00E	CLXDAT	R	*	*	*	*	Collision data reg. (read and clear)
DFF010	ADKCONR	R	*	*	*	*	Audio,disk control register read
DFF012	POT0DAT	R	*	*	*	*	Pot counter data left pair (vert, horiz)
DFF014	POT1DAT	R	*	*	*	*	Pot counter data right pair (vert, horiz)
DFF016	POTINP	R	*	*	*	*	Pot pin data read
DFF018	SERDATR	R	*	*	*	*	Serial port data and status read
DFF01A	DSKBYTR	R	*	*	*	*	Disk data byte and status read
DFF01C	INTENAR	R	*	*	*	*	Interrupt enable bits read
DFF01E	INTREQR	R	*	*	*	*	Interrupt request bits read
DFF020	DSKPTH	W	*	*	*	*	Disk pointer (high 5 bits, was 3 bits)
DFF022	DSKPTL	W	*	*	*	*	Disk pointer (low 15 bits)
DFF024	DSKLEN	W	*	*	*	*	Disk length
DFF026	DSKDAT	W	*	*	*	*	Disk DMA data write
DFF028	REFPTR	W	*	*	*	*	Refresh pointer
DFF02A	VPOSW	W	*	*	*	*	Write vert most sig. bits (and frame flop)
DFF02C	VHPOSW	W	*	*	*	*	Write vert and horiz pos of beam
DFF02E	COPCON	W	*	*	*	*	Coprocessor control
DFF030	SERDAT	W	*	*	*	*	Serial port data and stop bits write
DFF032	SERPER	W	*	*	*	*	Serial port period and control
DFF034	POTGO	W	*	*	*	*	Pot count start,pot pin drive enable data
DFF036	JOYTEST	W	*	*	*	*	Write to all 4 joystick-mouse counters at once
DFF038	STREQU	S	*	*	*	*	Strobe for horiz sync with VB and EQU
DFF03A	STRVBL	S	*	*	*	*	Strobe for horiz sync with VB (vert blank)
DFF03C	STRHOR	S	*	*	*	*	Strobe for horiz sync

DFF03E	STRLONG	S	*	*	*	*	Strobe for identification of long horiz line
DFF040	BLTCON0	W	*	*	*	*	Blitter control register 0
DFF042	BLTCON1	W	*	*	*	*	Blitter control register 1
DFF044	BLTAFWM	W	*	*	*	*	Blitter first word mask for source A
DFF046	BLTALWM	W	*	*	*	*	Blitter last word mask for source A
DFF048	BLTCPTH	W	*	*	*	*	Blitter pointer to source C (high 5 bits, was 3 bits)
DFF04A	BLTCPTL	W	*	*	*	*	Blitter pointer to source C (low 15 bits)
DFF04C	BLTBPTH	W	*	*	*	*	Blitter pointer to source B (high 5 bits, was 3 bits)
DFF04E	BLTBPTL	W	*	*	*	*	Blitter pointer to source B (low 15 bits)
DFF050	BLTAPTH	W	*	*	*	*	Blitter pointer to source A (high 5 bits, was 3 bits)
DFF052	BLTAPTL	W	*	*	*	*	Blitter pointer to source A (low 15 bits)
DFF054	BLTDPTH	W	*	*	*	*	Blitter pointer to dest D (high 5 bits, was 3 bits)
DFF056	BLTDPTL	W	*	*	*	*	Blitter pointer to dest D (low 15 bits)
DFF058	BLTSIZE	W	*	*	*	*	Blitter start and size (win/width,height)
DFF05A	BLTCON0L	W		*	*	*	Blitter control 0, lower 8 bits (minterms)
DFF05C	BLTSIZV	W		*	*	*	Blitter V size (for 15 bit vertical size)
DFF05E	BLTSIZH	W		*	*	*	Blitter H size and start (for 11 bit H size)
DFF060	BLTCMOD	W	*	*	*	*	Blitter modulo for source C
DFF062	BLTBMOD	W	*	*	*	*	Blitter modulo for source B
DFF064	BLTAMOD	W	*	*	*	*	Blitter modulo for source A
DFF066	BLTDMOD	W	*	*	*	*	Blitter modulo for dest D
DFF070	BLTCDAT	W	*	*	*	*	Blitter source C data register
DFF072	BLTBDAT	W	*	*	*	*	Blitter source B data register
DFF074	BLTADAT	W	*	*	*	*	Blitter source A data register
DFF078	SPRHDAT	W		*	*	*	Ext. logic UHRES sprite pointer and data identifier
DFF07A	BPLHDAT	W		*	*	*	Ext. logic UHRES bit plane identifier
DFF07C	DENISEID	R		*	*	*	Chip revision level for Denise/Lisa (video out chip)
DFF07E	DSKSYNC	W	*	*	*	*	Disk sync pattern reg for disk read
DFF080	COP1LCH	W	*	*	*	*	Coprocessor 1st location (high 5 bits,was 3 bits)

DFF082	COP1LCL	W	*	*	*	*	Coprocessor 1st location (low 15 bits)
DFF084	COP2LCH	W	*	*	*	*	Coprocessor 2nd location(high 5 bits,was 3 bits)
DFF086	COP2LCL	W	*	*	*	*	Coprocessor 2nd location (low 15 bits)
DFF088	COPJMP1	S	*	*	*	*	Coprocessor restart at 1st location
DFF08A	COPJMP2	S	*	*	*	*	Coprocessor restart at 2nd location
DFF08C	COPINS	S	*	*	*	*	Coprocessor inst fetch identify
DFF08E	DIWSTRT	W	*	*	*	*	Display window start (upper left vert,horiz pos)
DFF090	DIWSTOP	W	*	*	*	*	Display window stop (lower right vert,horiz pos)
DFF092	DDFSTRT	W	*	*	*	*	Display bit plane data fetch start,horiz pos
DFF094	DDFSTOP	W	*	*	*	*	Display bit plane data fetch stop,horiz pos
DFF096	DMACON	W	*	*	*	*	DMA control write (clear or set)
DFF098	CLXCON	W	*	*	*	*	Collision control
DFF09A	INTENA	W	*	*	*	*	Interrupt enable bits (clear or set bits)
DFF09C	INTREQ	W	*	*	*	*	Interrupt request bits (clear or set bits)
DFF09E	ADKCON	W	*	*	*	*	Audio,disk,UART control
DFF0A0	AUD0LCH	W	*	*	*	*	Audio channel 0 location (high 5 bits was 3 bits)
DFF0A2	AUD0LCL	W	*	*	*	*	Audio channel 0 location (low 15 bits)
DFF0A4	AUD0LEN	W	*	*	*	*	Audio channel 0 length
DFF0A6	AUD0PER	W	*	*	*	*	Audio channel 0 period
DFF0A8	AUD0VOL	W	*	*	*	*	Audio channel 0 volume
DFF0AA	AUD0DAT	W	*	*	*	*	Audio channel 0 data
DFF0B0	AUD1LCH	W	*	*	*	*	Audio channel 1 location (high 5 bits was 3 bits)
DFF0B2	AUD1LCL	W	*	*	*	*	Audio channel 1 location (low 15 bits)
DFF0B4	AUD1LEN	W	*	*	*	*	Audio channel 1 length
DFF0B6	AUD1PER	W	*	*	*	*	Audio channel 1 period
DFF0B8	AUD1VOL	W	*	*	*	*	Audio channel 1 volume
DFF0BA	AUD1DAT	W	*	*	*	*	Audio channel 1 data
DFF0C0	AUD2LCH	W	*	*	*	*	Audio channel 2 location (high 5 bits was 3 bits)
DFF0C2	AUD2LCL	W	*	*	*	*	Audio channel 2 location (low 15 bits)
DFF0C4	AUD2LEN	W	*	*	*	*	Audio channel 2 length
DFF0C6	AUD2PER	W	*	*	*	*	Audio channel 2 period
DFF0C8	AUD2VOL	W	*	*	*	*	Audio channel 2 volume

DFF0CA	AUD2DAT	W	*	*	*	*	Audio channel 2 data
DFF0CC	AUD2VOL2	W				*	Audio channel 2 volume far side
DFF0D0	AUD3LCH	W	*	*	*	*	Audio channel 3 location (high 5 bits was 3 bits)
DFF0D2	AUD3LCL	W	*	*	*	*	Audio channel 3 location (low 15 bits)
DFF0D4	AUD3LEN	W	*	*	*	*	Audio channel 3 length
DFF0D6	AUD3PER	W	*	*	*	*	Audio channel 3 period
DFF0D8	AUD3VOL	W	*	*	*	*	Audio channel 3 volume
DFF0DA	AUD3DAT	W	*	*	*	*	Audio channel 3 data
DFF0E0	BPL1PTH	W	*	*	*	*	Bitplane pointer 1 (high 5 bits was 3 bits)
DFF0E2	BPL1PTL	W	*	*	*	*	Bitplane pointer 1 (low 15 bits)
DFF0E4	BPL2PTH	W	*	*	*	*	Bitplane pointer 2 (high 5 bits was 3 bits)
DFF0E6	BPL2PTL	W	*	*	*	*	Bitplane pointer 2 (low 15 bits)
DFF0E8	BPL3PTH	W	*	*	*	*	Bitplane pointer 3 (high 5 bits was 3 bits)
DFF0EA	BPL3PTL	W	*	*	*	*	Bitplane pointer 3 (low 15 bits)
DFF0EC	BPL4PTH	W	*	*	*	*	Bitplane pointer 4 (high 5 bits was 3 bits)
DFF0EE	BPL4PTL	W	*	*	*	*	Bitplane pointer 4 (low 15 bits)
DFF0F0	BPL5PTH	W	*	*	*	*	Bitplane pointer 5 (high 5 bits was 3 bits)
DFF0F2	BPL5PTL	W	*	*	*	*	Bitplane pointer 5 (low 15 bits)
DFF0F4	BPL6PTH	W	*	*	*	*	Bitplane pointer 6 (high 5 bits was 3 bits)
DFF0F6	BPL6PTL	W	*	*	*	*	Bitplane pointer 6 (low 15 bits)
DFF0F8	BPL7PTH	W			*	*	Bitplane pointer 7 (high 5 bits was 3 bits)
DFF0FA	BPL7PTL	W			*	*	Bitplane pointer 7 (low 15 bits)
DFF0FC	BPL8PTH	W			*	*	Bitplane pointer 8 (high 5 bits was 3 bits)
DFF0FE	BPL8PTL	W			*	*	Bitplane pointer 8 (low 15 bits)
DFF100	BPLCON0	W	*	*	*	*	Bitplane control (miscellaneous control bits)
DFF102	BPLCON1	W	*	*	*	*	Bitplane control (scroll value)
DFF104	BPLCON2	W	*	*	*	*	Bitplane control (video priority control)
DFF106	BPLCON3	W	*	*	*	*	Bitplane control (enhanced features)
DFF108	BPL1MOD	W	*	*	*	*	Bitplane modulo (odd planes)
DFF10A	BPL2MOD	W	*	*	*	*	Bitplane modulo (even planes)

DFF10C	BPLCON4	W			*	*	Bitplane control (bitplane and sprite-masks)
DFF10E	CLXCON2	W			*	*	Extended collision control
DFF110	BPL1DAT	W	*	*	*	*	Bitplane 1 data (parallel to serial convert)
DFF112	BPL2DAT	W	*	*	*	*	Bitplane 2 data (parallel to serial convert)
DFF114	BPL3DAT	W	*	*	*	*	Bitplane 3 data (parallel to serial convert)
DFF116	BPL4DAT	W	*	*	*	*	Bitplane 4 data (parallel to serial convert)
DFF118	BPL5DAT	W	*	*	*	*	Bitplane 5 data (parallel to serial convert)
DFF11A	BPL6DAT	W	*	*	*	*	Bitplane 6 data (parallel to serial convert)
DFF11C	BPL7DAT	W			*	*	Bitplane 7 data (parallel to serial convert)
DFF11E	BPL8DAT	W			*	*	Bitplane 8 data (parallel to serial convert)
DFF120	SPR0PTH	W	*	*	*	*	Sprite 0 pointer (high 5 bits was 3 bits)
DFF122	SPR0PTL	W	*	*	*	*	Sprite 0 pointer (low 15 bits)
DFF124	SPR1PTH	W	*	*	*	*	Sprite 1 pointer (high 5 bits was 3 bits)
DFF126	SPR1PTL	W	*	*	*	*	Sprite 1 pointer (low 15 bits)
DFF128	SPR2PTH	W	*	*	*	*	Sprite 2 pointer (high 5 bits was 3 bits)
DFF12A	SPR2PTL	W	*	*	*	*	Sprite 2 pointer (low 15 bits)
DFF12C	SPR3PTH	W	*	*	*	*	Sprite 3 pointer (high 5 bits was 3 bits)
DFF12E	SPR3PTL	W	*	*	*	*	Sprite 3 pointer (low 15 bits)
DFF130	SPR4PTH	W	*	*	*	*	Sprite 4 pointer (high 5 bits was 3 bits)
DFF132	SPR4PTL	W	*	*	*	*	Sprite 4 pointer (low 15 bits)
DFF134	SPR5PTH	W	*	*	*	*	Sprite 5 pointer (high 5 bits was 3 bits)
DFF136	SPR5PTL	W	*	*	*	*	Sprite 5 pointer (low 15 bits)
DFF138	SPR6PTH	W	*	*	*	*	Sprite 6 pointer (high 5 bits was 3 bits)
DFF13A	SPR6PTL	W	*	*	*	*	Sprite 6 pointer (low 15 bits)
DFF13C	SPR7PTH	W	*	*	*	*	Sprite 7 pointer (high 5 bits was 3 bits)

DFF13E	SPR7PTL	W	*	*	*	*	Sprite 7 pointer (low 15 bits)
DFF140	SPR0POS	W	*	*	*	*	Sprite 0 vert,horiz start pos data
DFF142	SPR0CTL	W	*	*	*	*	Sprite 0 position and control data
DFF144	SPR0DATA	W	*	*	*	*	Sprite 0 image data register A
DFF146	SPR0DATB	W	*	*	*	*	Sprite 0 image data register B
DFF148	SPR1POS	W	*	*	*	*	Sprite 1 vert,horiz start pos data
DFF14A	SPR1CTL	W	*	*	*	*	Sprite 1 position and control data
DFF14C	SPR1DATA	W	*	*	*	*	Sprite 1 image data register A
DFF14E	SPR1DATB	W	*	*	*	*	Sprite 1 image data register B
DFF150	SPR2POS	W	*	*	*	*	Sprite 2 vert,horiz start pos data
DFF152	SPR2CTL	W	*	*	*	*	Sprite 2 position and control data
DFF154	SPR2DATA	W	*	*	*	*	Sprite 2 image data register A
DFF156	SPR2DATB	W	*	*	*	*	Sprite 2 image data register B
DFF158	SPR3POS	W	*	*	*	*	Sprite 3 vert,horiz start pos data
DFF15A	SPR3CTL	W	*	*	*	*	Sprite 3 position and control data
DFF15C	SPR3DATA	W	*	*	*	*	Sprite 3 image data register A
DFF15E	SPR3DATB	W	*	*	*	*	Sprite 3 image data register B
DFF160	SPR4POS	W	*	*	*	*	Sprite 4 vert,horiz start pos data
DFF162	SPR4CTL	W	*	*	*	*	Sprite 4 position and control data
DFF164	SPR4DATA	W	*	*	*	*	Sprite 4 image data register A
DFF166	SPR4DATB	W	*	*	*	*	Sprite 4 image data register B
DFF168	SPR5POS	W	*	*	*	*	Sprite 5 vert,horiz start pos data
DFF16A	SPR5CTL	W	*	*	*	*	Sprite 5 position and control data
DFF16C	SPR5DATA	W	*	*	*	*	Sprite 5 image data register A
DFF16E	SPR5DATB	W	*	*	*	*	Sprite 5 image data register B
DFF170	SPR6POS	W	*	*	*	*	Sprite 6 vert,horiz start pos data
DFF172	SPR6CTL	W	*	*	*	*	Sprite 6 position and control data
DFF174	SPR6DATA	W	*	*	*	*	Sprite 6 image data register A
DFF176	SPR6DATB	W	*	*	*	*	Sprite 6 image data register B
DFF178	SPR7POS	W	*	*	*	*	Sprite 7 vert,horiz start pos data
DFF17A	SPR7CTL	W	*	*	*	*	Sprite 7 position and control data
DFF17C	SPR7DATA	W	*	*	*	*	Sprite 7 image data register A
DFF17E	SPR7DATB	W	*	*	*	*	Sprite 7 image data register B
DFF180	COLOR00	W	*	*	*	*	Color table 0
DFF182	COLOR01	W	*	*	*	*	Color table 1
DFF184	COLOR02	W	*	*	*	*	Color table 2
DFF186	COLOR03	W	*	*	*	*	Color table 3
DFF188	COLOR04	W	*	*	*	*	Color table 4

DFF18A	COLOR05	W	*	*	*	*	Color table 5
DFF18C	COLOR06	W	*	*	*	*	Color table 6
DFF18E	COLOR07	W	*	*	*	*	Color table 7
DFF190	COLOR08	W	*	*	*	*	Color table 8
DFF192	COLOR09	W	*	*	*	*	Color table 9
DFF194	COLOR10	W	*	*	*	*	Color table 10
DFF196	COLOR11	W	*	*	*	*	Color table 11
DFF198	COLOR12	W	*	*	*	*	Color table 12
DFF19A	COLOR13	W	*	*	*	*	Color table 13
DFF19C	COLOR14	W	*	*	*	*	Color table 14
DFF19E	COLOR15	W	*	*	*	*	Color table 15
DFF1A0	COLOR16	W	*	*	*	*	Color table 16
DFF1A2	COLOR17	W	*	*	*	*	Color table 17
DFF1A4	COLOR18	W	*	*	*	*	Color table 18
DFF1A6	COLOR19	W	*	*	*	*	Color table 19
DFF1A8	COLOR20	W	*	*	*	*	Color table 20
DFF1AA	COLOR21	W	*	*	*	*	Color table 21
DFF1AC	COLOR22	W	*	*	*	*	Color table 22
DFF1AE	COLOR23	W	*	*	*	*	Color table 23
DFF1B0	COLOR24	W	*	*	*	*	Color table 24
DFF1B2	COLOR25	W	*	*	*	*	Color table 25
DFF1B4	COLOR26	W	*	*	*	*	Color table 26
DFF1B6	COLOR27	W	*	*	*	*	Color table 27
DFF1B8	COLOR28	W	*	*	*	*	Color table 28
DFF1BA	COLOR29	W	*	*	*	*	Color table 29
DFF1BC	COLOR30	W	*	*	*	*	Color table 30
DFF1BE	COLOR31	W	*	*	*	*	Color table 31
DFF1C0	HTOTAL	W		*	*	*	Highest number count, horiz line (VARBEAMEN=1)
DFF1C2	HSSTOP	W		*	*	*	Horizontal line position for HSYNC stop
DFF1C4	HBSTRT	W		*	*	*	Horizontal line position for HBLANK start
DFF1C6	HBSTOP	W		*	*	*	Horizontal line position for HBLANK stop
DFF1C8	VTOTAL	W		*	*	*	Highest numbered vertical line (VARBEAMEN=1)
DFF1CA	VSSTOP	W		*	*	*	Vertical line position for VSYNC stop
DFF1CC	VBSTRT	W		*	*	*	Vertical line for VBLANK start

DFF1CE	VBSTOP	W		*	*	*	Vertical line for VBLANK stop
DFF1D0	SPRHSTRT	W		*	*	*	UHRES sprite vertical start
DFF1D2	SPRHSTOP	W		*	*	*	UHRES sprite vertical stop
DFF1D4	BPLHSTRT	W		*	*	*	UHRES bit plane vertical start
DFF1D6	BPLHSTOP	W		*	*	*	UHRES bit plane vertical stop
DFF1D8	HHPOSW	W		*	*	*	DUAL mode hires H beam counter write
DFF1DA	HHPOSR	R		*	*	*	DUAL mode hires H beam counter read
DFF1DC	BEAMCON0	W	*	*	*	*	Beam counter control register (SHRES,UHRES,PAL)
DFF1DE	HSSTRT	W		*	*	*	Horizontal sync start (VARHSY)
DFF1E0	VSSTRT	W		*	*	*	Vertical sync start (VARVSY)
DFF1E2	HCENTER	W		*	*	*	Horizontal position for Vsync on interlace
DFF1E4	DIWHIGH	W		*	*	*	Display window - upper bits for start/stop
DFF1E6	BPLHMOD	W				*	Chunky plane modulo
DFF1E8	SPRHPTH	W		*	*	*	UHRES sprite pointer (high 5 bits)
DFF1EA	SPRHPTL	W		*	*	*	UHRES sprite pointer (low 15 bits)
DFF1EC	BPLHPTH	W				*	Chunky plane pointer (hi 15 bits)
DFF1EE	BPLHPTL	W				*	Chunky plane pointer (lo 15 bits)
DFF1F4	GFXMODE	W				*	Set Resolution and Pixformat
DFF1FC	FMODE	W			*	*	Fetch mode register
Address	**Name**	**Access**	**OCS**	**ECS**	**AGA**	**SAGA**	**Description**
DFF202	DMACON2 Read	R				*	
DFF21c	INTENA2 Read	R				*	
DFF21E	INTREQ2 Read	R				*	
DFF220	joy0buttons	R				*	16bit USB Joy Buttons (0)=active
DFF222	joy1buttons	R				*	16bit USB Joy Buttons (0)=active
DFF224	joy2buttons	R				*	16bit USB Joy Buttons (0)=active
DFF226	joy3buttons	R				*	16bit USB Joy Buttons (0)=active
DFF230	clxdat0	R				*	Sprite0 Detailed Collision
DFF232	clxdat1	R				*	Sprite1 Detailed Collision
DFF234	clxdat2	R				*	Sprite2 Detailed Collision
DFF236	clxdat3	R				*	Sprite3 Detailed Collision
DFF238	clxdat4	R				*	Sprite4 Detailed Collision
DFF23A	clxdat5	R				*	Sprite5 Detailed Collision

DFF23C	clxdat6	R				*	Sprite6 Detailed Collision
DFF23E	clxdat7	R				*	Sprite7 Detailed Collision
DFF296	DMACON2	W				*	DMACON2
DFF29A	INTENA2	W				*	INTENA2
DFF29C	INTREQ2	W				*	INTREQ2
DFF380	PlanarCOLH	W				*	32bit Planar COLOR Port register
DFF382	PlanarCOLL	W				*	256 Color Register, Format [ID,RR,GG,BB]
DFF384	SpriteCOLH	W				*	32bit Sprite COLOR Port register
DFF386	SpriteCOLL	W				*	256 Color Register, Format [ID,RR,GG,BB]
DFF388	ChunkyCOLH	W				*	32bit Chunky COLOR Port register
DFF38A	ChunkyCOLL	W				*	256 Color Register, Format [ID,RR,GG,BB]
DFF38C	PIPCOLH	W				*	32bit PIP COLOR Port register
DFF38E	PIPCOLL	W				*	256 Color Register, Format [ID,RR,GG,BB]
DFF3D0	PipXStrt	W				*	X start
DFF3D2	PipYStrt	W				*	Y start
DFF3D4	PipXStop	W				*	X stop
DFF3D6	PipYStop	W				*	Y stop
DFF3D8	PipPtr	W				*	32 bit Ptr
DFF3DC	PipFormat	W				*	Colorformat (8bit/16bit/15bit/YUV)
DFF3DE	PipModulo	W				*	Modulo
DFF3E0	PipColorKey	W				*	ColorKey 1000,RRRR,GGGG,BBBB
DFF3E2	PipDMARowLen	W				*	PipDMARowLen
DFF3FC	VAMPIRE VERSION	R				*	8bit Card Version / 8bit clock multiplier

Address	Name	Access	OCS	ECS	AGA	SAGA	Description
DFF400	AUD0L	W				*	Audio channel 0 location (32bit PTR)
DFF402	AUD0L	W				*	
DFF404	AUD0LEN	W				*	Audio channel 0 length (32bit)
DFF406	AUD0LEN	W				*	
DFF408	AUD0VOL	W				*	2x8bit VOL (LEFT/RIGHT)
DFF40A	AUD0CTRL	W				*	16 Control bits 2= Stereo 1= Oneshot 0= (8bit/16bit)
DFF40C	AUD0PER	W				*	16bit PERIOD
DFF410	AUD1L	W				*	Audio channel 1 location (32bit PTR)
DFF412	AUD1L	W				*	
DFF414	AUD1LEN	W				*	Audio channel 1 length (32bit)

DFF416	AUD1LEN	W				*	
DFF418	AUD1VOL	W				*	2x8bit VOL (LEFT/RIGHT)
DFF41A	AUD1CTRL	W				*	16 Control bits 2= Stereo 1= Oneshot 0= (8bit/16bit)
DFF41C	AUD1PER	W				*	16bit PERIOD
DFF420	AUD2L	W				*	Audio channel 2 location (32bit PTR)
DFF422	AUD2L	W				*	
DFF424	AUD2LEN	W				*	Audio channel 2 length (32bit)
DFF426	AUD2LEN	W				*	
DFF428	AUD2VOL	W				*	2x8bit VOL (LEFT/RIGHT)
DFF42A	AUD2CTRL	W				*	16 Control bits 2= Stereo 1= Oneshot 0= (8bit/16bit)
DFF42C	AUD2PER	W				*	16bit PERIOD
DFF430	AUD3L	W				*	Audio channel 1 location (32bit PTR)
DFF432	AUD3L	W				*	
DFF434	AUD3LEN	W				*	Audio channel 3 length (32bit)
DFF436	AUD3LEN	W				*	
DFF438	AUD3VOL	W				*	2x8bit VOL (LEFT/RIGHT)
DFF43A	AUD3CTRL	W				*	16 Control bits 2= Stereo 1= Oneshot 0= (8bit/16bit)
DFF43C	AUD3PER	W				*	16bit PERIOD
DFF440	AUD4L	W				*	Audio channel 4 location (32bit PTR)
DFF442	AUD4L	W				*	
DFF444	AUD4LEN	W				*	Audio channel 4 length (32bit)
DFF446	AUD4LEN	W				*	
DFF448	AUD4VOL	W				*	2x8bit VOL (LEFT/RIGHT)
DFF44A	AUD4CTRL	W				*	16 Control bits 2= Stereo 1= Oneshot 0= (8bit/16bit)
DFF44C	AUD4PER	W				*	16bit PERIOD
DFF450	AUD5L	W				*	Audio channel 5 location (32bit PTR)
DFF452	AUD5L	W				*	
DFF454	AUD5LEN	W				*	Audio channel 5 length (32bit)
DFF456	AUD5LEN	W				*	
DFF458	AUD5VOL	W				*	2x8bit VOL (LEFT/RIGHT)
DFF45A	AUD5CTRL	W				*	16 Control bits 2= Stereo 1= Oneshot 0= (8bit/16bit)
DFF45C	AUD5PER	W				*	16bit PERIOD
DFF460	AUD6L	W				*	Audio channel 6 location (32bit PTR)
DFF462	AUD6L	W				*	
DFF464	AUD6LEN	W				*	Audio channel 6 length (32bit)

DFF466	AUD6LEN	W				*	
DFF468	AUD6VOL	W				*	2x8bit VOL (LEFT/RIGHT)
DFF46A	AUD6CTRL	W				*	16 Control bits 2= Stereo 1= Oneshot 0= (8bit/16bit)
DFF46C	AUD6PER	W				*	16bit PERIOD
DFF470	AUD7L	W				*	Audio channel 7 location (32bit PTR)
DFF472	AUD7L	W				*	
DFF474	AUD7LEN	W				*	Audio channel 7 length (32bit)
DFF476	AUD7LEN	W				*	
DFF478	AUD7VOL	W				*	2x8bit VOL (LEFT/RIGHT)
DFF47A	AUD7CTRL	W				*	16 Control bits 2= Stereo 1= Oneshot 0= (8bit/16bit)
DFF47C	AUD7PER	W				*	16bit PERIOD