امیررضا حسینی ۹۸۲۰۳۶۳

سوال اول:

myReg Project Status (12/03/2021 - 20:39:47)			
Project File:	Q1.xise	**Parser Errors:**	No Errors
Module Name:	myReg	**Implementation State:**	Placed and Routed
Target Device:	xc6slx16-3csg324	**• Errors:**	No Errors
Product Version:	ISE 14.7	**• Warnings:**	No Warnings
Design Goal:	Balanced	**• Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	All Constraints Met
Environment:	System Settings	**• Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	8	18,224	1%	
Number used as Flip Flops	8			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	9	9,112	1%	
Number used as logic	9	9,112	1%	
Number using O6 output only	9			
Number using O5 output only	0			
Number using O5 and O6	0			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number of occupied Slices	3	2,278	1%	
Number of MUXCYs used	0	4,556	0%	
Number of LUT Flip Flop pairs used	9			
Number with an unused Flip Flop	1	9	11%	
Number with an unused LUT	0	9	0%	
Number of fully used LUT-FF pairs	8	9	88%	
Number of unique control sets	1			
Number of slice register sites lost to control set restrictions	0	18,224	0%	
Number of bonded IOBs	23	232	9%	
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	
Number of OLOGIC2/OSERDES2s	0	248	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	3.00			

سوال اول:

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report	
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report	
Timing Constraints:	All Constraints Met			

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Fri Dec 3 20:39:29 2021	0	0	0
Translation Report	Current	Fri Dec 3 20:39:32 2021	0	0	0
Map Report	Current	Fri Dec 3 20:39:38 2021	0	0	6 Infos (6 new)
Place and Route Report	Current	Fri Dec 3 20:39:42 2021	0	0	3 Infos (3 new)
Power Report					
Post-PAR Static Timing Report	Current	Fri Dec 3 20:39:46 2021	0	0	4 Infos (4 new)
Bitgen Report					

طراحی دوم:

m_counter Project Status (12/03/2021 - 20:28:51)			
Project File:	Q2.xise	**Parser Errors:**	No Errors
Module Name:	m_counter	**Implementation State:**	Placed and Routed
Target Device:	xc6slx16-3csg324	**• Errors:**	No Errors
Product Version:	ISE 14.7	**• Warnings:**	10 Warnings (3 new)
Design Goal:	Balanced	**• Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	All Constraints Met
Environment:	System Settings	**• Final Timing Score:**	0 (Timing Report)

Current Errors	[-]
No Errors Found	

Current Warnings	[-]
Synthesis Warnings	**New**
WARNING:HDLCompiler:413: - "C:\Users\amirVM\Desktop\tamrin 3\Q2\Q2\m_counter.v" Line 42: Result of 20-bit expression is truncated to fit in 19-bit target.	
WARNING:HDLCompiler:413: - "C:\Users\amirVM\Desktop\tamrin 3\Q2\Q2\m_counter.v" Line 43: Result of 10-bit expression is truncated to fit in 9-bit target.	
WARNING:HDLCompiler:413: - "C:\Users\amirVM\Desktop\tamrin 3\Q2\Q2\m_counter.v" Line 46: Result of 20-bit expression is truncated to fit in 19-bit target.	
WARNING:HDLCompiler:413: - "C:\Users\amirVM\Desktop\tamrin 3\Q2\Q2\m_counter.v" Line 47: Result of 9-bit expression is truncated to fit in 8-bit target.	
WARNING:HDLCompiler:413: - "C:\Users\amirVM\Desktop\tamrin 3\Q2\Q2\m_counter.v" Line 50: Result of 20-bit expression is truncated to fit in 19-bit target.	
WARNING:HDLCompiler:413: - "C:\Users\amirVM\Desktop\tamrin 3\Q2\Q2\m_counter.v" Line 51: Result of 8-bit expression is truncated to fit in 7-bit target.	
WARNING:HDLCompiler:413: - "C:\Users\amirVM\Desktop\tamrin 3\Q2\Q2\m_counter.v" Line 54: Result of 32-bit expression is truncated to fit in 1-bit target.	
WARNING:Xst:1293: - FF/Latch <counting_0> has a constant value of 0 in block <m_counter>. This FF/Latch will be trimmed during the optimization process.	New
WARNING:Xst:1896: - Due to other FF/Latch trimming, FF/Latch <counting_1> has a constant value of 0 in block <m_counter>. This FF/Latch will be trimmed during the optimization process.	New
WARNING:Xst:1896: - Due to other FF/Latch trimming, FF/Latch <counting_2> has a constant value of 0 in block <m_counter>. This FF/Latch will be trimmed during the optimization process.	New

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	41	18,224	1%	
Number used as Flip Flops	41			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	51	9,112	1%	
Number used as logic	48	9,112	1%	
Number using O6 output only	10			
Number using O5 output only	19			
Number using O5 and O6	19			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number used exclusively as route-thrus	3			
Number with same-slice register load	0			
Number with same-slice carry load	3			
Number with other load	0			
Number of occupied Slices	16	2,278	1%	
Number of MUXCYs used	48	4,556	1%	
Number of LUT Flip Flop pairs used	51			
Number with an unused Flip Flop	12	51	23%	
Number with an unused LUT	0	51	0%	
Number of fully used LUT-FF pairs	39	51	76%	
Number of unique control sets	5			
Number of slice register sites lost to control set restrictions	15	18,224	1%	
Number of bonded IOBs	49	232	21%	
Number of RAMB16BWERs	0	32	0%	

طراحی دوم:

Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	
Number of OLOGIC2/OSERDES2s	0	248	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	2.72			

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report	
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report	
Timing Constraints:	All Constraints Met			

Clock Report	[-]
Data Not Yet Available	

Detailed Reports						[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**	
Synthesis Report	Current	Fri Dec 3 20:28:32 2021	0	10 Warnings (3 new)	1 Info (1 new)	
Translation Report	Current	Fri Dec 3 20:28:35 2021	0	0	0	
Map Report	Current	Fri Dec 3 20:28:41 2021	0	0	6 Infos (6 new)	
Place and Route Report	Current	Fri Dec 3 20:28:46 2021	0	0	3 Infos (3 new)	
Power Report						
Post-PAR Static Timing Report	Current	Fri Dec 3 20:28:50 2021	0	0	4 Infos (4 new)	
Bitgen Report						

Secondary Reports			[-]
Report Name	**Status**	**Generated**	

طراحی سوم:

sequence_detector Project Status (12/07/2021 - 21:33:40)			
Project File:	soal3.xise	**Parser Errors:**	No Errors
Module Name:	sequence_detector	**Implementation State:**	Placed and Routed
Target Device:	xc6slx16-3csg324	**• Errors:**	No Errors
Product Version:	ISE 14.7	**• Warnings:**	2 Warnings (1 new)
Design Goal:	Balanced	**• Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	All Constraints Met
Environment:	System Settings	**• Final Timing Score:**	0 (Timing Report)

Current Warnings	[-]
Synthesis Warnings	**New**
WARNING:HDLCompiler:413: - "C:\Users\amirVM\Desktop\tamrin 3\Q3\soal3\sequence_detector.v" Line 60: Result of 17-bit expression is truncated to fit in 16-bit target.	
Map Warnings	**New**
WARNING:Place:837: - Partially locked IO Bus is found. Following components of the bus are not locked: Comp: dseq_count<0>	New

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	22	18,224	1%	
Number used as Flip Flops	22			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	40	9,112	1%	
Number used as logic	39	9,112	1%	
Number using O6 output only	24			
Number using O5 output only	14			
Number using O5 and O6	1			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number used exclusively as route-thrus	1			
Number with same-slice register load	0			
Number with same-slice carry load	1			
Number with other load	0			
Number of occupied Slices	12	2,278	1%	
Number of MUXCYs used	16	4,556	1%	
Number of LUT Flip Flop pairs used	40			
Number with an unused Flip Flop	18	40	45%	
Number with an unused LUT	0	40	0%	
Number of fully used LUT-FF pairs	22	40	55%	
Number of unique control sets	3			
Number of slice register sites lost to control set restrictions	10	18,224	1%	
Number of bonded IOBs	22	232	9%	
Number of LOCed IOBs	21	22	95%	
Number of unique control sets	3			
Number of slice register sites lost to control set restrictions	10	18,224	1%	
Number of bonded IOBs	22	232	9%	
Number of LOCed IOBs	21	22	95%	
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	
Number of OLOGIC2/OSERDES2s	0	248	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	3.64			

طراحی چهارم:

Binary_Divisibility_By_7 Project Status (12/01/2021 - 11:45:32)			
Project File:	Q4.xise	**Parser Errors:**	No Errors
Module Name:	Binary_Divisibility_By_7	**Implementation State:**	Programming File Generated
Target Device:	xc6slx16-3csg324	**• Errors:**	No Errors
Product Version:	ISE 14.7	**• Warnings:**	2 Warnings (2 new)
Design Goal:	Balanced	**• Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	All Constraints Met
Environment:	System Settings	**• Final Timing Score:**	0 (Timing Report)

Current Errors	[-]
No Errors Found	

Current Warnings	[-]
Synthesis Warnings	**New**
WARNING:HDLCompiler:413: - "C:\Users\amirVM\Desktop\tamrin 3\Q4\Binary_Divisibility_By_7.v" Line 56: Result of 32-bit expression is truncated to fit in 1-bit target.	New
Map Warnings	**New**
WARNING:Place:837: - Partially locked IO Bus is found. Following components of the bus are not locked: Comp: Remainder<0>	New

Current Errors	[-]
No Errors Found	

Current Warnings	[-]
Synthesis Warnings	**New**
WARNING:HDLCompiler:413: - "C:\Users\amirVM\Desktop\tamrin 3\Q4\Binary_Divisibility_By_7.v" Line 56: Result of 32-bit expression is truncated to fit in 1-bit target.	New
Map Warnings	**New**
WARNING:Place:837: - Partially locked IO Bus is found. Following components of the bus are not locked: Comp: Remainder<0>	New

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	3	18,224	1%	
Number used as Flip Flops	3			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	4	9,112	1%	
Number used as logic	4	9,112	1%	
Number using O6 output only	4			
Number using O5 output only	0			
Number using O5 and O6	0			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number of occupied Slices	2	2,278	1%	
Number of MUXCYs used	0	4,556	0%	
Number of LUT Flip Flop pairs used	4			
Number with an unused Flip Flop	1	4	25%	
Number with an unused LUT	0	4	0%	
Number of fully used LUT-FF pairs	3	4	75%	
Number of unique control sets	1			
Number of slice register sites lost to control set restrictions	5	18,224	1%	
Number of bonded IOBs	8	232	3%	
Number of LOCed IOBs	7	8	87%	
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	

طراحی چهارم:

Number of OLOGIC2/OSERDES2s	0	248	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	3.29			

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report	
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report	
Timing Constraints:	All Constraints Met			

Failing Constraints	[-]
All Constraints Were Met	

Clock Report	[-]
Data Not Yet Available	

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Wed Dec 1 11:40:30 2021	0	1 Warning (1 new)	0
Translation Report	Current	Wed Dec 1 11:41:57 2021	0	0	0
Map Report	Current	Wed Dec 1 11:42:03 2021	0	1 Warning (1 new)	7 Infos (7 new)
Place and Route Report	Current	Wed Dec 1 11:42:09 2021	0	0	3 Infos (3 new)
Power Report					
Post-PAR Static Timing Report	Current	Wed Dec 1 11:42:12 2021	0	0	4 Infos (4 new)
Bitgen Report	Current	Wed Dec 1 11:45:29 2021	0	0	0

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
SmartXplorer Report	Current	Fri Dec 3 19:50:23 2021	
WebTalk Report	Current	Wed Dec 1 11:45:29 2021	
WebTalk Log File	Current	Wed Dec 1 11:45:32 2021	