Computational Foundations of Cyber Physical Systems (CS61063)

Tutorial 1
on RISC

Memory Hierarchy Problem - 1

Suppose that a computer has a processor with two L1 caches, one for instructions and one for data, and an L2 cache. Let the access time for the two L1 caches be $C_1=t$. The miss penalties are : approximately $C_2=15t$ for transferring a block from L2 to L1 on miss, and M=100t for transferring a block from the main memory to L2 on miss. Assume that, the hit rates are the same for instructions and data i.e. the hit rates in the L1 cache is $h_1=0.96$ and in L2 cache is $h_2=0.80$.

Memory Hierarchy Problem 1

(a) What fraction of accesses miss in both the L1 and L2 caches, thus requiring access to the main memory?

Soln. With L1 and L2 caches, the average memory access time (AMAT) is

$t_{avg} = h_1C_1+(1-h_1)[h_2C_2+(1-h_2)M]$

The fraction of memory accesses that miss in both the L1 and L2 caches is$(1-h_1)(1-h_2)=(1-0.96)(1-0.80)=0.008$

Memory Hierarchy Problem 1

(b) What is the average access time as seen by the processor?

Soln. The average memory access time using two cache levels =

t_{avg} (actual)= $h_1C_1+(1-h_1)[h_2C_2+(1-h_2)M]$

= 0.96t+0.04(0.80×15t+0.20×100t)=2.24t

(c) Suppose that the L2 cache has an ideal hit rate of 1. By what factor would this reduce the average memory access time as seen by the processor?

Soln. With no misses in the L2 cache, average memory access time

t_{avg} (ideal)= *0.96t+0.04×15t= 1.56t*

Therefore, t_{avg}(actual)/t_{avg}(ideal) = 2.24t/1.56t = 1.44

Memory Hierarchy Problem 1

(d) Consider the following change to the memory hierarchy. The L2 cache is removed and the size of the L1 caches is increased so that their miss rate is cut in half. What is the average memory access time as seen by the processor in this case?

Soln. For single level cache the AMAT is $t_{avg}=h_1C_1+(1-h_1)M$
So, with larger L1 caches and the L2 cache removed, the AMAT is
$t_{avg}= 0.98t + 0.02 \times 100t = 2.98t$

Memory Hierarchy: Problem 2

The memory access time is 1 nsec for a read operation with a hit in cache, 5 nsec for a read operation with a miss in cache, 2 nsec for a write operation with a hit in cache, and 10 nsec for a write operation with a miss in cache. The execution of a sequence of instructions involves 100 instruction fetch operations, 60 memory operand read operations, and 40 memory operand write operations. The cache hit ratio is 0.9. What is the average memory access time (in nanoseconds) in executing the sequence of instructions?

Solve

Memory Hierarchy: Problem 2

The memory access time is 1 nsec for a read operation with a hit in cache, 5 nsec for a read operation with a miss in cache, 2 nsec for a write operation with a hit in cache, and 10 nsec for a write operation with a miss in cache. The execution of a sequence of instructions involves 100 instruction fetch operations, 60 memory operand read operations, and 40 memory operand write operations. The cache hit ratio is 0.9. What is the average memory access time (in nanoseconds) in executing the sequence of instructions?

Number of reads = 100 + 60 = 160
Number of writes = 40
Fraction of reads = 160/200 = 0.8
Fraction of writes = 0.2
Average access time = 0.8*[0.9 + (0.1*5)] + 0.2*[(0.9*2 + (0.1*10))] ns = 1.68 ns

Memory Hierarchy: Problem 3

A cache memory of 1 MB has a block size of 256 bytes. The cache has an access time of 3 ns and a hit rate of 94%. During a cache miss, it takes 20 ns to bring the first word of a block from the main memory, while each subsequent word takes 5 ns. The word size is 64 bits. What is the average memory access time in ns ?

Solve

Memory Hierarchy: Problem 3

A cache memory of 1 MB has a block size of 256 bytes. The cache has an access time of 3 ns and a hit rate of 94%. During a cache miss, it takes a total of 20 ns to look into the cache and bring the first word of a block from the main memory if missed, while each subsequent word takes 5 ns. The word size is 64 bits. What is the average memory access time in ns ?

Word size = 64 bits = 8B; Block size = 256B

No. of words = 256/8 = 32

$T_{avg} = (0.94 \times 3) + (1 - 0.94)\ [20 + (31 \times 5)]$ ns

$= 13.3$ ns

DRAM Refresh Cycle: Problem 1

All dynamic memories have to be refreshed. A typical DRAM takes 64 ms to refresh. Suppose there are 8 K rows and it takes four clock cycles to access each row. If the clock rate is 133 MHz, find the refresh overhead in terms of percentage (upto 2 decimal places).

Total number of cycles required to refresh = 8k * 4 = 2^{15}

Time required to refresh = 2^{15} /(133 * 10^6) s = 0.246 ms

Overhead = (0.246/64) * 100 % = 0.38%