Home Assignment
CSE 231: Digital Logic Design
Spring 2020
Due Date: June 4th, 2020
Total Questions: 4 Total Marks: 85

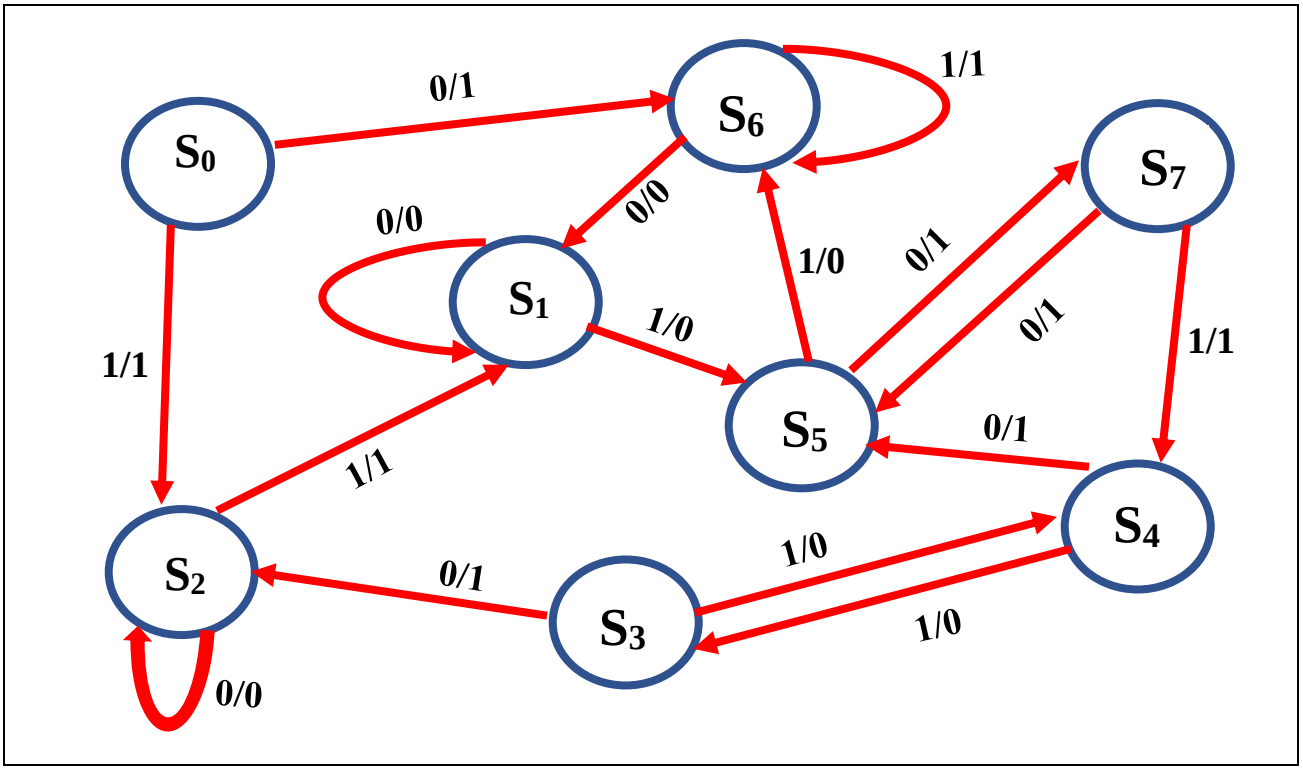
Instructions:

- You are required to submit **handwritten answers to all questions (make a single PDF)**.
- **Answer the questions in a numerical order** (Ques 1 first, then Ques 2, and so on)**.**
- You **must show all necessary steps** that are required to answer a specific question.
- Any sorts of plagiarism, or unauthorized assistance will be considered as a serious act of violation of academic conduct and will be dealt accordingly (e.g. marks deduction).
- You **must mention your Name and ID** on top of every page of your answer script.

[Q1] (a) Discuss the differences between combinational and sequential logic circuits. Provide an example to explain your answer. **[5]**

(b) Discuss the differences between latches and flip-flops with an example. **[5]**

[Q2] A state diagram is given in **Fig. 1**. You are required to design the sequential circuit that implements the given state diagram **using (a) T-flipflops, and (b) JK-flipflops (i.e. two different circuits)**. **Explain which one of these designed circuits is preferable for implementation and why.** [You must show all required steps for your answer] **[15+15+5]**



[Q3] (a) Design a **positive-edge triggered MOD-9 asynchronous counter**. For your answer, you are required to **show the circuit diagram, the state diagram, and the timing diagram** for a whole cycle of the MOD-9 counter. **You need to explain your design/steps to justify your answer.** **[10]**

(b) Is it possible to design a **synchronous counter** to show similar operation as the **MOD-9 asynchronous counter** mentioned in part (a)? If yes, then **show the state diagram and state table** for the **synchronous counter for this specific problem and explain how it works.** **[10]**

[Q4] (a) Design (show the diagram of) a **8 × 6 RAM**. **Briefly discuss** what you understand by the term **8 × 6** here and **state why your** drawn diagram represents a **8 × 6 RAM.** **[10]**

(b) Design a digital circuit that includes a **single ROM (use basic components to draw ROM circuit, do not use block diagram directly) and a seven-segment display** to show a combination of letters and digits. The circuits should **show the first letters of your first and last names, and 6 digits of your Student ID starting from the 3rd position of the ID**. **For example,** a student (**name: Shahriar Athar, ID: 1932130615**) will make a circuit that that shows the sequence: **SA321306**. You can use small/capital letters if you require. Moreover, if you cannot show the first letter of your name on a seven-segment display select the next letter in order. **For example**, if your name is **Rishad Zahir**, then you may show '**rA'** as a part of your combination. **[10]**

--*-*-*-* **Best of Luck** *-*-*-*-*-*