North South University

Department of Electrical & Computer Engineering

Project

Final Report

Course Title: CSE231

Course Instructor: Faculty Name: **Fahimul Haque (FHE)**

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Section: 05

Group Number: 08

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Project : CSE 231

Objective :

Switching on the circuit through **ON/OFF Switch** results in the string of characters being displayed on the seven-segment display one character at a time at a set time interval of 2-3 seconds. At the end of the sequence, the string is repeated.

The sequential logic circuit produces a sequence of codes to represent the string of characters ‘’**CSE231-8’’ .**

Apparatus :

- BreadBoard
- Jumping wire
- 7 segment LED display
- 9v connection with switch
- 5v converter 7805-IC
- NE555 Pulse Frequency Duty Cycle Adjustable Module Timer
- T Filp Flop -3 units (using J k Flip Flop by attaching J & K) – 7476 IC 2units
- 2 Input And Gate || 7408 IC – 4 units
- 3 Input Or gate || 4075 IC – 2 units
- Not Gate || 7404 IC – 1 unit

Wire Marking :

- Green wire – A
- Blue wire – B
- Silver wire – C
- Orange wire – A’
- Pink wire – B’
- White wire – C’
- Brown wire - Preset
- Blue wire – Clock
- White wire – Input of Flip Flops

- Orange wire – Clear
- Pink wire - Output of Flip Flops (Q0)
- Yellow wire – JK short
- Red wire – VCC connection
- Black wire – GND connection

Combinational Part

Truth Table

CSE231-8

Minterm	A	B	C	a	b	c	d	e	f	g	Letter
0	0	0	0	1	0	0	1	1	1	0	C
1	0	0	1	1	0	1	1	0	1	1	S
2	0	1	0	1	0	0	1	1	1	1	E
3	0	1	1	1	1	0	1	1	0	1	2
4	1	0	0	1	1	1	1	0	0	1	3
5	1	0	1	0	1	1	0	0	0	0	1
6	1	1	0	0	0	0	0	0	0	1	-
7	1	1	1	1	1	1	1	1	1	1	8

By using the truth table we find out the equations with the help of K Map .

1.Using Basic Gates :

Algebric Expressions :

K map for **a**

1	1	1	1
1		1	

a = A’ + B’C’ + BC

K map for **b**

		1	
1	1	1	

b = AB’ + BC

K map for **c**

	1		
1	1	1	

c = AB’ + AC + B’C

K map for **d**

1	1	1	1
1		1	

d = A’ + B’C’ + BC

K map for **e**

1		1	1
		1	

e = A’C’ + BC

K map for **f**

1	1		1
		1	

f = A’B’ + A’C’ + ABC

K map for **g**

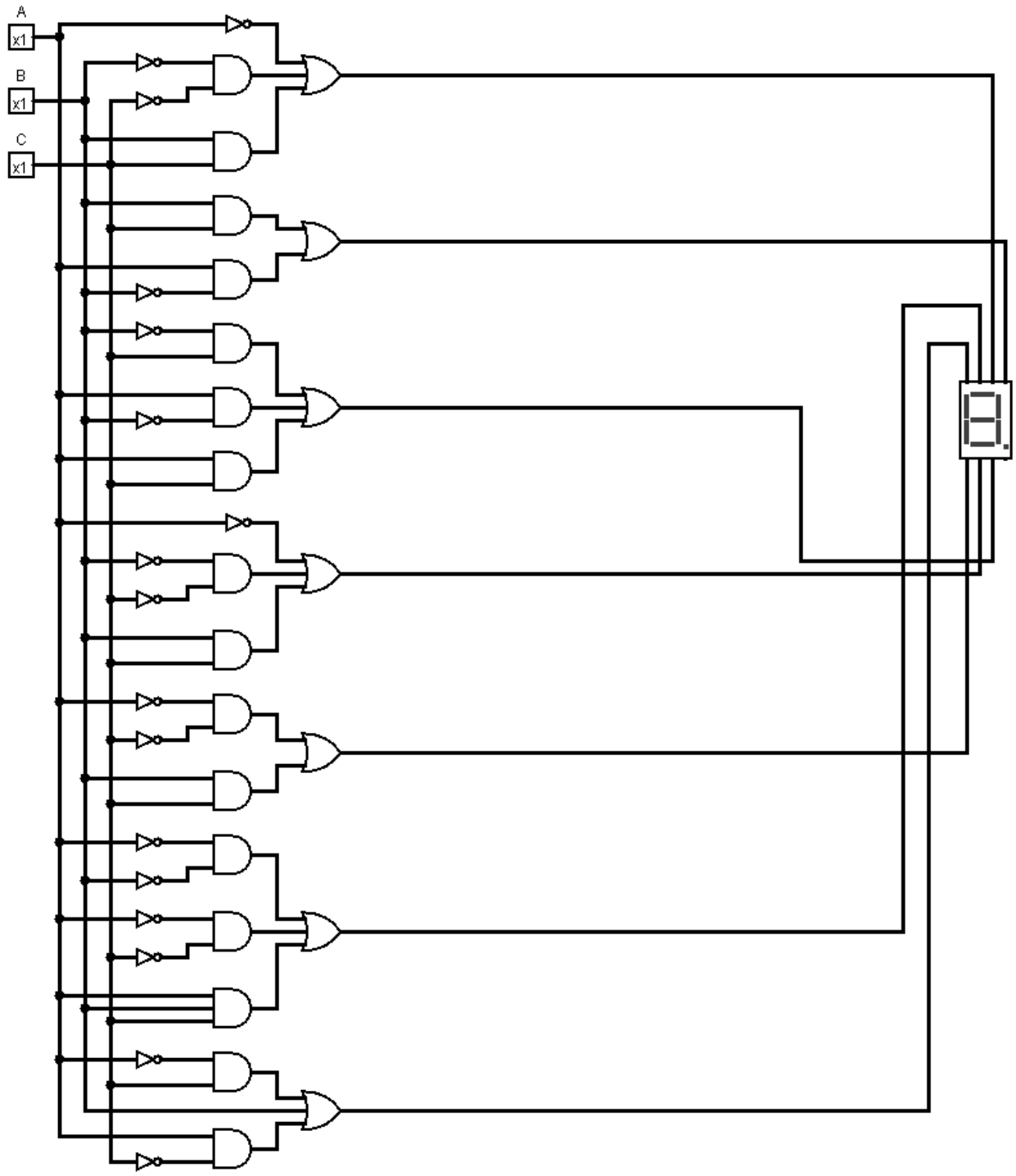
	1	1	1
1		1	1

g = A’C + AC’ + B

By using the equations we have build the combinational part of the circuit .

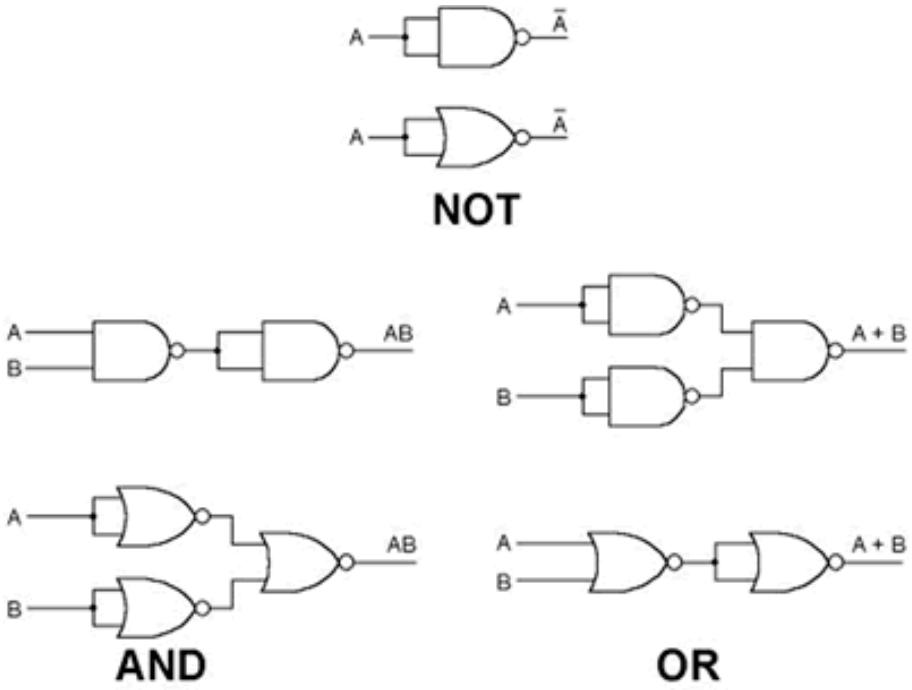
Here is the Logisim of the combinational part of the circuit by using **Basic Gates.**

Using Basic Gates [CSE231-8]



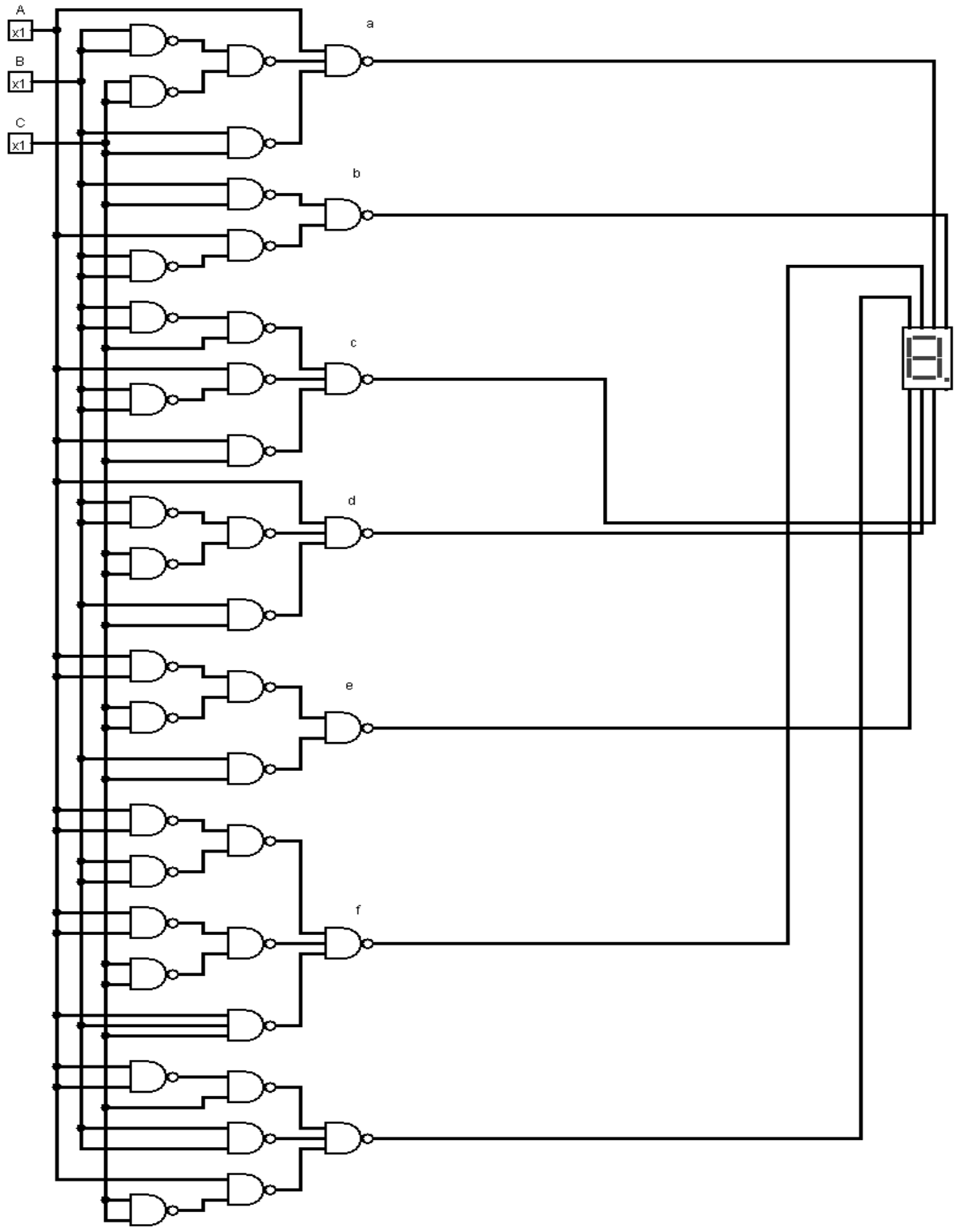
2. Using Nand Gates :

By replacing the basics gates with equivalent nand or nor gates we can implement the same circuit.



We have used nand gates to make the circuits Logisim.

Using Nand Gates



3 . Using 4*1 Multiplexer

Truth Table :

Minterm	A	B	C	a	b	c	d	e	f	g	Letter
0	0	0	0	1	0	0	1	1	1	0	C
1	0	0	1	1	0	1	1	0	1	1	S
2	0	1	0	1	0	0	1	1	1	1	E
3	0	1	1	1	1	0	1	1	0	1	2
4	1	0	0	1	1	1	1	0	0	1	3
5	1	0	1	0	1	1	0	0	0	0	1
6	1	1	0	0	0	0	0	0	0	1	-
7	1	1	1	1	1	1	1	1	1	1	8

C	a
0	1
1	1
0	1
1	1
0	1
1	0
0	0
1	1

C	b
0	0
1	0
0	0
1	1
0	1
1	1
0	0
1	1

C	c
0	0
1	1
0	0
1	0
0	1
1	1
0	0
1	1

C	d
0	1
1	1
0	1
1	1
0	1
1	0
0	0
1	1

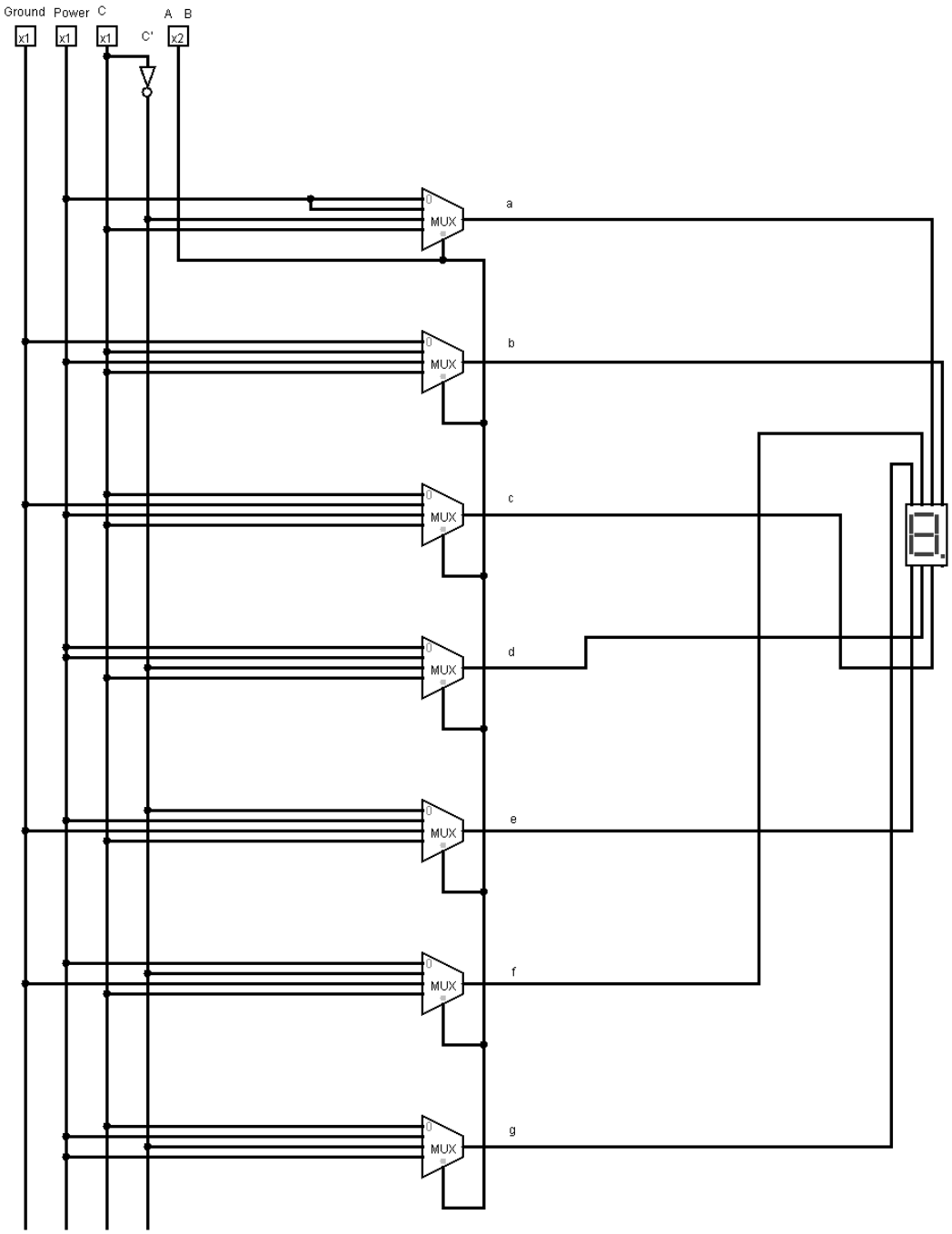
C	e
0	1
1	0
0	1
1	1
0	0
1	0
0	0
1	1

C	f
0	1
1	1
0	1
1	0
0	0
1	0
0	0
1	1

C	g
0	0
1	1
0	1
1	1
0	1
1	0
0	1
1	1

By using 4 * 1 MUX the circuit can be build . Using C , C’ , 1 , 0 as the data input and A,B as the selection input. It needs 7 MUXes to build the circuit .

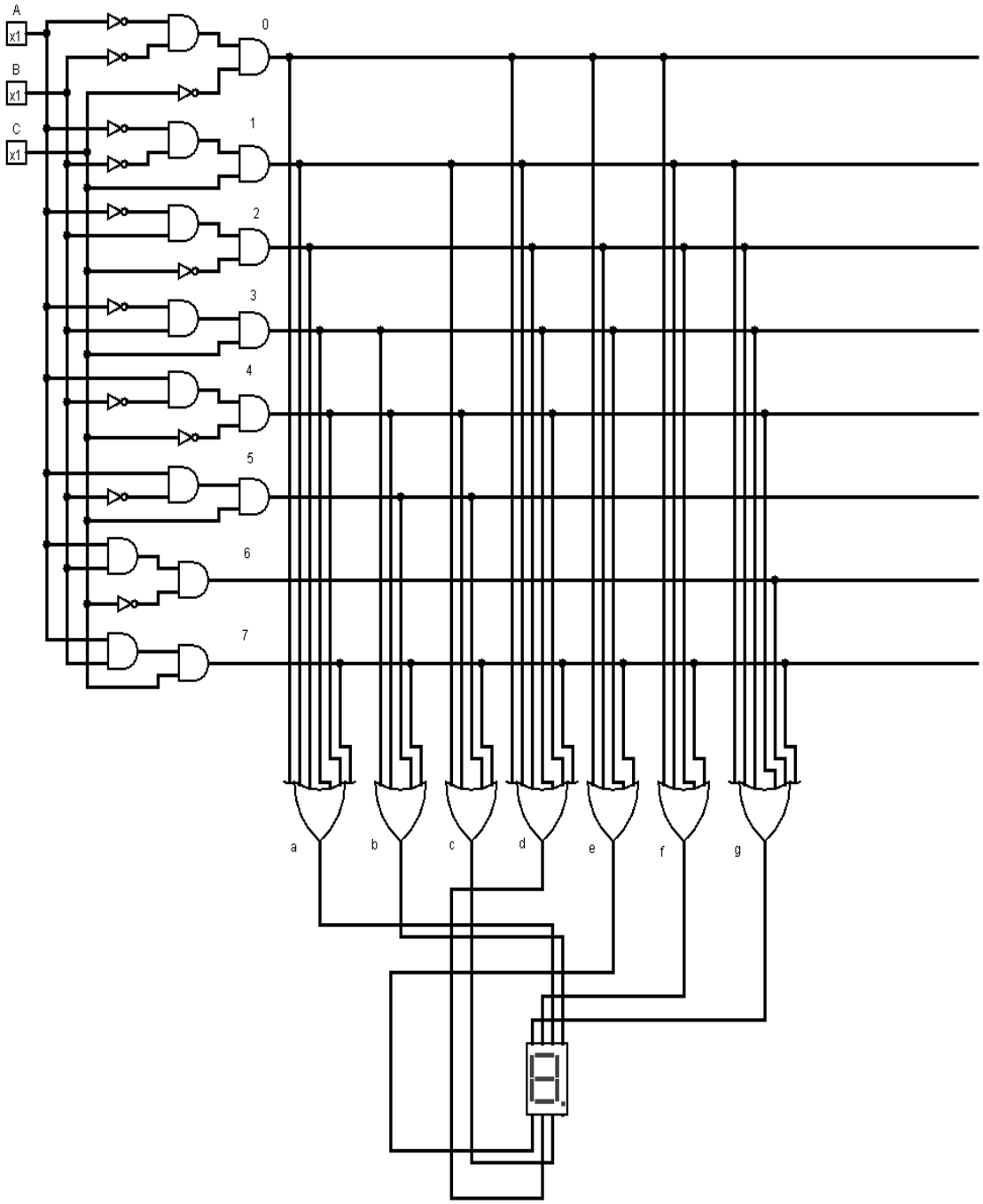
Logisim (Multiplexer 4*1)



4. Using Decoder :

We can use a 3*8 Decoder to make the circuit. The inputs will be A,B,C . The Outputs will be min term for a, b, c, d, e, f, g .

Using Decoder

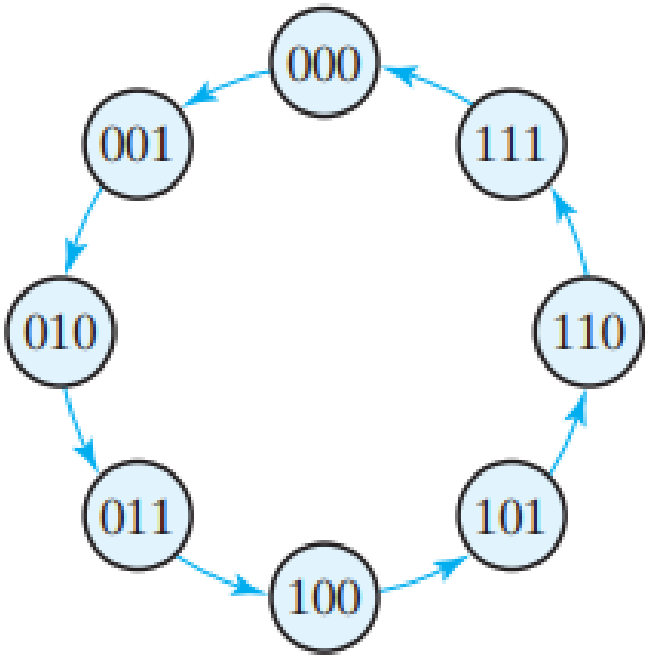


Sequential Part

Process :

By shorting JK FF IC's J & K we make a T FF . .

State diagram of 3-bit binary counter



T FF Excitation Table

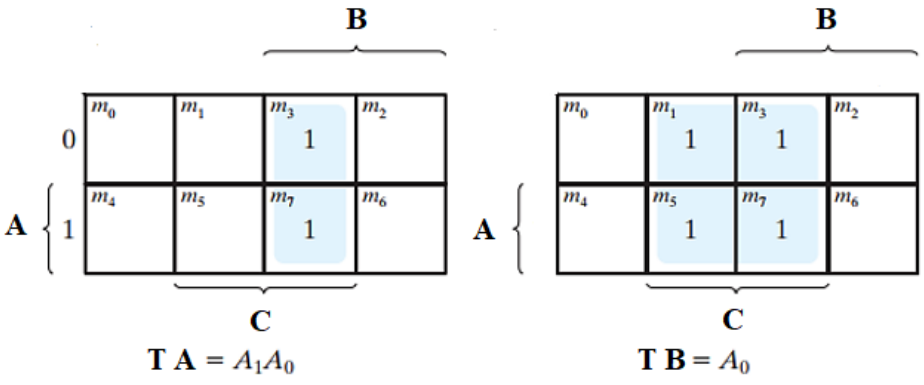
Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

T Flip-flop

T FF State Table

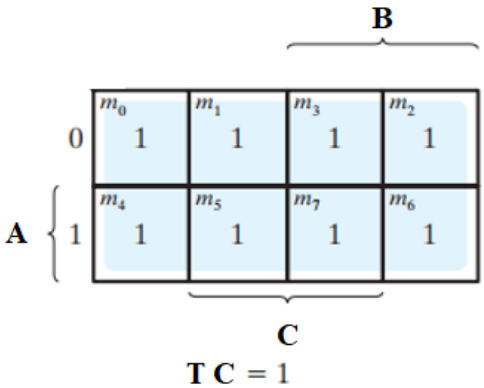
Present State			Next State			Flip-Flop Inputs		
A	B	C	A	B	C	TA	TB	Tc
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	1	1
1	1	1	0	0	0	1	1	1

T FF Input K map



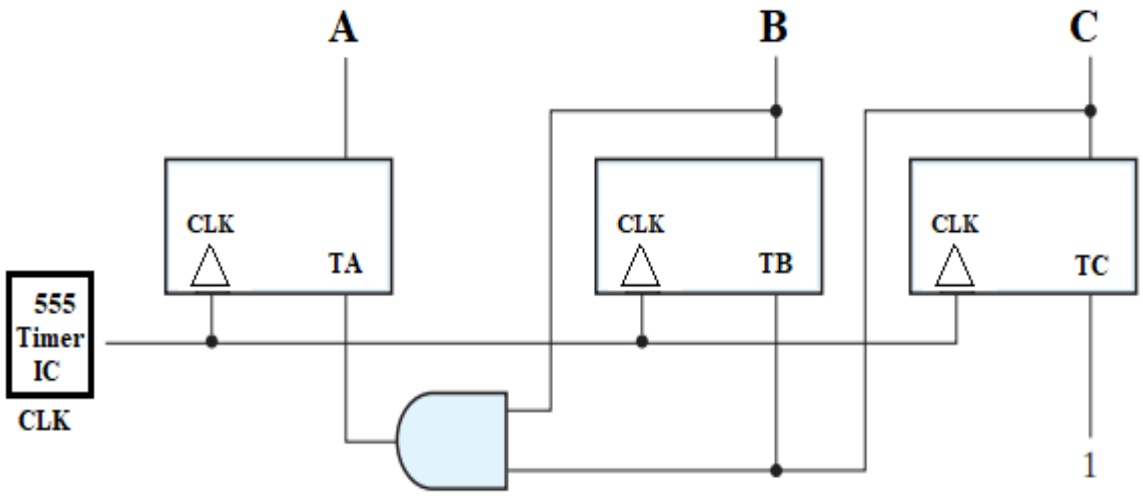
T A = A_1A_0

T B = A_0



T C = 1

Logic diagram of three-bit binary counter using *T* flip-flop



After Building the T Flip Flop circuit then we connected the out put of T F's A,B,C with the combinational part's A,B,C.

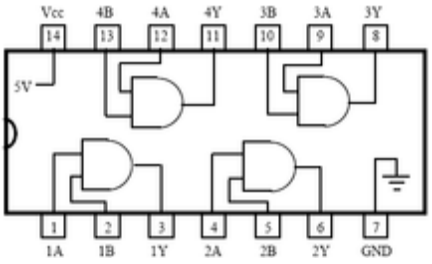
Explanation :

Combinational Part

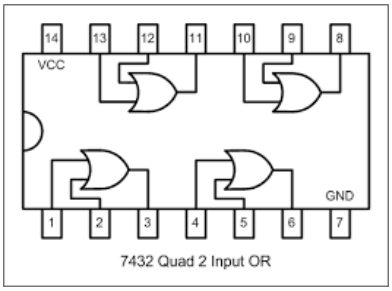
We have used 3 two input And gate ICs,1 Not Gate IC , 2 three input OR Gate ICs and 1 two input OR Gate IC to make the combinational part .

Here are the Pin Diagrams of the ICS

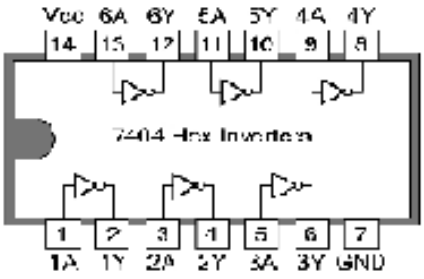
7408 AND GATE



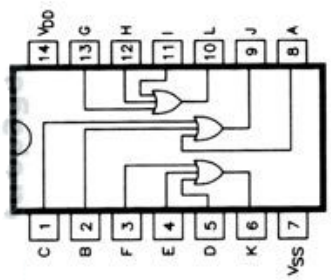
7432 OR GATE



7404 INVERTER

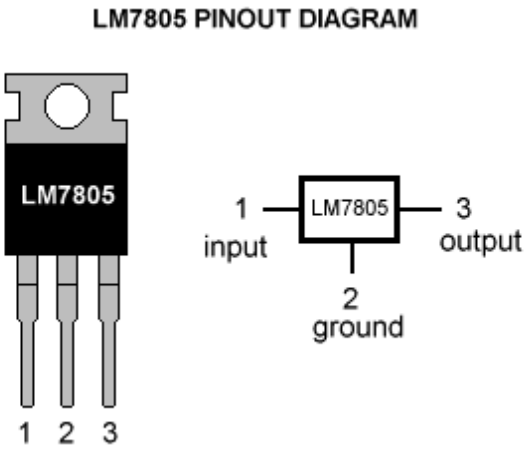


4075 3 INPUT OR

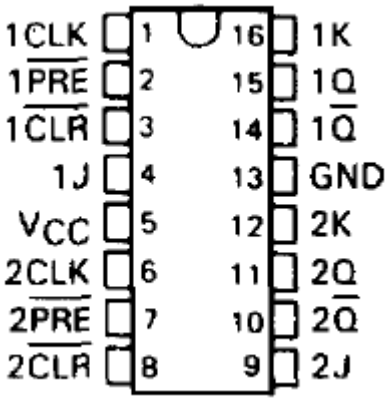


Sequential Part

We have used a 7805 Ic to convert the 9v supply into 5 volt .



We have used 2 JK FF IC 7476 . Then we short the J & K to make it a T FF .



The End