

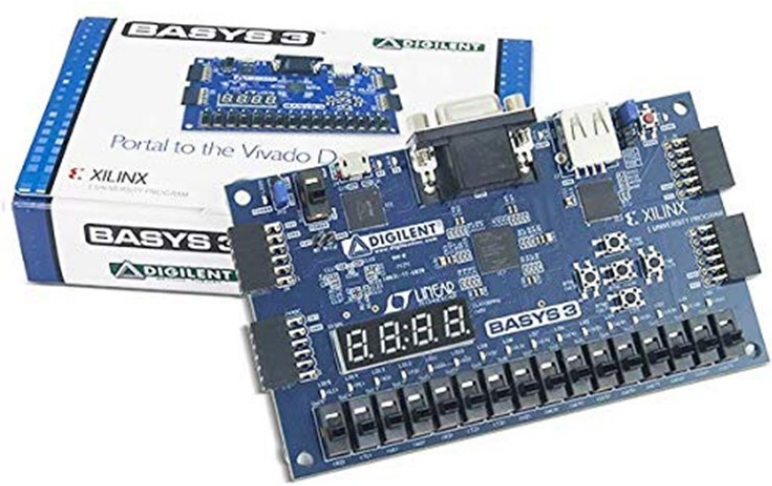
# NES Handheld Emulation Breakout Board for the BASYS-3

Brooks Corbett, Samuel Keadu, Amilcar Paniagua, Joshua Riggs, Anthony Tang  
Faculty Supervisor: Dr. Jens-Peter Kaps

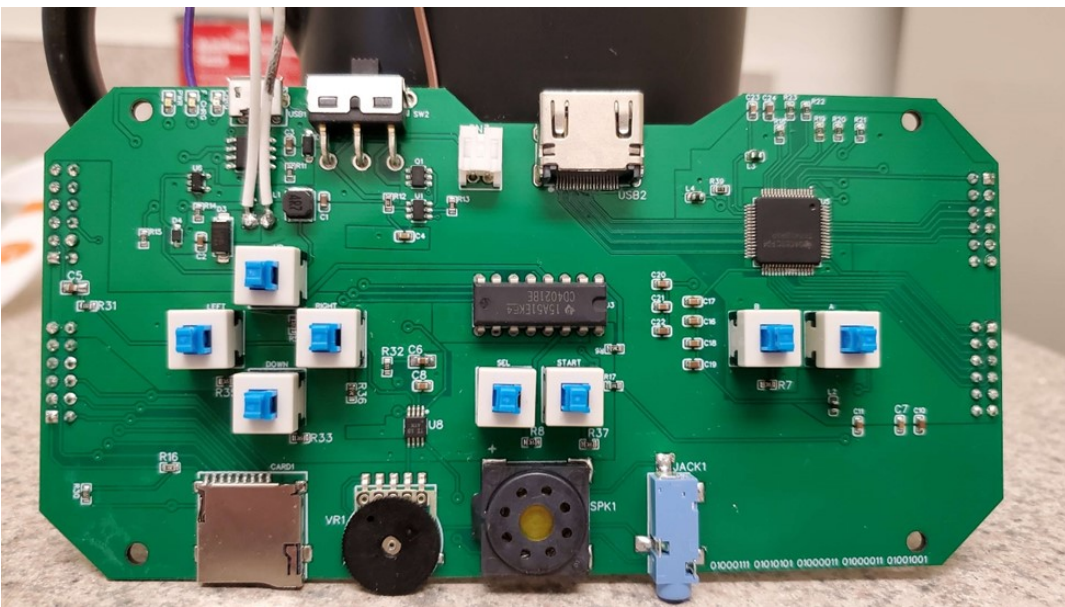
## Abstract

There are several methods to emulate the NES, including software or hardware emulation, with the latter being a more authentic emulation. We emulated the Nintendo Entertainment System (NES) on a BASYS-3 Artix-7 FPGA and minimized overall cost of components needed to create a portable/handheld device. Our NES FPGA emulation device will be comparable to existing devices in terms of price and capabilities. We used existing functionalities of power systems and of P-MOD accessories for the BASYS-3 to create a singular breakout PCB to interface with the BASYS-3. Additionally, this project is designed to be open source to allow future expansion of capabilities and to provide an opportunity to learn about retro console emulation.

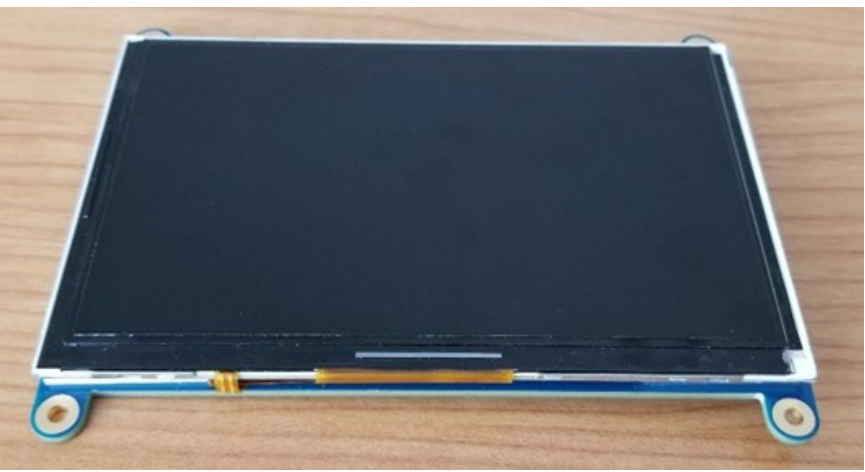
## Hardware



Our project revolves around the use of the BASYS-3, an FPGA prototyping board that all CEC Students have at GMU. The BASYS-3 holds the NES CPU architecture and will handle all input and output signals.



The PCB was designed in EasyEDA software and manufactured by JLCPCB. We designed the PCB contains all necessary circuits needed for controller, power management/charging, audio, SD card memory, and display output. To interface on top of the BASYS-3, we integrated PMOD headers on bottom of the PCB.



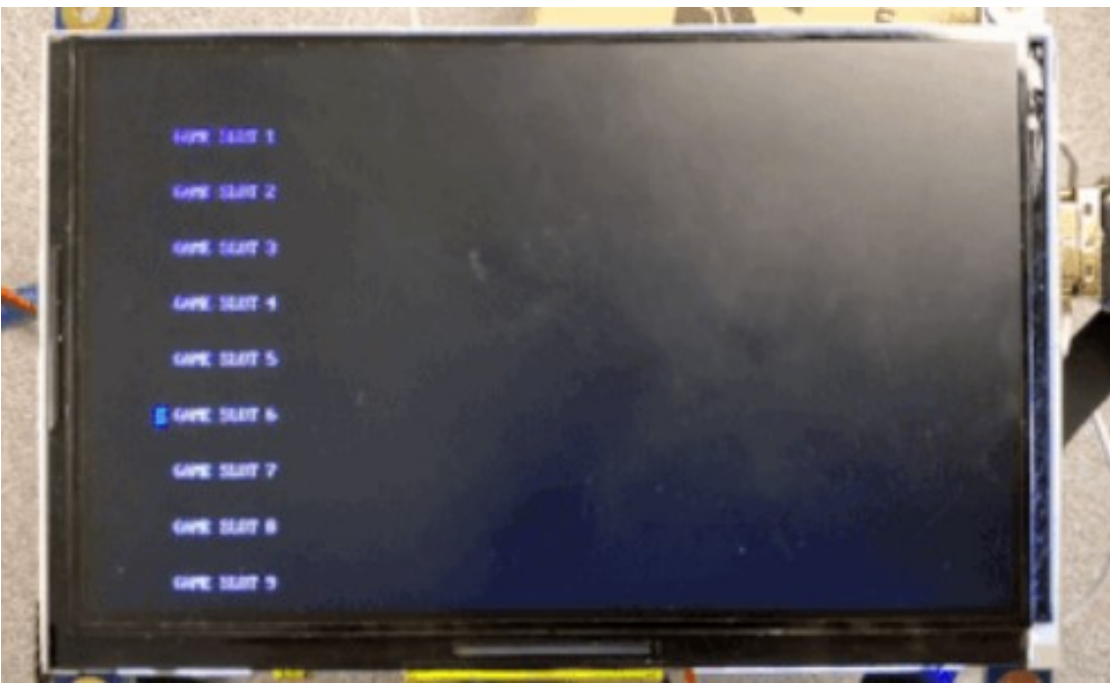
We chose to have an HDMI 5" display backpack. The NES architecture outputs VGA signal, therefore in the display circuit on the PCB, the VGA signal is converted to HDMI by a TFP410PAP IC.

We used a 3.7V 4000mAh li-poly rechargeable battery to power our project. Within the PCB circuit, the battery power is boosted to 5V in order to power the BASYS-3.

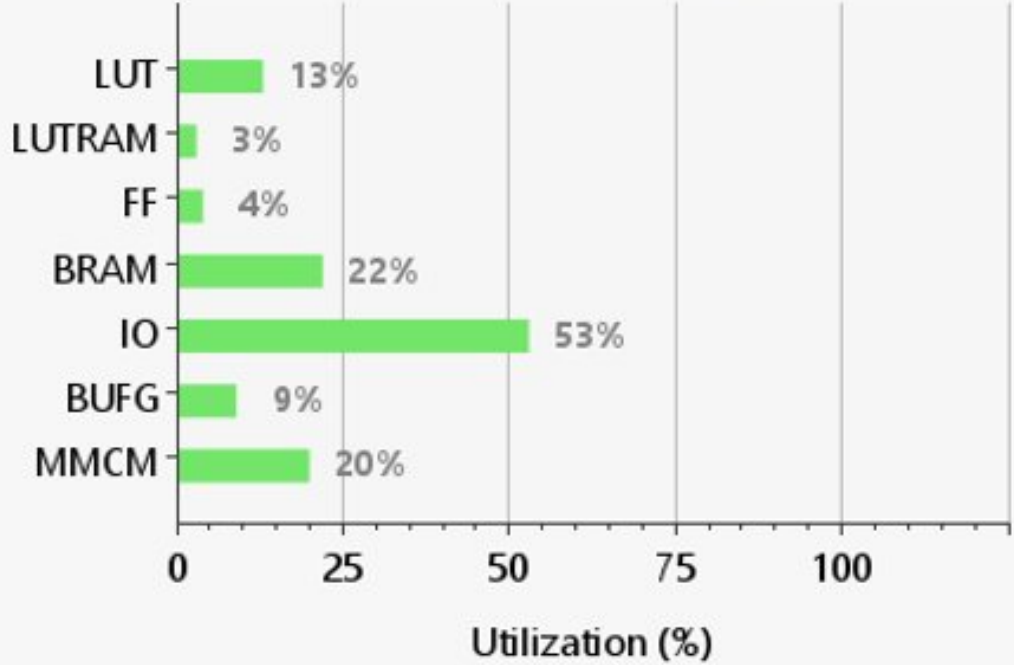


## Software

We based our NES FPGA project on the open-source Verilog implementation of the NES processor written by Brian Bennett on GitHub [1]. Since his implementation was for the Nexys-6 with a Spartan 6 FPGA, we had to learn Verilog and modify the constraints to adapt to the I/O of the BASYS-3. We also created our own Verilog code to interface with an SD card and to select stored games via a start menu.



## Resource Utilization

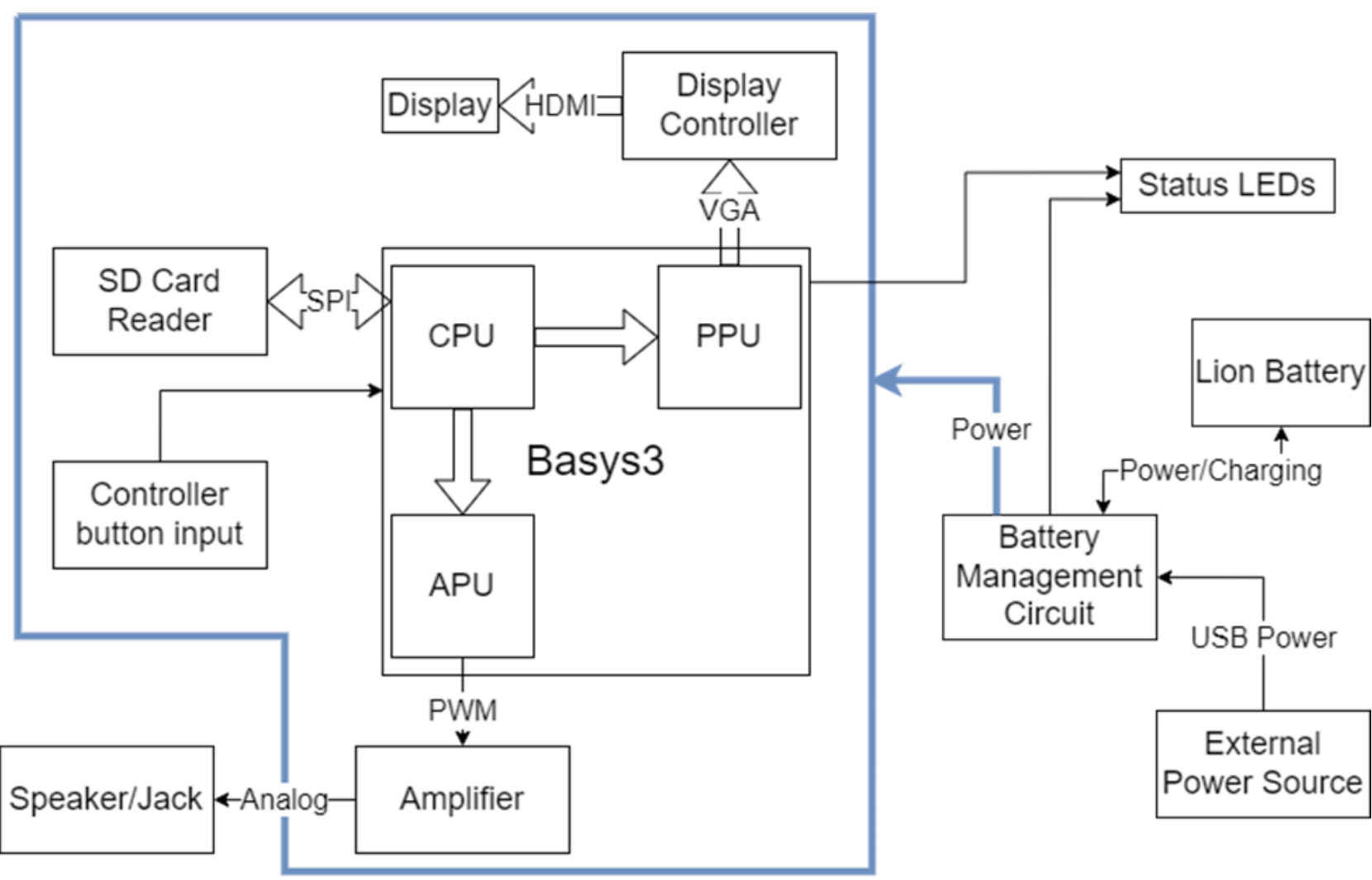


Resource	Utilization	Available	Utilization...
LUT	2601	20800	12.50
LUTRAM	240	9600	2.50
FF	1567	41600	3.77
BRAM	11	50	22.00
IO	56	106	52.83
BUFG	3	32	9.38
MMCM	1	5	20.00

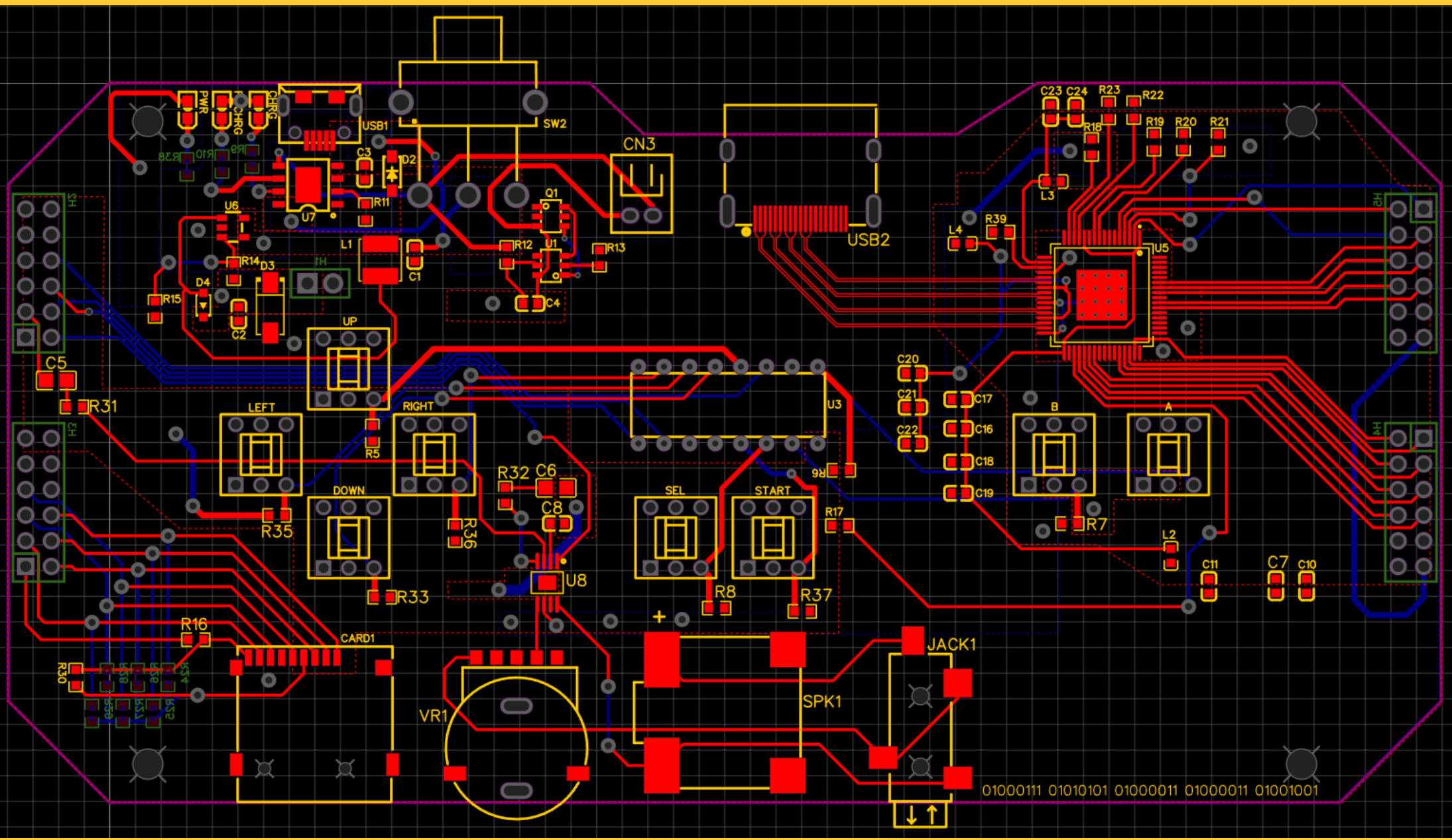
## Testing Results

After playtesting, we were able to achieve parity with original console experience. Our device had an average button response time of 86.32 ms, nearly 10 ms faster than the original NES. We confirmed that audio and video were synchronized and our battery life lasted around 3 hr. Overall, the device we developed will serve as a good platform for expanding FPGA emulations of additional retro consoles.

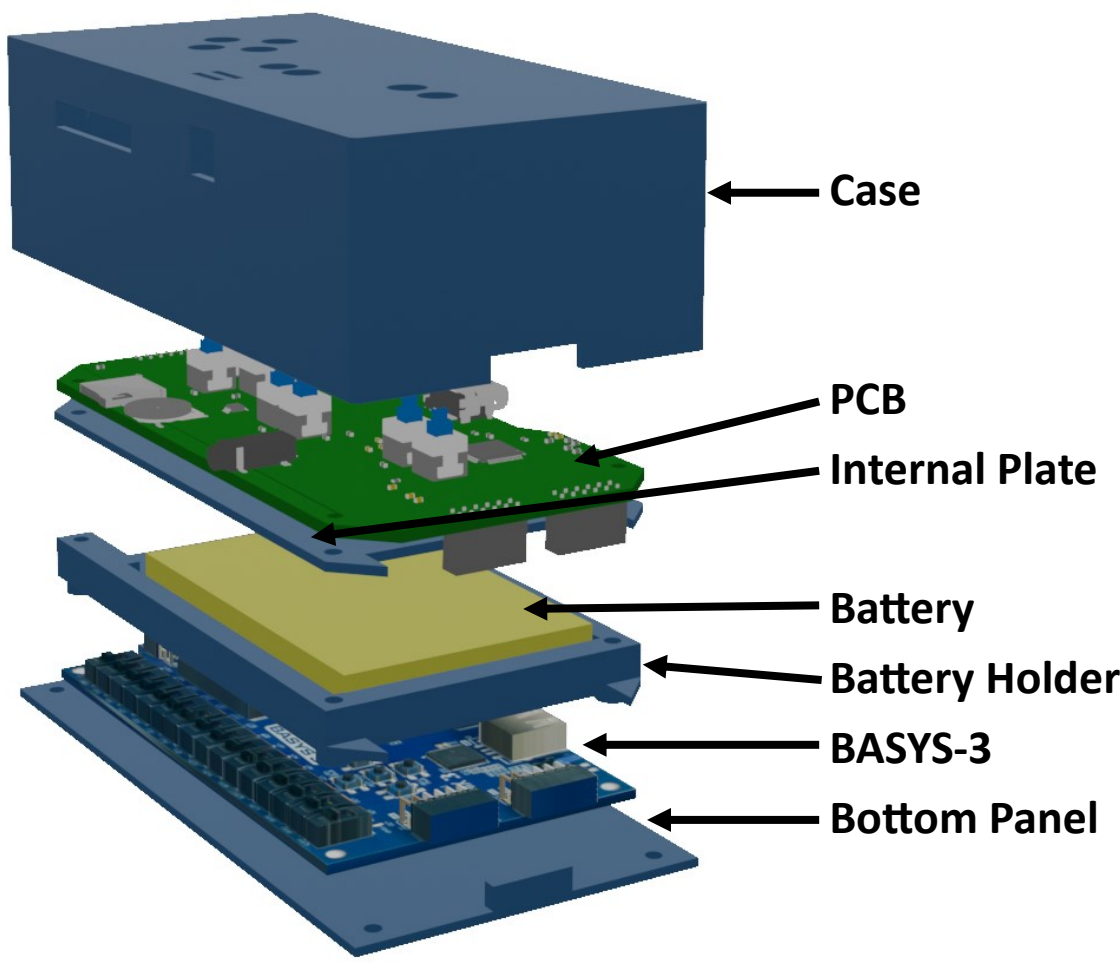
## System Architecture



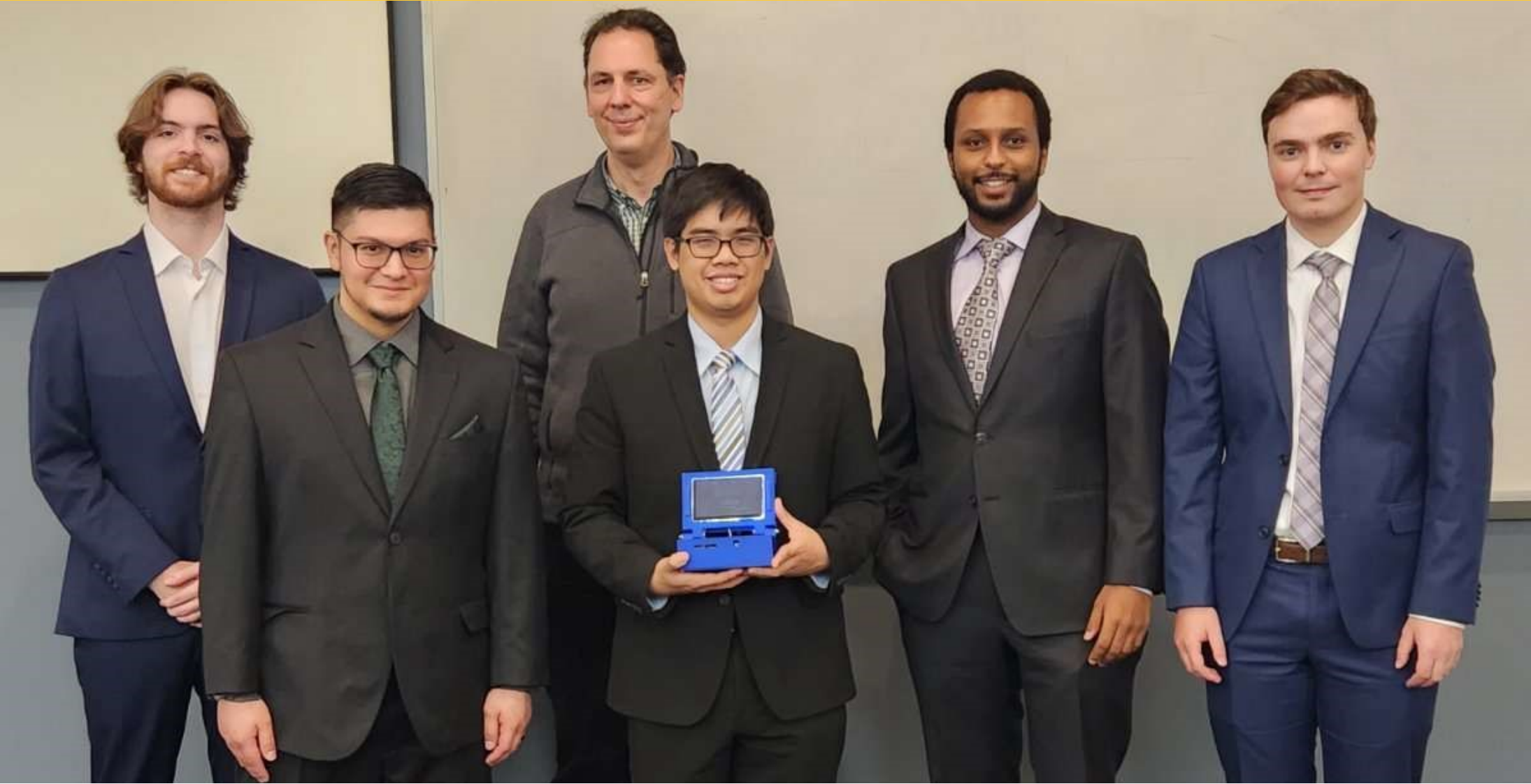
## PCB Layout



## Final Design



## Team Members



From left to right:

Brooks Corbett, Amilcar Paniagua, Dr. Jens-Peter Kaps (FS), Anthony Tang, Samuel Keadu (PM), Joshua Riggs

[1] B. Bennett, "FPGA-based Nintendo Entertainment System Emulator," 14 July 2012. [Online]. Available: [https://github.com/brianbennett/fpga\\_nes](https://github.com/brianbennett/fpga_nes). [Accessed 2022].