Electrical and Computer Engineering
McGill University

ECSE 222 - Digital Logic

Winter 2022

1 General Information

Instructor and Teaching Assistants

Instructor - Prof. Boris Vaisband

- Email: boris.vaisband@mcgill.ca
- Office: McConnell Engineering Building, Room 547
- Office hours: Wednesday, 3:00pm - 4:00pm. Note that office hours are subject to change, in which case the class will be notified in advance.

Teaching assistants

- Tutorial TA: Mr. Amir Ardakani (amir.ardakani@mail.mcgill.ca)
- Tutorial TA: Mr. Maninder Bir Singh Gulshan (maninder.gulshan@mail.mcgill.ca)
- Lab TA: Mr. Yousef Safari (yousef.safari@mail.mcgill.ca)
- Lab TA: Mr. Muhammad Bilal Babar (muhammad.babar@mail.mcgill.ca)

Tomlinson Engagement Award for Mentoring (TEAM) program

- Mr. Abe Arafat (abdullah.arafat@mail.mcgill.ca)
- Mr. Wassim Jabbour (wassim.jabbour@mail.mcgill.ca)
- Ms. Sehr Moosabhoy (sehr.moosabhoy@mail.mcgill.ca)
- Mr. Ryan Reszetnik (ryan.reszetnik@mail.mcgill.ca)

Course Website

All course-related communication, resources, and Q&A will be hosted on myCourses. Please note that all communication and resources will be posted ONLY on myCourses (accessible through the myMcgill web portal or at mycourses2.mcgill.ca/) and will be considered delivered to all students. Please avoid sending the instructor and/or TAs course-material questions over email, but rather post your questions in the relevant forums/topics within the discussion board. Students are encouraged to actively participate in the online discussions as well as answer their classmates' questions.

Lectures, Tutorials, and Labs

Lectures

Monday, Wednesday, and Friday 9:35am - 10:25am in the Adams Building Auditorium.

- No lectures on Monday, February 28, 2022, Wednesday, March 2, 2022, and Friday, March 4, 2022 due to winter reading brake.

Tutorials and labs

Section	Day	Tutorials		Labs	
		Time	Location	Time	Location
002	Monday	1:35pm - 2:25pm	ENGTR 0060	2:35pm - 3:25pm	ENGTR 4060
003	Tuesday	1:35pm - 2:25pm	ENGTR 0060	2:35pm - 3:25pm	ENGTR 4060
004	Wednesday	1:35pm - 2:25pm	ENGTR 2120	2:35pm - 3:25pm	ENGTR 4060
005	Thursday	1:35pm - 2:25pm	ENGTR 0060	2:35pm - 3:25pm	ENGTR 4060
006	Friday	1:35pm - 2:25pm	ENGTR 0060	2:35pm - 3:25pm	ENGTR 4060
007	Tuesday	3:35pm - 4:25pm	ENGTR 0060	4:35pm - 5:25pm	ENGTR 4060
008	Wednesday	3:35pm - 4:25pm	ENGTR 0060	4:35pm - 5:25pm	ENGTR 4060
009	Thursday	3:35pm - 4:25pm	ENGTR 0060	4:35pm - 5:25pm	ENGTR 4060

- Tutorials and labs will begin on Monday, January 10, 2022
- Total of twelve tutorials/labs for each section
- No tutorials/labs during the week of February 28, 2022 due to winter reading brake.

2 Course Description and Pre-Requisites

Description

An introduction to digital logic, binary numbers and Boolean algebra, combinational circuits, optimized implementation of combinational circuits, arithmetic circuits, combinational circuit building blocks, flip-flops, registers, counters, design of digital circuits with VHDL, synchronous sequential circuits, and finite state machines.

Pre-requisite

ECSE 202 – Introduction to Software Development

Graduate Attributes

Knowledge base (KB); Design (DE); Use of engineering tools (ET); Individual and teamwork (IT)

Learning Outcomes

Upon successful completion of this course, a student should:

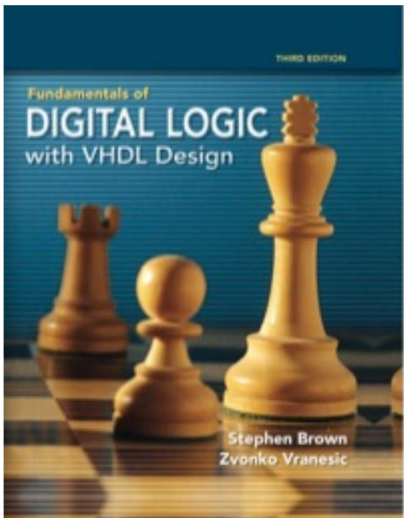
- Show an in-depth understanding of key ideas and concepts related to the design of digital circuits (KB)
- Demonstrate an ability to use relevant digital circuit design, synthesis, and simulation tools (ET)
- Be able to develop a process to design a digital system with the desired specifications (DE)
- Collaborate with other team members and jointly design a complex digital system (IT)

3 List of Topics

- Boolean logic
- Variables and functions
- Boolean algebra
- Logic gates
- Number representations
- Binary numbers
- Signed binary numbers: 1's complement, 2's complement, and sign-magnitude representations
- Introduction to VHDL
- Combinational circuits
- Two-level circuits: sum-of-products and product-of-sums
- NAND and NOR logic networks
- Optimized implementation: Karnaugh maps
- Multilevel synthesis
- Combinational circuits building blocks
- Arithmetic circuits: adders and multipliers
- Multiplexers, encoders, and decoders
- Sequential circuits
- Latches and Flip-Flops
- Registers and counters
- Synchronous sequential circuits
- Finite state machines: design and optimization

4 Course Material

Course Textbook – Brown and Vranesic, Fundamentals of Digital Logic with VHDL Design, Third Edition, McGraw-Hill, 2009.



5 Course Evaluation

McGill University values academic integrity. All students must, therefore, understand the meaning and consequences of cheating, plagiarism, and other academic offenses under the Code of Student Conduct and Disciplinary Procedures (more information: www.mcgill.ca/students/srr/honest/).

In accord with the McGill University Charter of Students Rights, students have the right to submit any written work (that is to be graded), in either English or French.

Grading Scheme

Component	Percentage
Pen-and-paper assignments	10%
VHDL assignments	20%
Midterm exam 1	15%
Midterm exam 2	15%
Final exam	40%

Pen-and-Paper (PP) Assignments

- There will be 12 PP assignments, to be posted on myCourses along with due dates and other relevant information.
- Two lowest-grade PP assignments will not be considered towards the relevant portion of the final grade. All of the other PP assignments will carry the same weight (1%).
- All PP assignments **must** be completed in groups of two students. Students are strongly encouraged (and expected) to attempt, at first, the assignment problems individually. In special cases and only with approval of instructor, a team of three students may be formed.
- Solutions will be posted on the course web page after the due date of each assignment.

Tentative PP assignment schedule

The instructor reserves the right to change the schedule and number of assignments depending on how the course progresses.

PP assignment	Post date	Due date
1	January 7, 2022	January 14, 2022
2	January 14, 2022	January 21, 2022
3	January 21, 2022	January 28, 2022
4	January 28, 2022	February 4, 2022
5	February 4, 2022	February 11, 2022
6	February 11, 2022	February 18, 2022
7	February 18, 2022	February 25, 2022
8	February 25, 2022	March 11, 2022
9	March 11, 2022	March 18, 2022
10	March 18, 2022	March 25, 2022
11	March 25, 2022	April 1, 2022
12	April 1, 2022	April 8, 2022

VHDL Assignments

- There will be 6 VHDL assignments, to be posted on myCourses along with due dates and other relevant information.
- All VHDL assignments will be considered towards the relevant portion of the final grade.

- All VHDL assignments **must** be completed in groups of two students. Students are strongly encouraged (and expected) to attempt, at first, the assignment problems individually. In special cases and only with approval of instructor, a team of three students may be formed.
- The last VHDL assignment (#6) will include, in addition to the regular deliverables (design/simulation/report), a demo component where students will answer questions about the assignment during their respective lab sessions in the last week of the labs, *i.e.*, from April 4, 2022 to April 8, 2022.

VHDL assignments grade percentage and tentative schedule

The instructor reserves the right to change the schedule and number of assignments depending on how the course progresses.

VHDL assignment	Post date	Due date	Percentage
1	January 7, 2022	January 14, 2022	3%
2	January 14, 2022	January 28, 2022	3%
3	January 28, 2022	February 11, 2022	3%
4	February 11, 2022	February 25, 2022	3%
5	February 25, 2022	March 18, 2022	3%
6 (demo)	March 18, 2022	April 8, 2022	5%

Exams

Midterm exams

Two in-class midterms will take place during the semester according to the following tentative schedule.

Midterm	Date	Location
1	February 18, 2022	Adams Building Auditorium
2	March 25, 2022	Adams Building Auditorium

Final exam

The final exam will take place according to the general exam schedule to be posted by the university.

Additional Policies

- In the event of extraordinary circumstances beyond the University's control, the content and/or evaluation scheme in this course is subject to change.
- All assignments are to be submitted online through myCourses by 11:59pm on the due date, unless otherwise stated on the assignment. Note that you can upload as many times as you want before the deadline. Only the last upload will be kept by the system. Submission is required by only one member of the team.
- Late submission of PP assignments will only be accepted within the first 24 hours after the deadline. Penalty for late submission of PP assignments: 40% of the mark. No assignments will be accepted after the solutions have been posted (even if the solutions were posted within 24 hours after the deadline).
- Late submission of VHDL assignments will only be accepted within the first 24 hours after the deadline. Penalty for late submission of VHDL assignments: 40% of the mark.
- Penalty for incomplete submission of VHDL assignments
  - For partially submitted assignments, *i.e.*, some of the files (design/simulation/report) are missing, the penalty is at least 20% of the full mark of the assignment, depending on what is missing.
  - For assignments where all the design/simulation files are missing, *i.e.*, only a report was submitted, the penalty is 50% of the full mark of the assignment.

  - For not submitted assignments, *i.e.*, all files are missing, the penalty is 100% of the full mark of the assignment.

- **Quality of submitted work** - all submitted assignments must be written/typed in a formal manner, with complete answers to all questions, legible handwriting (if written), and clear marking of all questions/sections. Marks will be deducted for submitted work that doesn't follow these guidelines. Additional guidelines will be posted with the VHDL assignments.
- For any written assignment (*i.e.*, PP assignments, VHDL reports, midterms, and final exam), writing "I don't know" as an answer to any question for any number of questions within the assignment, will be graded with a mark of 20% of the full mark of the question (rounded down to the closest integer). Note, it may happen, for a specific question, that writing "I don't know" will result in a higher mark than an incorrect answer.
- Any request for reevaluation of an assignment must be made within a week of the return date of the assignment by contacting the instructor. Note that the entire assignment may be reevaluated. When requesting a reevaluation, attach a separate letter describing the reason for the reevaluation request – do not write anything on the original paper of the assignment.
- There will not be make-up examinations for students who miss an exam. The only exception is an approved deferral of the exam.
  - Final exam deferrals will be handled according to the Faculty of Engineering Guidelines posted here: https://www.mcgill.ca/engineering/students/undergraduate/courses-registration/exams-assessment/deferred-exams
  - Midterm deferrals will be handled according to the Faculty of Engineering Guidelines posted here: www.mcgill.ca/engineering/current-students/undergraduate/courses-registration/exams-assessment/midterms-and-class-tests/adjustments-missed-midterms-and-class-tests.
  - Approval of midterm deferrals is at the discretion of the instructor. If a midterm deferral request is approved, the weight of the missed midterm will be shifted to the second midterm or final exam.
  - Deferral requests from students who took a midterm or final exam will not be approved.
  - Students who miss a midterm for unjustified reasons will get a mark of zero for the missed exam.

6 Additional Information

Health and Wellness Resources at McGill University

Student well-being is a priority for the University. Below are some suggested resources that all students have access to for free. We highly encourage students to investigate and make use of the services available.

- **Student Wellness Hub** - All of McGill's health and wellness resources, integrated into a single hub; includes urgent care, self-help, various events and workshops, and more. Visit the Virtual Hub at mcgill.ca/wellness-hub or drop by the Brown Student Services Building (downtown) or Centennial Centre (Macdonald campus), COVID-19 regulations must be observed.
- **Office for Students with Disabilities (OSD)** - Works with students who have documented disabilities, mental health issues, chronic health conditions, or other impairments. Includes services such as note-taking, exam accommodations, access technology, and student funding. Visit mcgill.ca/osd/student-resources or drop by 1010 Sherbrooke Street West, Suite 410, COVID-19 regulations must be observed.
- **McGill Engineering Student Centre (MESC)** - Provides academic and career advising, wellness support, and peer tutoring services. Visit mcgill.ca/engineering/students/undergraduate/mesc or drop by FDA 22, COVID-19 regulations must be observed.
- **Local Wellness Advisor (LWA - Miss Lauren Weber)** - Trained clinicians are here to orient and connect you with the appropriate resource(s) for your unique situation. To make an appointment, visit mcgill.ca/lwa or ask for Lauren at MESC in FDA 22, COVID-19 regulations must be observed.

Copyright and Course Material

Use of Mobile Computing and Communications Devices

- Mobile computing and communications devices are permitted in class only for note taking or note consulting
- No audio or video recording of the lectures and/or tutorials is allowed

McGill
Faculty of Engineering

Course Outline

ECSE 222

Course Title:	**Digital Logic**
Credits:	**3**
Contact Hours:	**(3-2-4)**
Course Prerequisite(s):	**ECSE 202**
Course Corequisite(s):	**N/A**
Course Description:	**An introduction to digital logic, binary numbers and Boolean algebra, combinational circuits, optimized implementation of combinational circuits, arithmetic circuits, combinational circuit building blocks, flip-flops, registers, counters, design of digital circuits with VHDL, and synchronous sequential circuits.**

Canadian Engineering Accreditation Board (CEAB) Curriculum Content

CEAB curriculum category content	Number of AU's	Description
Math	**0**	Mathematics include appropriate elements of linear algebra, differential and integral calculus, differential equations, probability, statistics, numerical analysis, and discrete mathematics.
Natural science	**0**	Natural science includes elements of physics and chemistry, as well as life sciences and earth sciences. The subjects are intended to impart an understanding of natural phenomena and relationships through the use of analytical and/or experimental techniques.
Complementary studies	**0**	Complementary studies include the following areas of study to complement the technical content of the curriculum: engineering economics and project management; the impact of technology on society; subject matter that deals with the arts, humanities and social sciences; management; oral and written communications; health and safety; professionalism, ethics, equity and law; and sustainable development and environmental stewardship.
Engineering science	**26**	Engineering science involves the application of mathematics and natural science to practical problems. They may involve the development of mathematical or numerical techniques, modeling, simulation, and experimental procedures. Such subjects include, among others, applied aspects of strength of materials, fluid mechanics, thermodynamics, electrical and electronic circuits, soil mechanics, automatic control, aerodynamics, transport phenomena, elements of materials science, geoscience, computer science, and environmental science.
Engineering design	**26**	Engineering design integrates mathematics, natural sciences, engineering sciences, and complementary studies in order to develop elements, systems, and processes to meet specific needs. It is a creative, iterative, and open-ended process, subject to constraints which may be governed by standards or legislation to varying degrees depending upon the discipline. These constraints may also relate to economic, health, safety, environmental, societal or other interdisciplinary factors.

Accreditation units (AU's) are defined on an hourly basis for an activity which is granted academic credit and for which the associated number of hours corresponds to the actual contact time: one hour of lecture (corresponding to 50 minutes of activity) = 1 AU; one hour of laboratory or scheduled tutorial = 0.5 AU. Classes of other than the nominal 50-minute duration are treated proportionally. In assessing the time assigned to determine the AU's of various components of the curriculum, the actual instruction time exclusive of final examinations is used.

Graduate Attributes

This course contributes to the acquisition of graduate attributes as follows:

Graduate attribute	KB	PA	IN	DE	ET	IT	CS	PR	IE	EE	EP	LL
Level descriptor	I			I	I	I						

I = Introduced; D = Developed; A = Applied

KB *- Knowledge Base for Engineering: Demonstrated competence in university level mathematics, natural sciences, engineering fundamentals, and specialized engineering knowledge appropriate to the program.*

PA *- Problem Analysis: An ability to use appropriate knowledge and skills to identify, formulate, analyze, and solve complex engineering problems in order to reach substantiated conclusions.*

IN *- Investigation: An ability to conduct investigations of complex problems by methods that include appropriate experiments, analysis and interpretation of data, and synthesis of information in order to reach valid conclusions.*

DE *- Design: An ability to design solutions for complex, open-ended engineering problems and to design systems, components or processes that meet specified needs with appropriate attention to health and safety risks, applicable standards, economic, environmental, cultural and societal considerations.*

ET *- Use of Engineering Tools: An ability to create, select, adapt, and extend appropriate techniques, resources, and modern engineering tools to a range of engineering activities, from simple to complex, with an understanding of the associated limitations.*

IT *- Individual and Team Work: An ability to work effectively as a member and leader in teams, preferably in a multi-disciplinary setting.*

CS *- Communication Skills: An ability to communicate complex engineering concepts within the profession and with society at large. Such abilities include reading, writing, speaking and listening, and the ability to comprehend and write effective reports and design documentation, and to give and effectively respond to clear instructions.*

PR *- Professionalism: An understanding of the roles and responsibilities of the professional engineer in society, especially the primary role of protection of the public and the public interest.*

IE *- Impact of Engineering on Society and the Environment: An ability to analyse social and environmental aspects of engineering activities. Such abilities include an understanding of the interactions that engineering has with the economic, social, health, safety, legal, and cultural aspects of society; the uncertainties in the prediction of such interactions; and the concepts of sustainable design and development and environmental stewardship.*

EE *- Ethics and Equity: An ability to apply professional ethics, accountability, and equity.*

EP *- Economics and Project Management: An ability to appropriately incorporate economics and business practices including project, risk and change management into the practice of engineering, and to understand their limitations.*

LL *- Life-Long Learning: An ability to identify and to address their own educational needs in a changing world, sufficiently to maintain their competence and contribute to the advancement of knowledge.*

Policies

Academic Integrity

McGill University values academic integrity. Therefore, all students must understand the meaning and consequences of cheating, plagiarism and other academic offences under the Code of Student Conduct and Disciplinary Procedures.
(see www.mcgill.ca/students/srr/honest/ for more information).
(approved by Senate on 29 January 2003)

In accord with McGill University's Charter of Students' Rights, students in this course have the right to submit in English or in French any written work that is to be graded.
(approved by Senate on 21 January 2009)

Grading Policy

In the Faculty of Engineering, letter grades are assigned according to the grading scheme adopted by the professor in charge of a particular course. This may not correspond to practices in other Faculty and Schools in the University.

In the event of extraordinary circumstances beyond the University's control, the content and/or evaluation scheme in this course is subject to change.