Amin Sahebi

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Profile Summary

I'm a PhD student, have been admitted to the Smart Computing Program on November 2018, a joint program between three universities, Firenze, Pisa and Siena in Tuscany region. Currently, I'm working on Reconfigurable Architectures as High Performance Computing solutions for Artificial Intelligence Application.

Experiences

PHD STUDENT, SMART COMPUTING PROGRAM; ITALY – 2018–PRESENT

My researches are mostly focusing on reconfigurable architectures to accelerate performance of computing applications such as Artificial Intelligence real-world applications. I'm contributing in a team-work group and we have been powered with AXIOM project, which is a part of European Horizon 2020 project which already finished. My current tasks are comprising FPGA PL and PS side design (we are working on ZYNQ Ultrascale+ MPSoCs) including HLS-high level synthesized language and VHDL and Linux Embedded Device Driver development to have access our Metrics and Registers from User level side. Moreover, as some case studies, I worked on MAXELER accelerators to design and develop a Data-Flow FFT architecture which at the first step concluded to achieve the *Best Paper Award* of the IEEE MECO conference June 2019.

EMBEDDED SYSTEMS ENGINEER, MAPNA COMPANY; IRAN – 2013-2018

During 5 years working as Embedded System Engineer, my major activities were about Hardware solutions and firmware applications and protocols on real-time operating systems. I contributed to a research and development team with responsibilities to design and developing Main Processing Units (MPU) Firmware applications, operating system and interfaces, with a concentration on C/C++ applications, along with powerful IBM UML Modeling software tools. The environment of programming was almost in Unix-based operating systems such as Linux and QNX OS and almost using POSIX as standard programming API.

Activities

My recent activities including:

1. Developing Power Measurement and Timing Constraint measurement tool for Reconfigurable Architectures based on Data-Flow execution models.

2. Cooperation to design a reconfigurable architecture based on Data-Flow on Xilinx Ultrascale+ MPSoC hardware structure.

3. Design and contribute in finding novel Data-Flow architectures for well-know applications and their implementation on Data-Flow Accelerators such as MAXELER GALAVA board and MAX2C.

4. To find a real-world application as benchmark, I used to train and test some CNNs based on TensorFlow platform and Keras API.

5. Wide understanding of PetaLinux tool provided by Xilinx to make Board Support Packages including the PL side configuration.

6. Developing device drivers for linux based kernels, to extract necessary information from the under development architecture from PL and PS side of Xilinx Ultrascale+ MPSoC.

7. Usage, modification, and development of General Boot loaders to launch different Operating Systems (Mostly U-Boot).

Education

PhD, Computer Science, Smart Computing Program, 2018 - Present, Italy

MS, Electronic Engineering, Digital Electronic, 2011 - 2013, Iran

B.S, Electronic Engineering, 2006 - 2011, Iran

Research Interests

My research Interests can be categorized as following, sorted by their priority,

EMBEDDED SYSTEM DESIGN

– Artificial Intelligence, Neural Network, Image Processing

– Parallel and High Performance Computing

– Design and Computer-Aided Design of High-Speed Digital Integrated Circuits

– Industrial Internet of Things (IIOT)

ANALOG AND MIXED-SIGNAL INTEGRATED CIRCUITS AND SYSTEMS

– Analog and Digital Interfacing Circuits

– High Frequency Analog Circuits, Mixed-Signal, and Digital Integrated Circuits

Feature Graduated Courses

A short list of featured graduated courses in Smart Computing Program I've attended are as following,

1. Machine Learning: A Constrained-Based Approach, Prof. Marco Gori, Siena, April 2019, Siena.
2. Network Calculus for Deterministic Performance Analysis, Prof. Giovanni Stea, May 2019, Pisa.
3. Introduction to Generative Adversarial Networks, Prof. Marco Bertini and Prof. Lorenzo Seidenari, Sep-Oct 2019, Florence.

Teacher Assistantship

Teacher assistant, Electronic III, Spring 2009

Teacher assistant, Electromagnetic, Spring and Fall 2008

Publications

(Best Paper Award) L. Verdoscia, A. Sahebi and R. Giorgi, "A Data-Flow Methodology for Accelerating FFT," *2019 8th Mediterranean Conference on Embedded Computing (MECO)*, Budva, Montenegro, 2019, pp. 1-4.