Amin SAHEBI

PhD Computer Science | Hardware Engineer | Embedded Systems

linkedin.com/in/amin-sahebi-47370039/ bitbucket.org/AminSahebi

+39 331 206 7519 sahebi.amin@gmail.com amin.sahebi@unifi.it
via dei pispini 122, Siena, Italy
born in 4 June 1988, Gorgan/Iran, Live in Tuscany, Italy

I'm a PhD student, have been admitted to the Smart Computing Program in November 2018, a joint program between three universities, Florence, Pisa and Siena Italy. Currently, I'm working as a visiting researcher with "Custom Computing Research Group at Imperial College London" on Reconfigurable Architectures as High-Performance Computing solutions for Artificial Intelligence Application. I'm highly interested in Embedded system design and development with looking for high performance computing approaches. I have been reviewer of Top Rank Conferences such as FPL, ARC and ARC for last 3 years.

SKILLS

Programming Languages	**C/C++11**, **HLS**, **VHDL**, Python, Bash Script
Programming Models	**Dataflow Threads**, **OpenMP**, **MPI+X**, OmpSs
Development Platforms	Unix-based systems, Heterogeneous systems (Mostly Xilinx Zynq MPSoC Platforms (FPGA + arm), Maxeler Platforms (Dataflow Engine), Xilinx ALVEO U250 and U280
Architectures	x86_64, aarch64
Development tools	Cross Compile GNU compilers, CMake, vi editor, Eclipse, Clion, Visual Studio Code, Qt, vivado design suite

EXPERIENCES

Present – Oct 2018

PhD Student, INFORMATION ENGINEERING, University of Florence

- I have been admitted as a visiting researcher to Custom Computing Research Group in Imperial College London, under supervision of Professor Wayne Luk. During this visit (virtual because of COVID-19) I'm collaborating on Massive Scale Distributed Computing Project. The project has been structured as a novel method to deploy on Maxeler DFE engines MPC-X.

My research mostly focuses on reconfigurable architectures to accelerate performance of computing applications such as Artificial Intelligence real-world applications. I'm contributing in a team-work group and we have been powered with AXIOM project, which is a part of European Horizon 2020 project. My current tasks comprise FPGA design (we are working on ZYNQ Ultrascale+ MPSoCs) including HLS-high level synthesized language and VHDL and Linux Embedded Device Driver development to have access the logic from User level side.
My contribution is also considered as developing benchmarks written in C/C++ and extend it to the real-world application with the baseline of Parallel Programming Paradigms such as OpenMP, OpenmPI and OpmSs Parallel Programming Languages. Moreover, as some case studies, I worked on Maxeler accelerators to design and develop a Data-Flow FFT architecture which at the first step concluded to achieve the Best Paper Award of the IEEE MECO conference June 2019.

C/C++ | Computer Architecture | Cache | Device Drivers | VHDL | Dataflow | FPGA | Maxeler | Xilinx Ultrascale+ | OMP | OpenMPI

Sept 2018 – Oct 2013

Hardware Engineer, MAPNA, Iran

During 5 years working as Embedded System Engineer, my major activities were about Hardware solutions and firmware applications and protocols on real-time operating systems. I contributed to a research and development team with responsibilities to design and developing Main Processing Units (MPU), The PCB plus Firmware applications, operating system and interfaces, such as Modbus, Profibus, USB, Ethernet, I2C, SPI, CAN and etc., with a concentration on C/C++ applications, along with powerful IBM UML Modeling software tools.
The environment of programming was almost in Unix-based operating systems such as Linux and QNX OS and almost using POSIX as standard programming API and Vivado for VHDL to program the FPGA module. Moreover, I got experienced as Network administration, server maintenance and project management.*Design Materials -the non-confidential parts- can be sent on request.*

Embedded Systems | UML | C/C++ | PCB Design | IO Cards

Projects

General Prpjects — 2021

bitbucket.org/AminSahebi/

In my bitbucket repository there are some General works (and some forked) which I keep them there. However, as you know there are manu stuff that are private or may not be possible to share it online, therefore, these materials will be discussed based on request.

C/C++ | HLS | FPGA | OmpSs | Parallel Programming | Python | bash script

DRT Runtime — 2021

bitbucket.org/AminSahebi/dataflow-runtime/src/master/

DRT (Dataflow Run-Time) is a tool that enables the fast prototyping of those benchmarks for the Dataflow Threads (DF-Threads) PXM. In this work, we show how to use DRT to develop dataflow based examples to be targeted by a future compiler for the dataflow PXM. The presentation is published here : My Presentation at ARCS-21 Conference

C/C++ | Runtime | Dataflow Programming | thread-level parallelism

Parallel Programming — 2020

bitbucket.org/AminSahebi/ompss/src/master/
bitbucket.org/AminSahebi/cilk/src/master/

I contributed in some parallel programming solutions as a baseline of our projects, such as OmpSs and OpenMPI, for multicore programming I used OpenMP and Cilk. Many good benchmarks comparisons and scalability tests have been done with both OpenMPI and Ompss.

Parallel Programming | openMPI | openMP | MPI+X

GLUON Board — 2020

bitbucket.org/AminSahebi/gluon/src/master/

There was a need to exploit all serial transceivers of Xilinx Zynq Ultrascale+, plus, can also capable of carrying full operating system support with a sufficient amount of memory. We designed the GLUON board, which can provide all these requirements.

PCB Design | Altium Designer | FPGA

Languages

Persian ●●●●●
English ●●●●○
Italian ●●○○○

Teaching Assistant

- Electronic III, Spring 2009
- Electromagnetic, Spring and Fall 2008

Education

2020-2021 Visiting Researcher at the **Imperial College London**.
2018-2021 PhD of Computer Science atSmart Computing program at the **University of Florence**, Italy.
2011-2013 Master of Science in Digital Electronics at the University of Shahroud, Iran.
2006-2011 Bachelor of Science in Electronics Engineering at the University of Mazandaran, Iran.

Publications

2019 **Best Paper Award** L. Verdoscia, A. Sahebi and R. Giorgi, "A Data Flow Methodology for Accelerating FFT," 8th Mediterranean Conference on Embedded Computing (Budva, Montenegro, 2019, pp. 1-4.

2021 A. Sahebi, M. Procaccini, R. Giorgi, " A lightweight runtime for developing benchmarks for a data flow execution model", 2021 34th GI/ITG International Conference of Architecture Computing System (ARCS).

2020 A. Sahebi, R. Giorgi, " The High Speed Inexpensive and Easy Interconnect Solution", 2020 HiPEAC International Summer School, ACACES.

2013 Soleimani, A., and A. Sahebi. "Using Neural Networks to Predict Road Roughness." Journal of Solid and Fluid Mechanics 2.3 (2012)