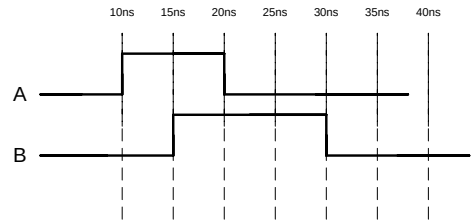
Shahid Beheshti University
Faculty of Computer Science and Engineering

Computer Aided Digital System Design
Homework No.1

1. Sketch the waveform of the output and internal signals.

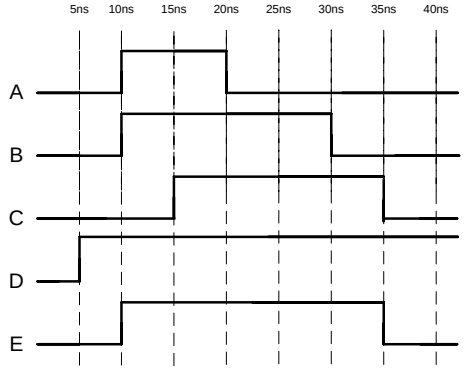
```
ENTITY excercise1 IS
     PORT (    a, b : IN  bit;
               y    : OUT bit);
END test;
ARCHITECTURE test OF excercise1 IS
     SIGNAL n1 : bit;
BEGIN
     n1 <= NOT b AFTER 3 ns;
     y <= a XOR n1 AFTER 5 ns;
END test;
```



2. Sketch the waveform of the output and internal signals.

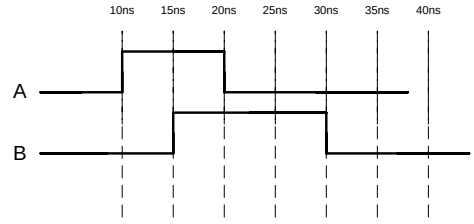
```
ENTITY excercise1 IS
     PORT (    a, b, c, d, e : IN  bit;
               y             : OUT bit);
END test;
ARCHITECTURE test OF excercise1 IS
     SIGNAL n1, n2, n3 : bit;
BEGIN
     n1 <= a AND b;
     n2 <= d AND e;
     n3 <= n1 XOR c AFTER 3 ns;
     y <= n1 XOR n2 XOR n3 AFTER 4 ns;

END test;
```



3. Sketch the waveform of the output and internal signals.

```
ENTITY excercise1 IS
     PORT (    a, b : IN  bit;
               y    : OUT bit);
END test;
ARCHITECTURE test OF excercise1 IS
     SIGNAL n1 : bit;
BEGIN
     n1 <= NOT b AFTER;
     y <= a XOR n1 AFTER;
END test;
```



4. Sketch the waveform of the output and internal signals.

```
ENTITY excercise2 IS END test;
ARCHITECTURE test OF excercise2 IS
    SIGNAL y : bit;
BEGIN
    y <= NOT y;
END test;
```

Ali Jahanian