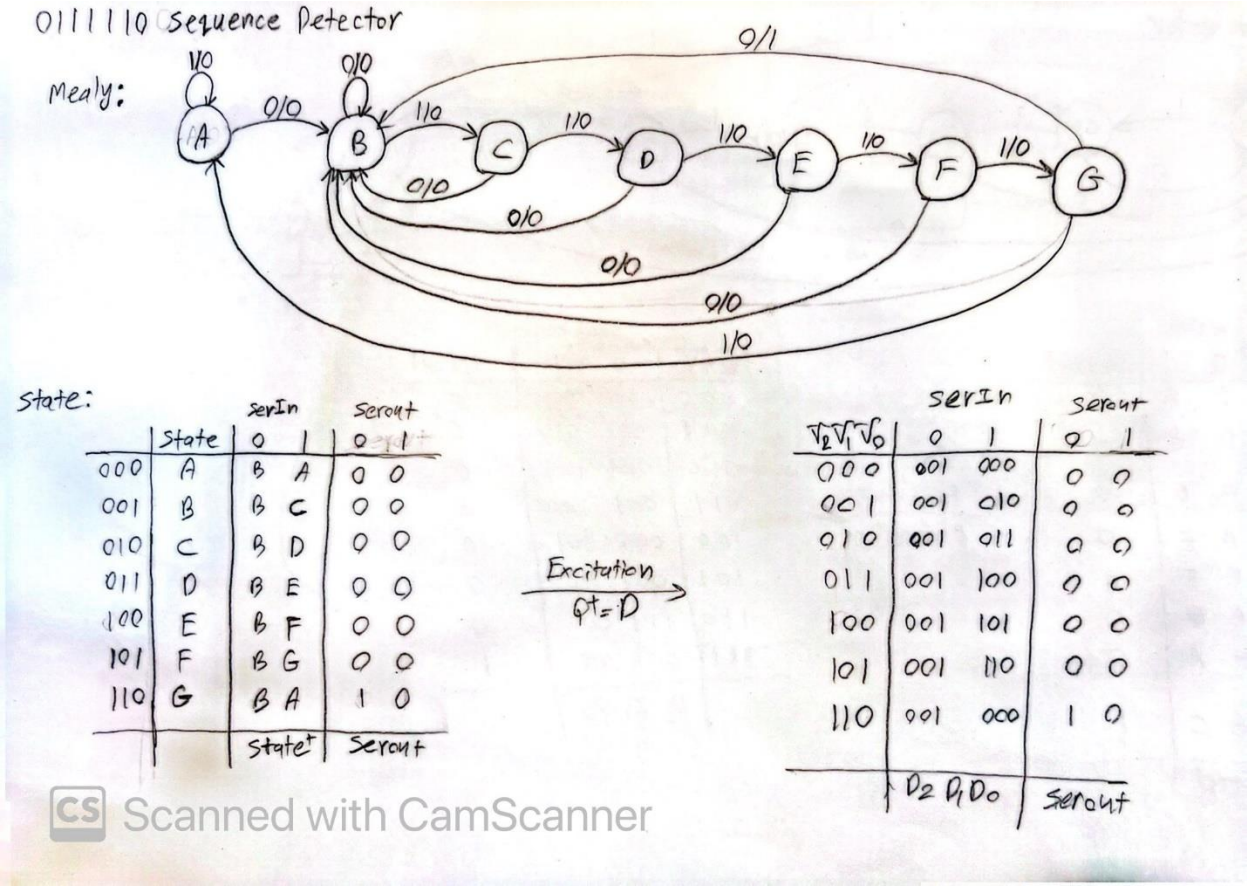
Amin Aghakasiri 810101381

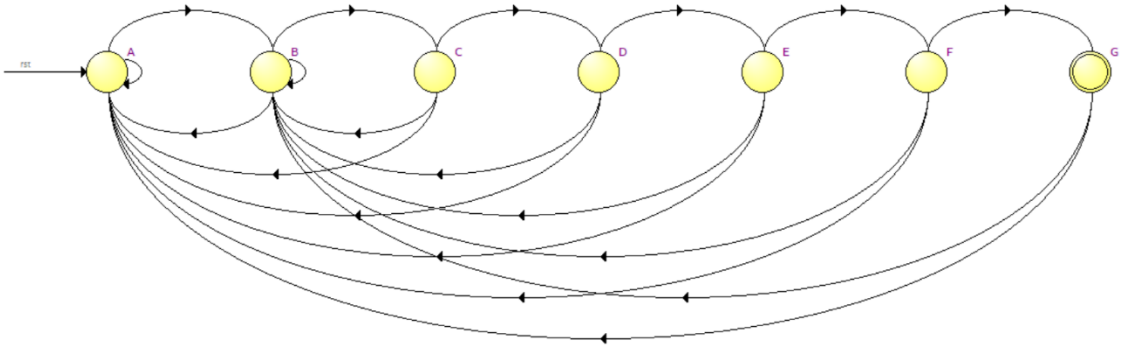
CA5 Report

Part a:

i.

Diagram and state machine for mealy machine:





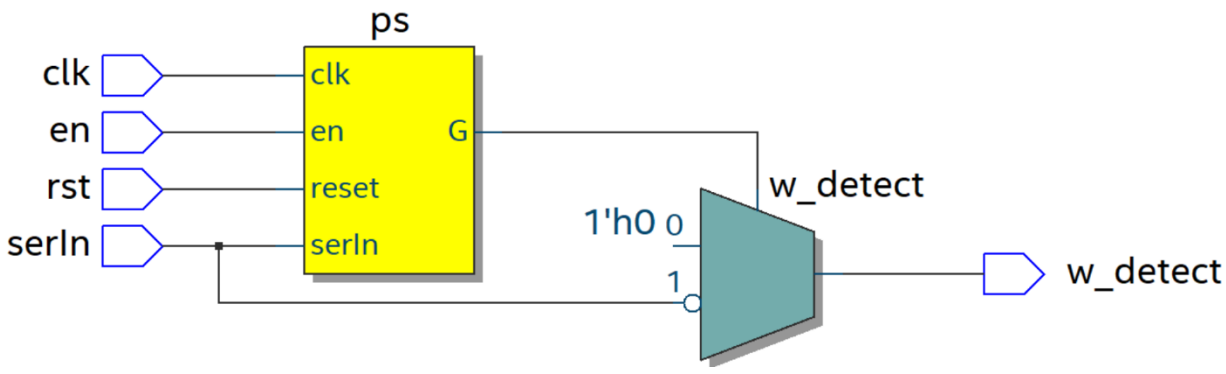
Mealy Machine code and test bench:

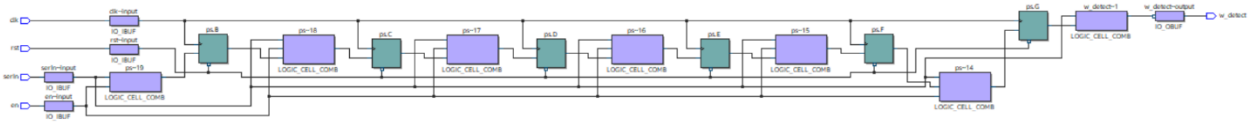
```
module Mealy (input clk,rst,serIn,en,output w_detect);
    reg[2:0] ns,ps;
    parameter [2:0] A=3'b000,B=3'b001,C=3'b010,D=3'b011,E=3'b100,F=3'b101,G=3'b110;

    always @(ps,serIn) begin
        ns = A;
        case (ps)
            A: ns= serIn ? A:B;
            B: ns= serIn ? C:B;
            C: ns= serIn ? D:B;
            D: ns= serIn ? E:B;
            E: ns= serIn ? F:B;
            F: ns= serIn ? G:B;
            G: ns= serIn ? A:B;
            default: ns=A;
        endcase
    end
    assign w_detect = (ps == G)? ~serIn: 1'b0;
    always @(posedge clk,posedge rst) begin
        if(rst)
            ps<=A;
        else if(~en)
            ps <= A;
        else
            ps<=ns;
    end
endmodule
```

```
1   `timescale 1ns/1ns
2   module testb ();
3       reg serIn=0,clk=0,rst=0,en=0;
4       wire w_detect_moore;
5       Mealy UUT(clk,rst,serIn,en,w_detect_moore);
6       always #100 clk = ~clk;
7       initial begin
8               #50
9               #200 serIn = 0;
10              #200 serIn = 1;
11              #200 serIn = 1;
12              #200 serIn = 1;
13              #200 serIn = 1;
14              #200 serIn = 1;
15              #200 serIn = 0;
16              #200 $stop;
17      end
18  endmodule
```

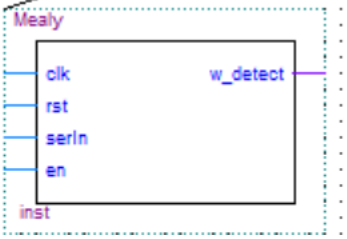
ii.

Symbols using RTL Viewer and Technology Map viewer:





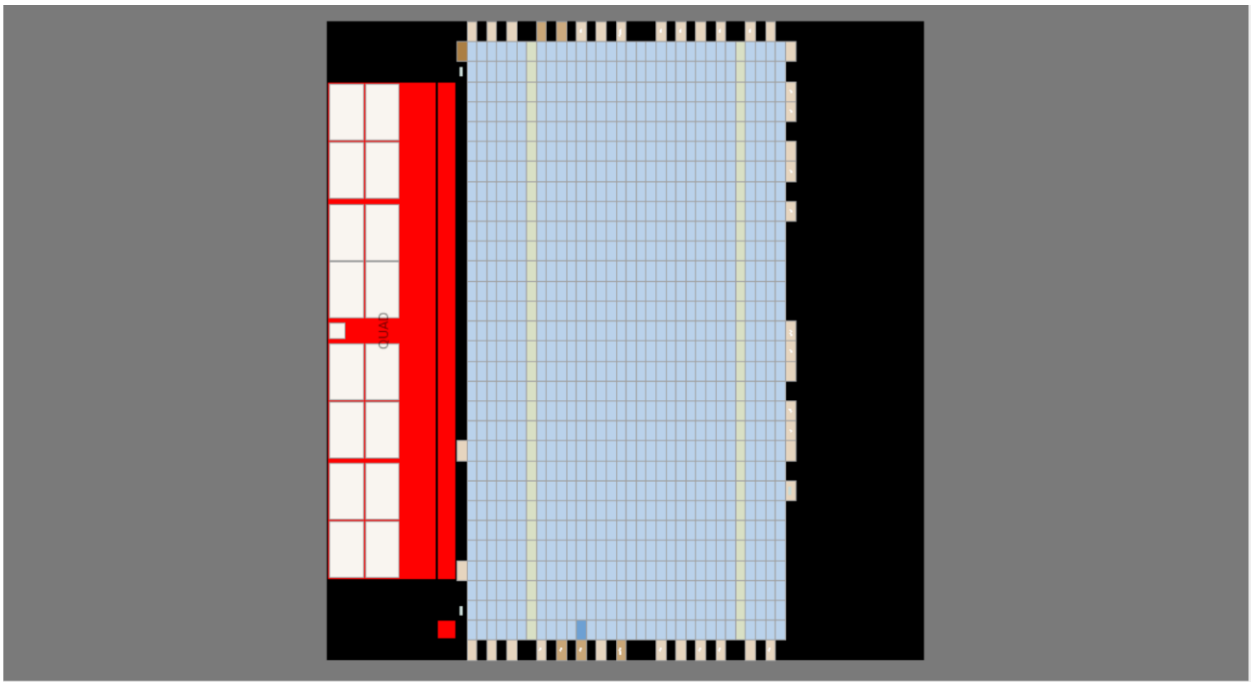
Parameter	Value	Type
A	000	Unsigned Binary
B	001	Unsigned Binary
C	010	Unsigned Binary
D	011	Unsigned Binary
E	100	Unsigned Binary
F	101	Unsigned Binary
G	110	Unsigned Binary



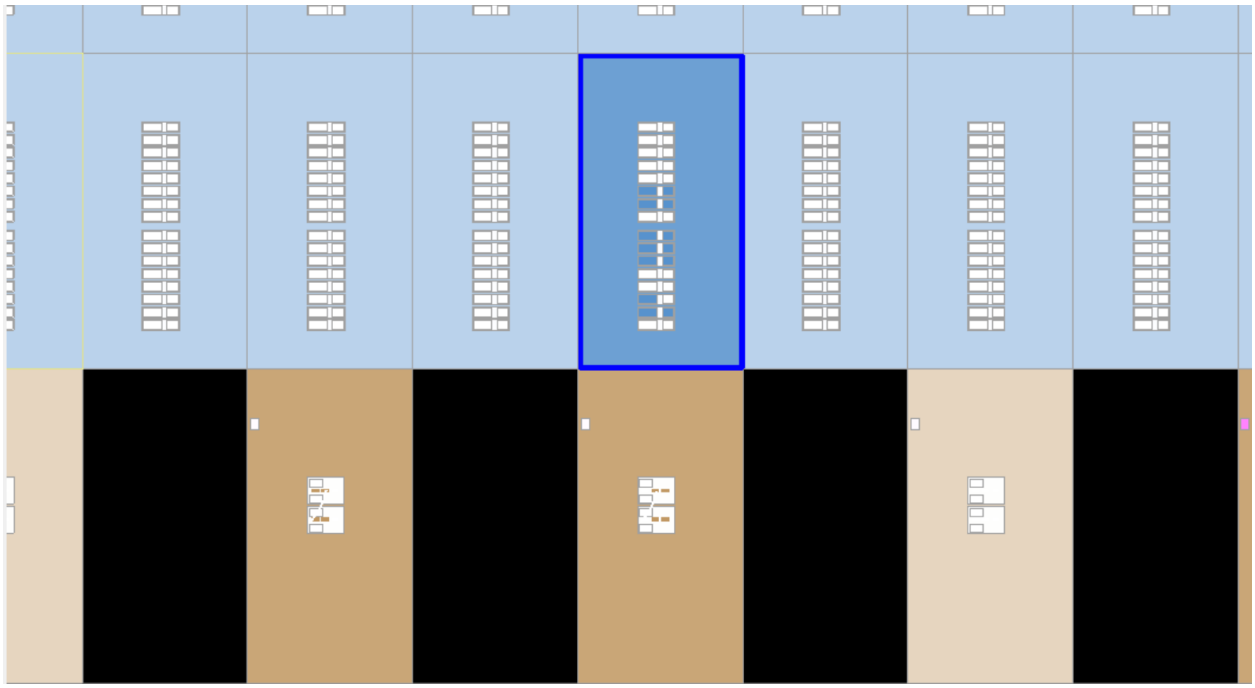
Resources used for building the curcuit(after synthesis):

Flow Status	Successful - Sat Dec 30 21:09:02 2023
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	Mealy
Top-level Entity Name	Mealy
Family	Cyclone IV GX
Device	EP4CGX15BF14A7
Timing Models	Final
Total logic elements	7 / 14,400 (< 1 %)
Total registers	6
Total pins	5 / 81 (6 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)

Floor plan:

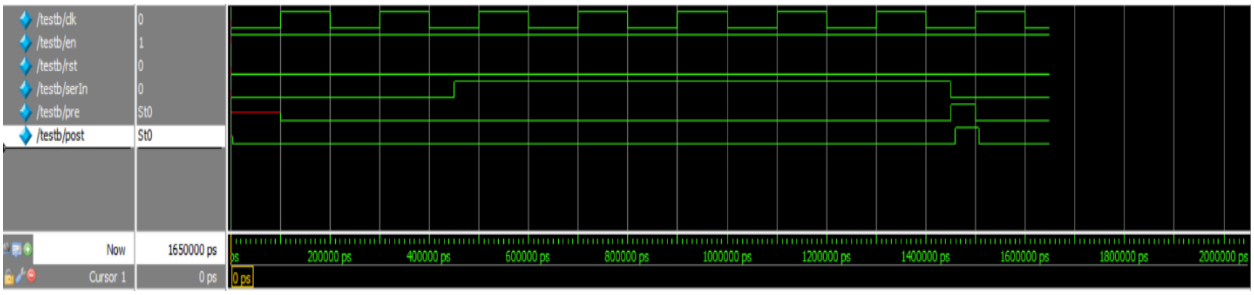


The light blue blocks are logic blocks. The yellow blocks are memory blocks. The tan blocks around the edge are I/O blocks. The dark blue block are used blocks for building logics of this circuit(which is 1 in this).



The last picture is the used logic block for building this circuit. Each logic block is made of 16 logic elements. As we can see, 7 logic elements are used for building this circuit.

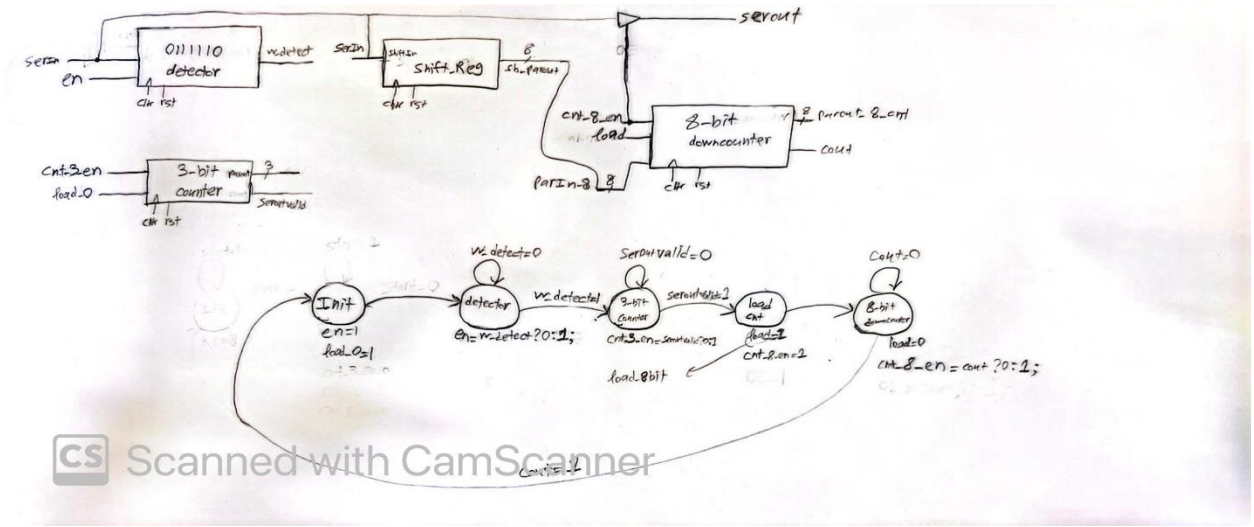
iii.



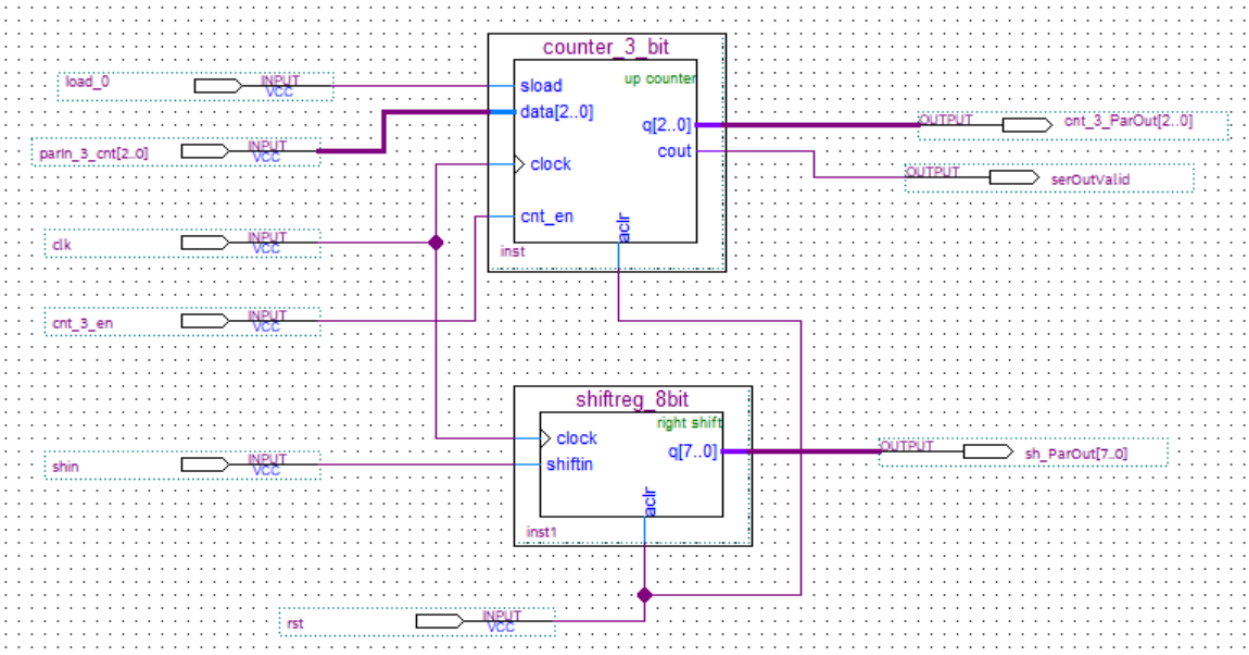
The post-synthesis is based on the delays which are presented in .sdo file that leads to a time difference in comparison to the pre-synthesis module. In post-synthesis version we have a little delay before the changes on the output whereas in the pre-synthesis version, the changes are instant.

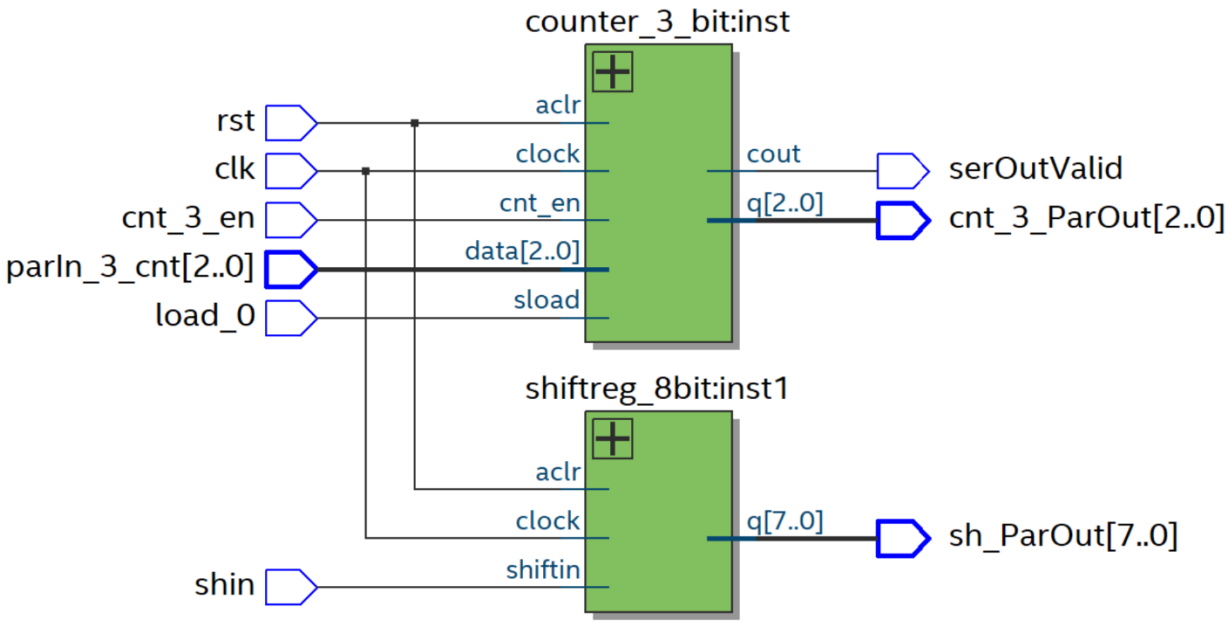
Part b:

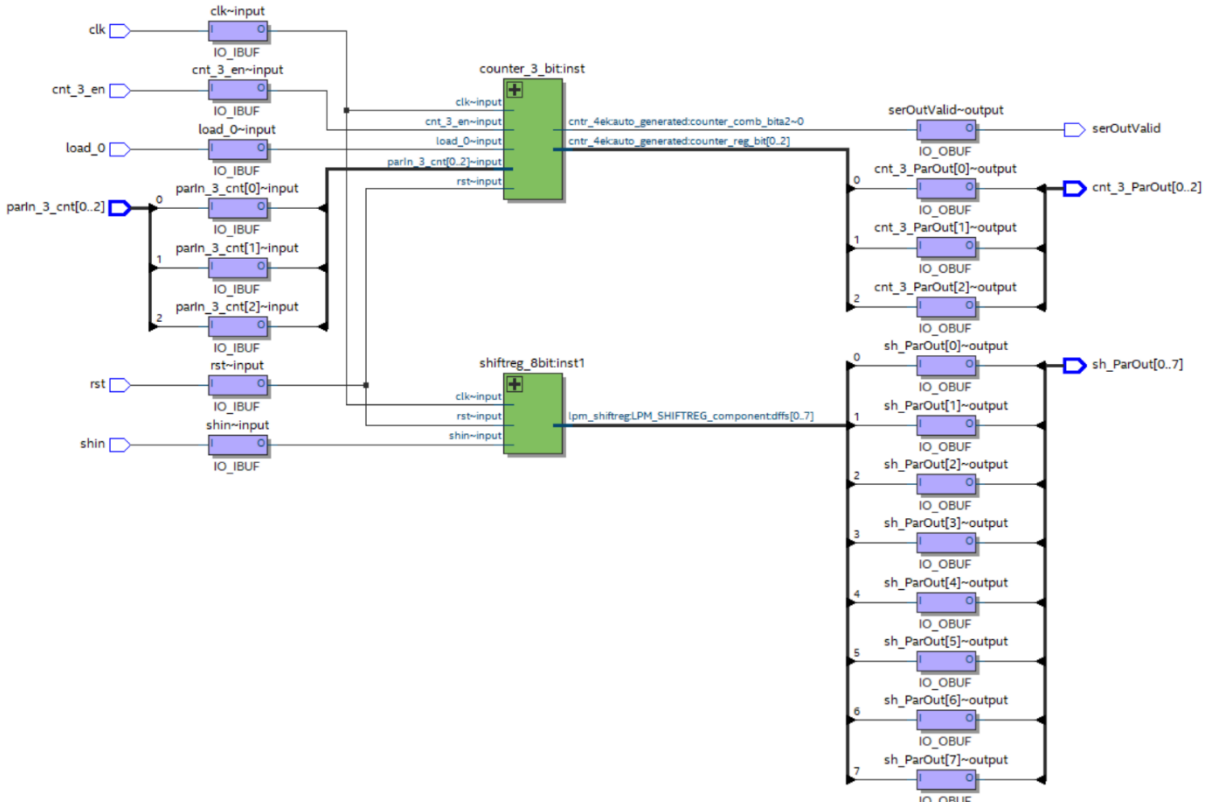
The complete diagram of the project:



Symbols using RTL Viewer and Technology Map viewer:



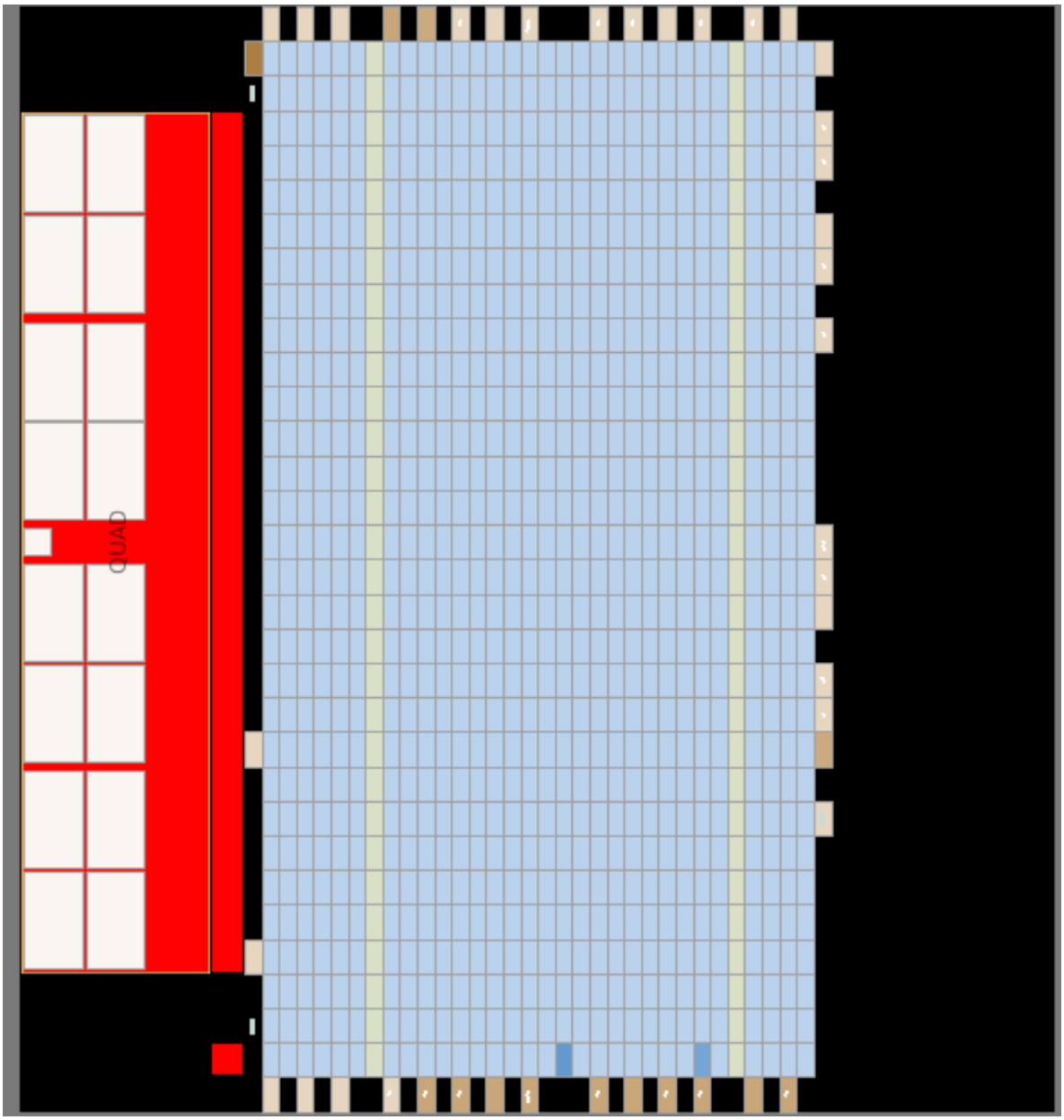




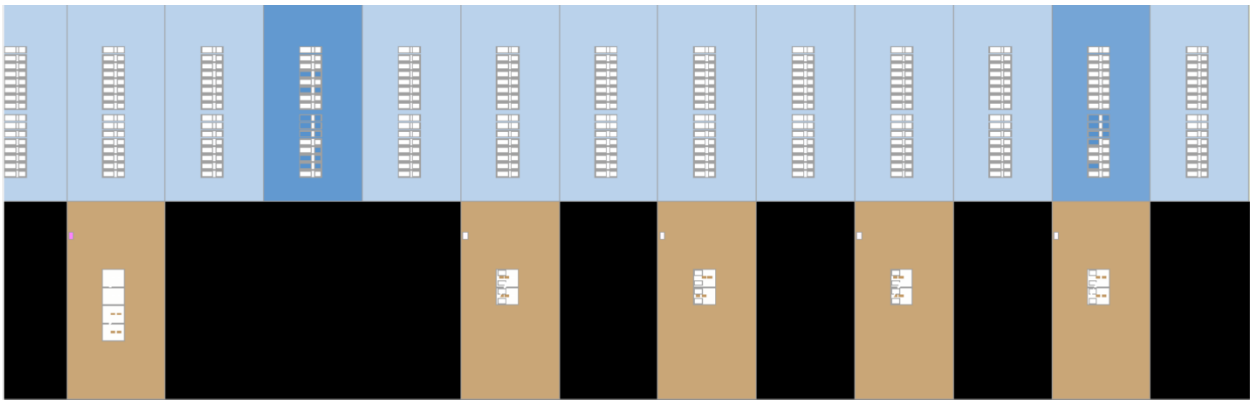
Resources used for building the curcuit(after synthesis):

Flow Status	Successful - Sun Dec 31 20:29:13 2023
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	bit_counter
Top-level Entity Name	bit_counter
Family	Cyclone IV GX
Device	EP4CGX15BF14A7
Timing Models	Final
Total logic elements	13 / 14,400 (< 1 %)
Total registers	11
Total pins	20 / 81 (25 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)

Floor plan:



Two blocks are used for building the logic of this circuit.



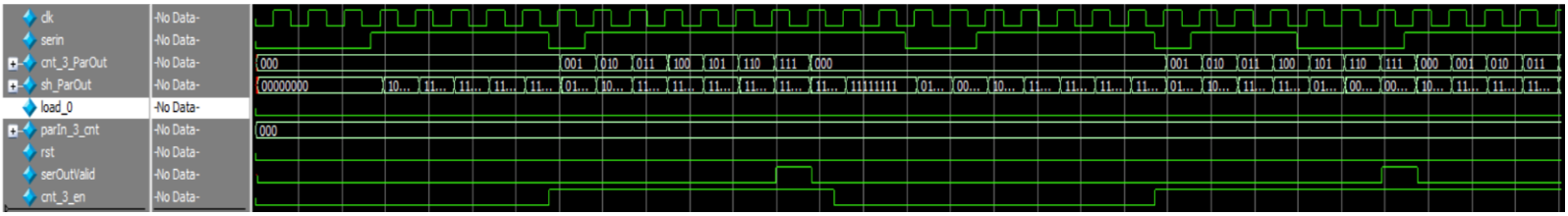
Two logic blocks are used for building this circuit that the left one uses 7 logic elements and the right one uses 5 logic elements.

ii.

Testbench:

```
`timescale 1ns/1ns
module ex2_tb();
    reg serin=0,cnt_3_en=0,clk=0,rst=0,load_0 = 1;
    wire serOutValid;
    wire [7:0] sh_ParOut;
    wire [2:0] cnt_3_ParOut;
    reg [2:0] parIn_3_cnt = 3'b000;
    bit_counter UUT3(serOutValid,load_0,clk,cnt_3_en,rst,parIn_3_cnt,cnt_3_ParOut,sh_ParOut,serin);
    initial forever begin #41;clk=~clk; end
    initial begin
    load_0 = 0;
        #82;
        #82;
        #20; serin=0;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1;
        #82; serin=0; cnt_3_en=1;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1; cnt_3_en=0;
        #82; serin=1;
        #82; serin=0;
        #82; serin=0;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1;
        #82; serin=0; cnt_3_en=1;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1;
        #82; serin=0;
        #82; serin=0;
        #82; serin=0;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1;
        #200
        $stop;
    end
endmodule
```

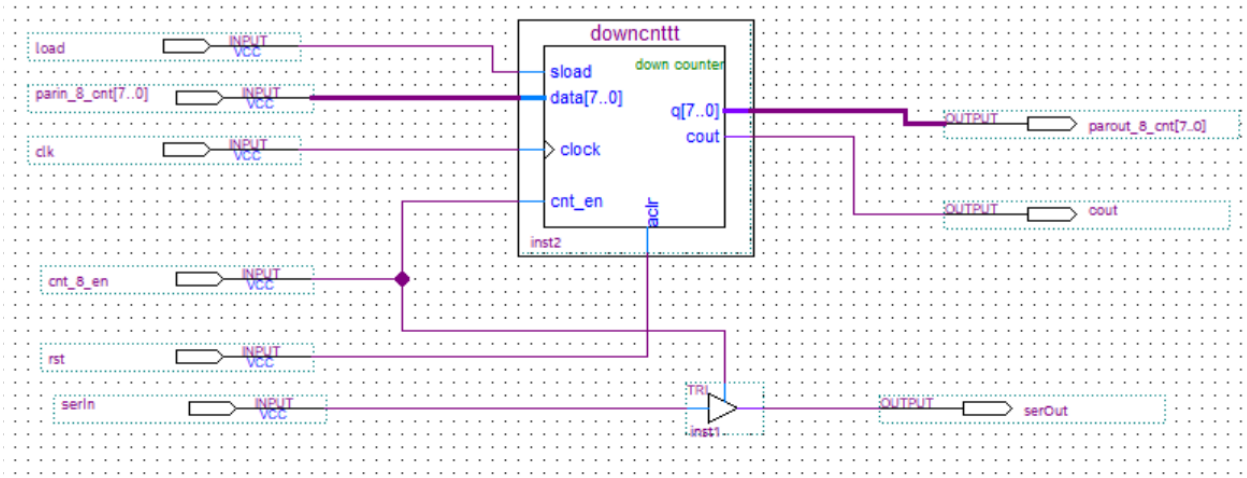
Result of the testbench:

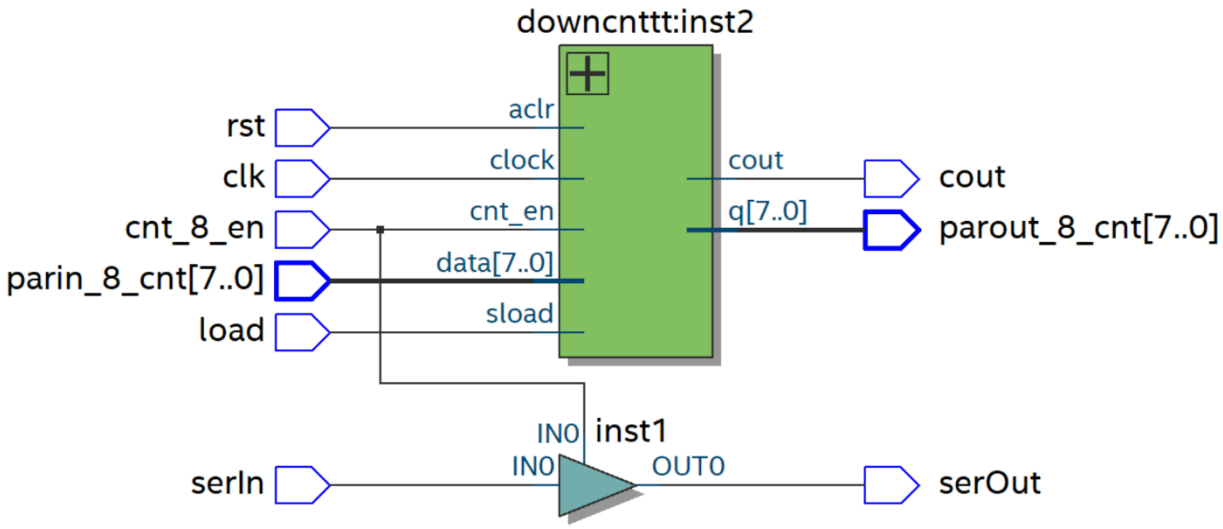


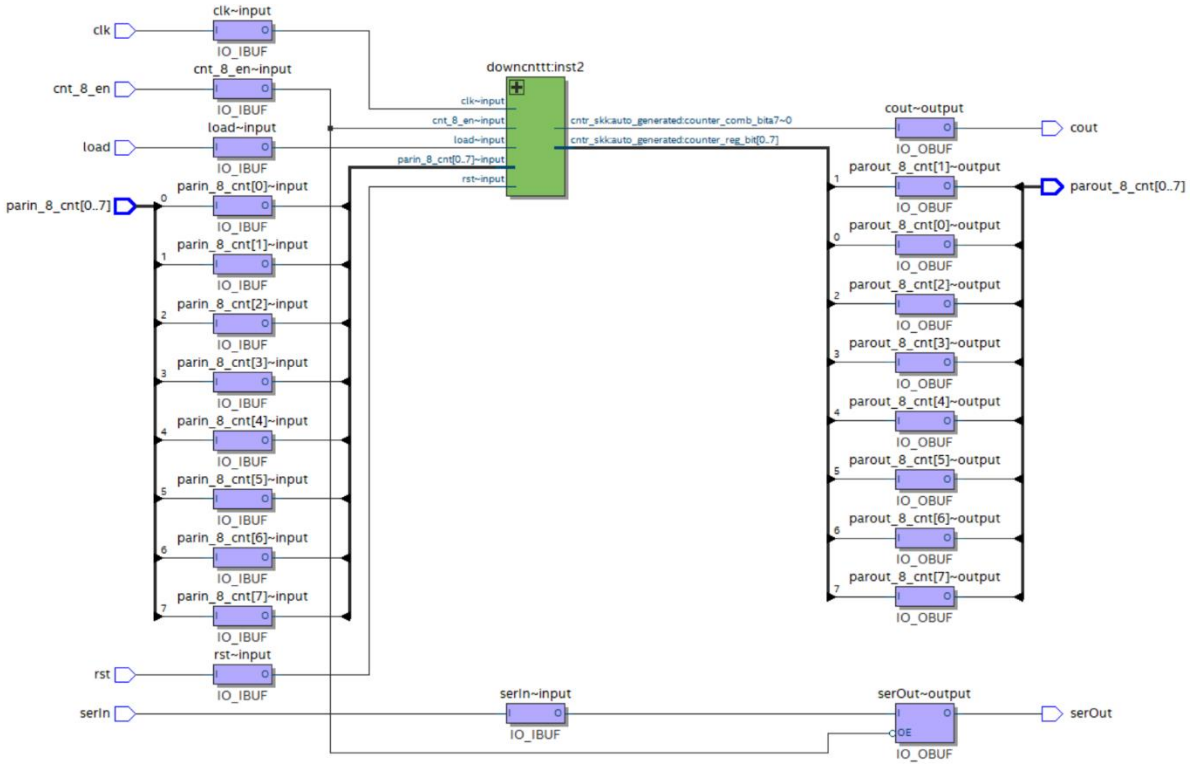
Part c:

i.

Symbols using RTL Viewer and Technology Map viewer:



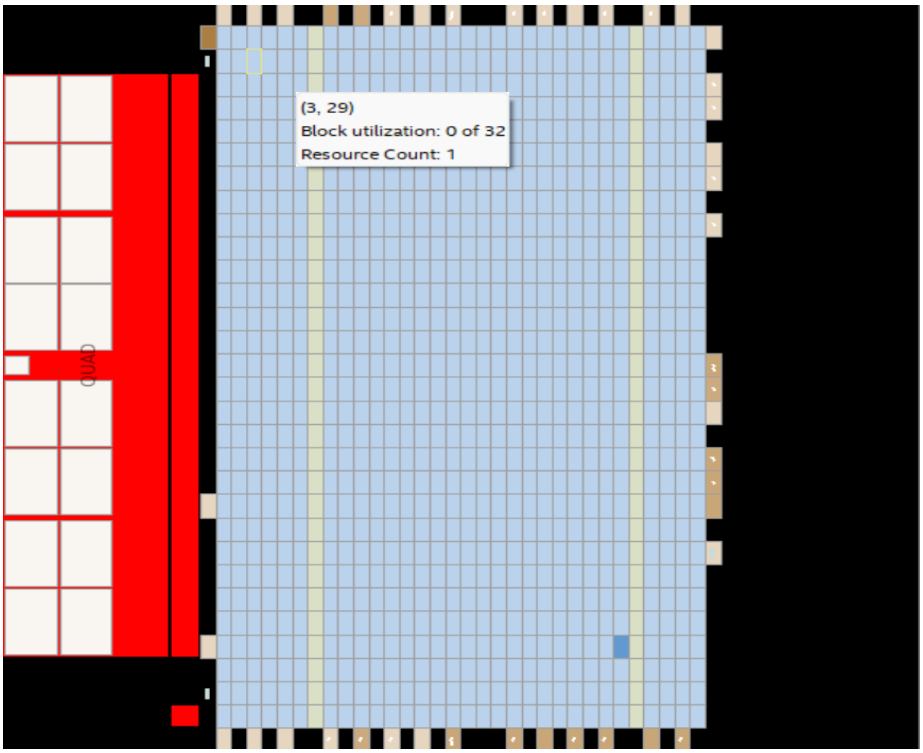

downcnttt:inst2
rst
clk
cnt_8_en
parin_8_cnt[7..0]
load
aclr
clock
cnt_en
data[7..0]
sload
cout
q[7..0]
cout
parout_8_cnt[7..0]
IN0
inst1
IN0
OUT0
serIn
serOut


clk
clk~input
IO_IBUF
cnt_8_en
cnt_8_en~input
IO_IBUF
load
load~input
IO_IBUF
parin_8_cnt[0..7]
parin_8_cnt[0]~input
parin_8_cnt[1]~input
parin_8_cnt[2]~input
parin_8_cnt[3]~input
parin_8_cnt[4]~input
parin_8_cnt[5]~input
parin_8_cnt[6]~input
parin_8_cnt[7]~input
rst
rst~input
serIn
serIn~input
downcnttt:inst2
clk~input
cnt_8_en~input
load~input
parin_8_cnt[0..7]~input
rst~input
cntr_skkauto_generated:counter_comb_bita7~0
cntr_skkauto_generated:counter_reg_bit[0..7]
cout~output
cout
parout_8_cnt[1]~output
parout_8_cnt[0]~output
parout_8_cnt[2]~output
parout_8_cnt[3]~output
parout_8_cnt[4]~output
parout_8_cnt[5]~output
parout_8_cnt[6]~output
parout_8_cnt[7]~output
parout_8_cnt[0..7]
IO_OBUF
serOut~output
serOut
OE

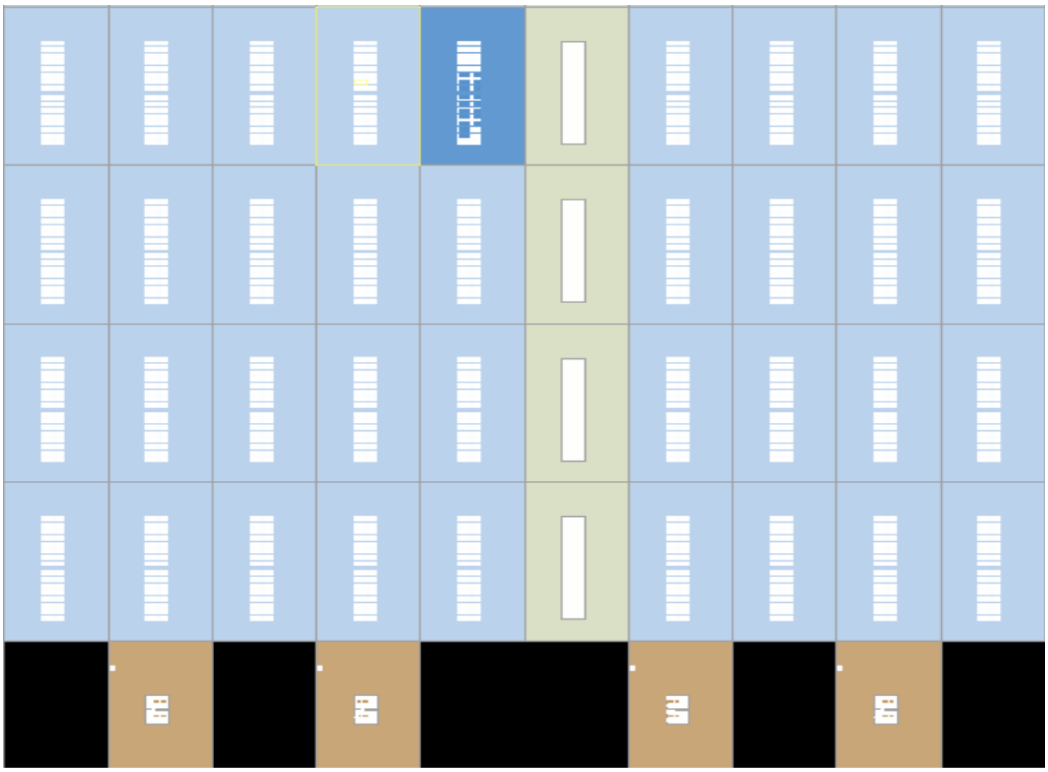
Resources used for building the curcuit(after synthesis):

Flow Status	Successful - Sun Dec 31 21:03:22 2023
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	bitt_transmittor
Top-level Entity Name	bitt_transmittor
Family	Cyclone IV GX
Device	EP4CGX15BF14A7
Timing Models	Final
Total logic elements	10 / 14,400 (< 1 %)
Total registers	8
Total pins	23 / 81 (28 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)

Floor plan:



One logic block is used for building the logic of this circuit.



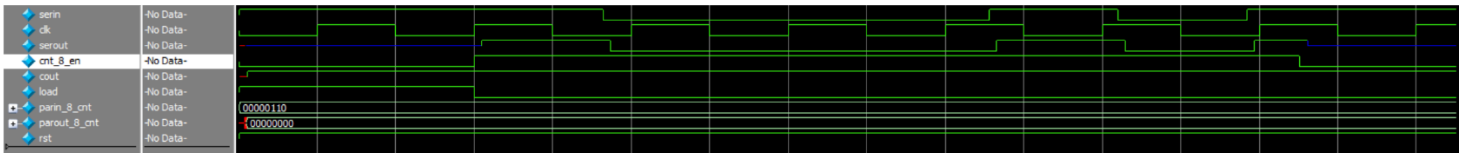
One logic block is used for building this circuit that uses 9 logic elements.

ii.

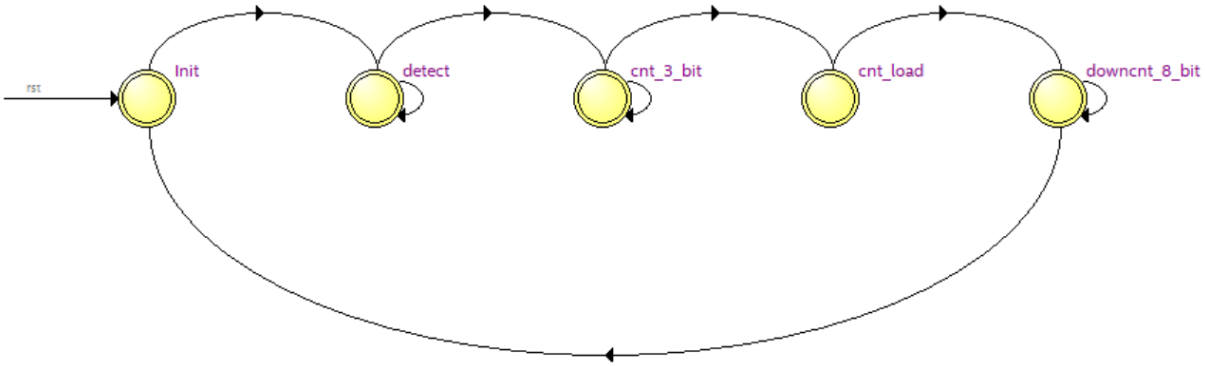
Testbench:

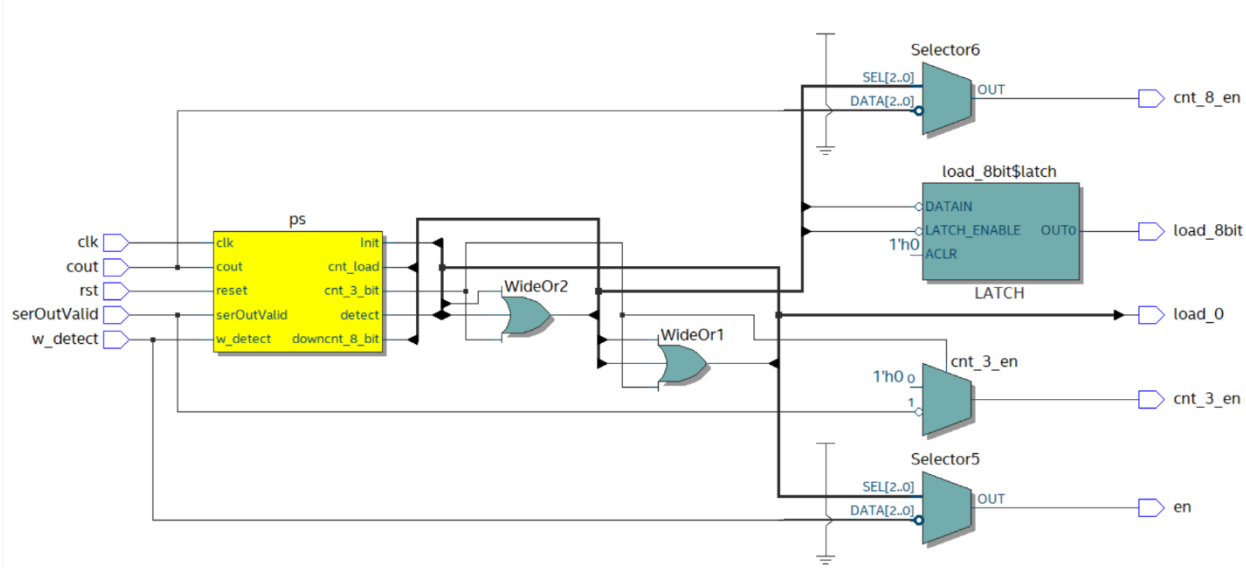
```
`timescale 1ns/1ns
module transmitter_tb();
    reg serin=1, clk=0, rst=1,cnt_8_en=0,load=1;
    wire [7:0] parout_8_cnt;
    wire cout,serout;
    reg [7:0] parin_8_cnt=8'b00000110;
    bit_transmitter UUT(serout,serin,cnt_8_en,cout,clk,rst,load,parin_8_cnt,parout_8_cnt);
    initial forever begin #50;clk=~clk; end
    initial begin
        #150; cnt_8_en=1; load=0;
        #82; serin=0;
        #82; serin=0;
        #82; serin=0;
        #82; serin=1;
        #82; serin=0;
        #82; serin=1;
        #34; cnt_8_en=0;
        #100
        $stop;
    end
endmodule
```

Result of the testbench:



Controller Part:





Resources used for building the curcuit(after synthesis):

Flow Status	Successful - Sun Dec 31 21:22:14 2023
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	control
Top-level Entity Name	control
Family	Cyclone IV GX
Device	EP4CGX15BF14A7
Timing Models	Final
Total logic elements	10 / 14,400 (< 1 %)
Total registers	5
Total pins	10 / 81 (12 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)

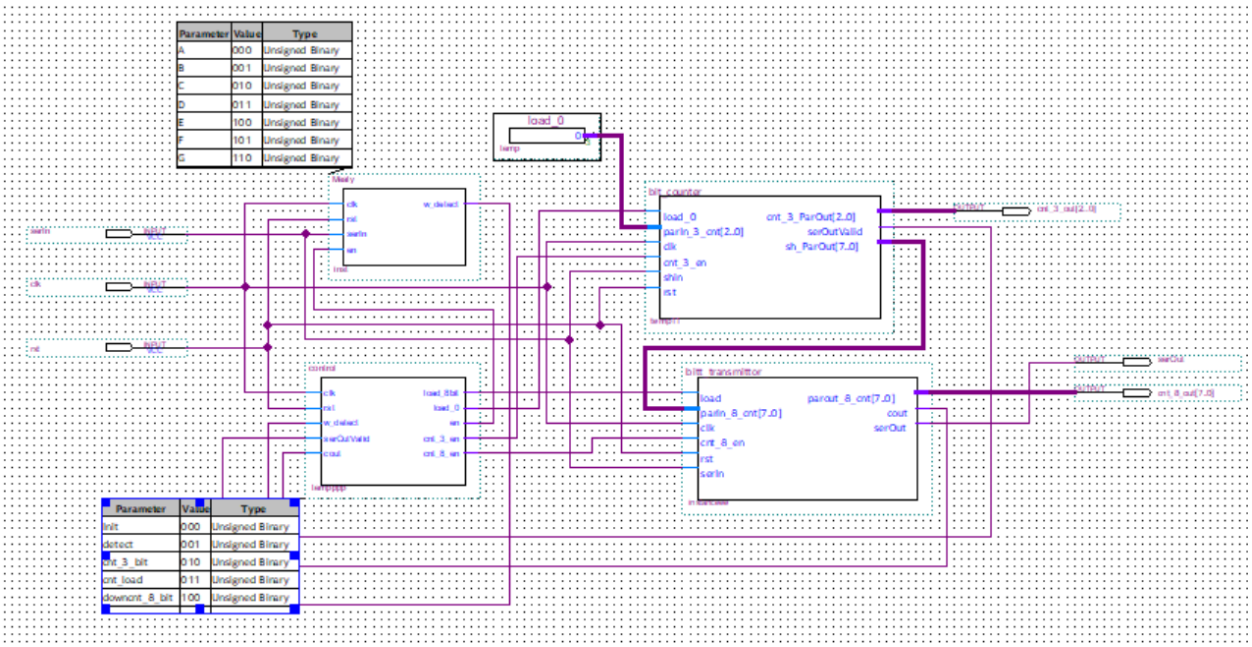
Code of the controller:

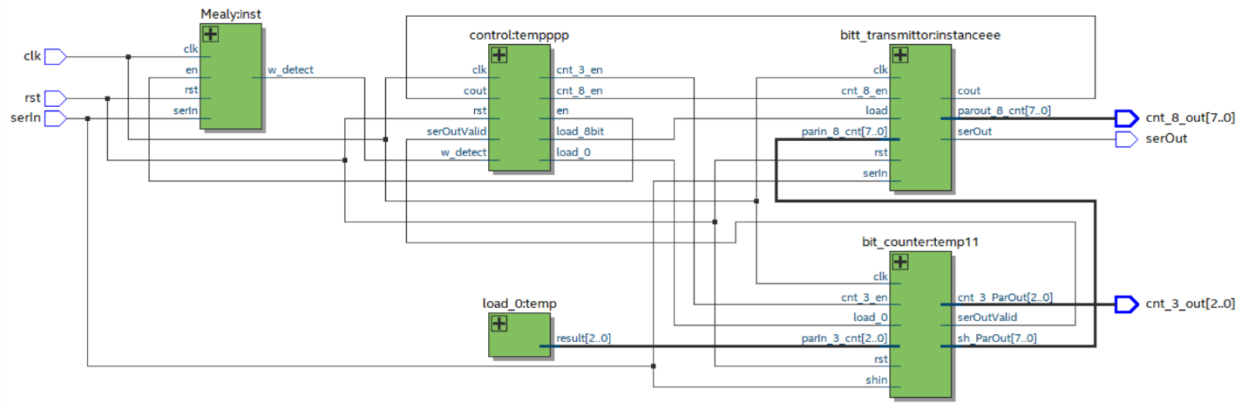
```
module control(input clk,rst,w_detect,serOutValid,cout, output reg load_8bit,load_0,en,cnt_3_en,cnt_8_en);
    reg[2:0] ps,ns;
    parameter[2:0] Init = 0, detect = 1, cnt_3_bit = 2, cnt_load = 3, downcnt_8_bit = 4;
    always @(ps,w_detect,serOutValid,cout) begin
        ns = Init;
        {load_0,en,cnt_3_en,cnt_8_en} = 4'b0;
        case (ps)
            Init : begin ns = detect; en=1;load_0=1; end
            detect : begin ns = w_detect ? cnt_3_bit : detect; en=w_detect?0:1; end
            cnt_3_bit : begin ns = serOutValid ? cnt_load : cnt_3_bit; cnt_3_en = serOutValid?0:1; end
            cnt_load : begin ns = downcnt_8_bit; load_8bit=1;cnt_8_en=1; end
            downcnt_8_bit : begin ns = cout ? Init : downcnt_8_bit; load_8bit=0;cnt_8_en = cout ? 0:1; end
            default: ns = Init;
        endcase
    end
    always @(posedge clk,posedge rst) begin
        if(rst)
            ps <= Init;
        else
            ps <= ns;
    end
endmodule
```

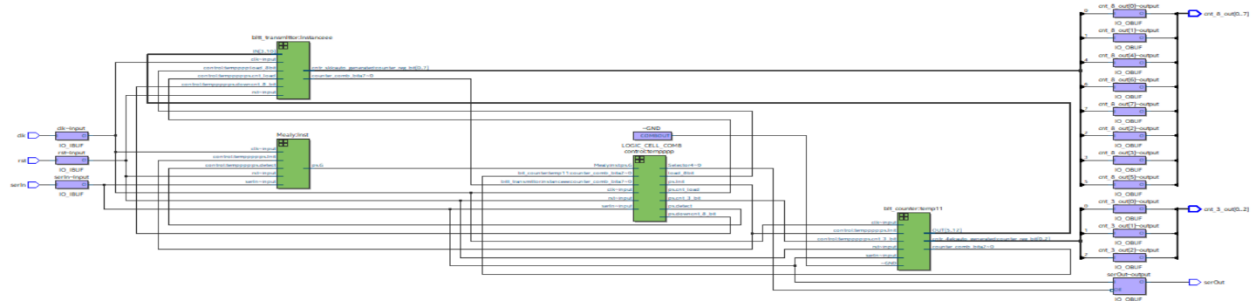
Part d:

i.

Symbols using RTL Viewer and Technology Map viewer:



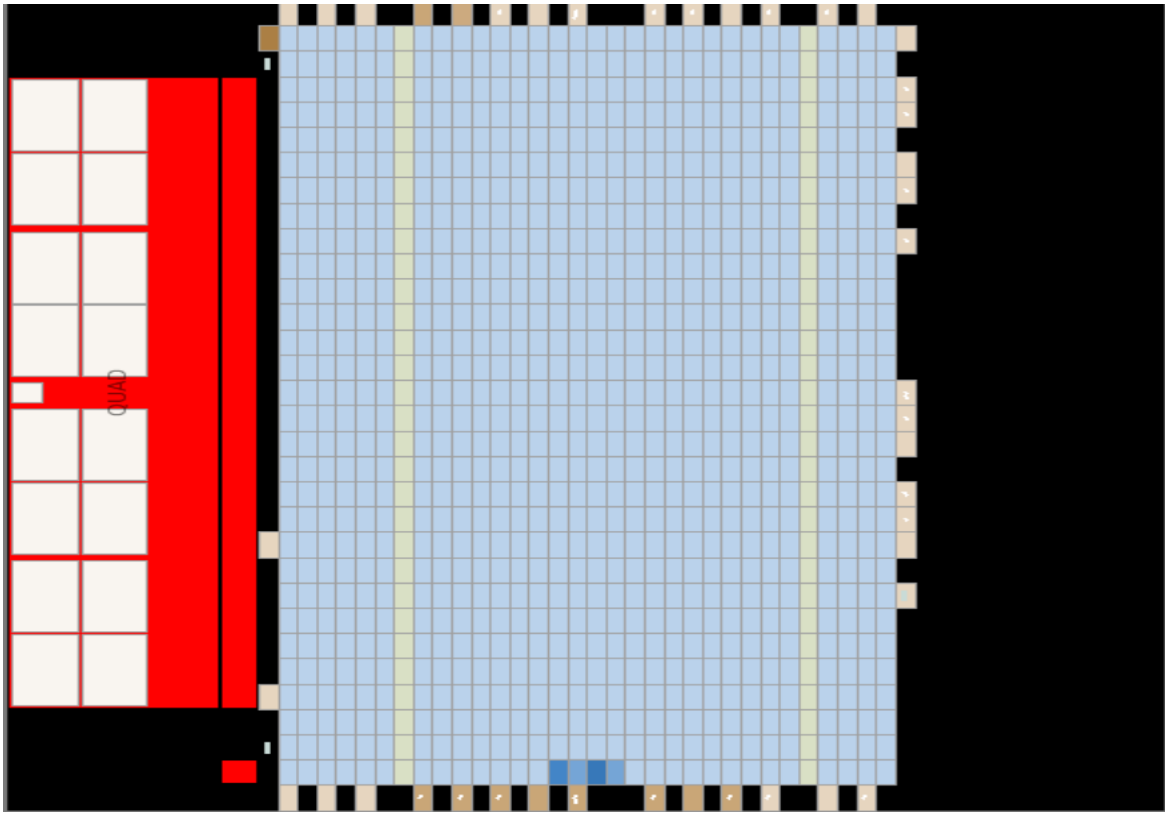




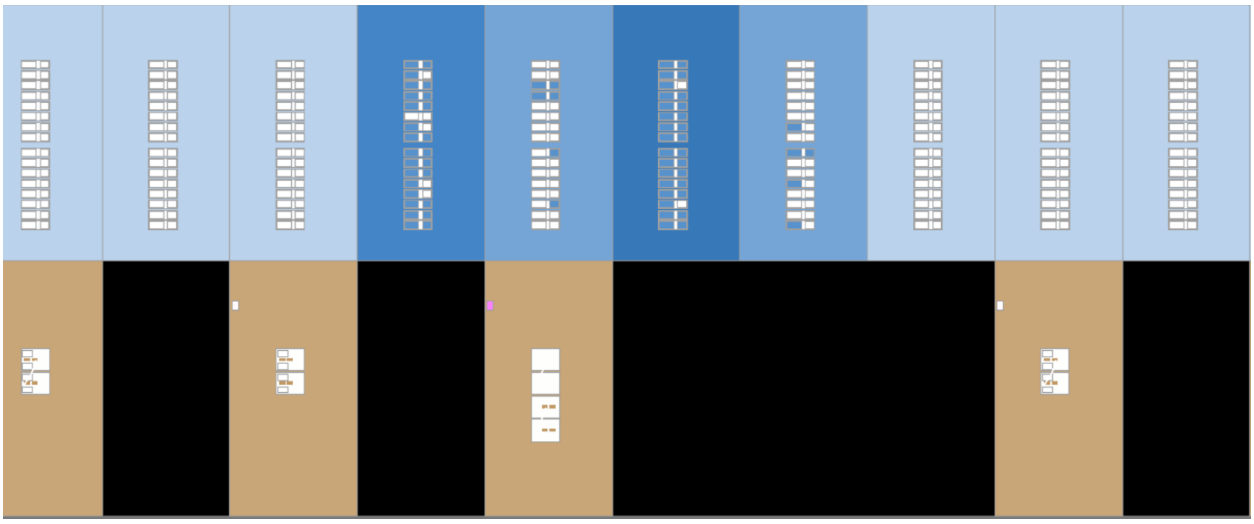
Resources used for building the curcuit(after synthesis):

Flow Status	Successful - Sun Dec 31 21:29:29 2023
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	nt_collector
Top-level Entity Name	nt_collector
Family	Cyclone IV GX
Device	EP4CGX15BF14A7
Timing Models	Final
Total logic elements	39 / 14,400 (< 1 %)
Total registers	30
Total pins	15 / 81 (19 %)
Total virtual pins	0
Total memory bits	0 / 552,960 (0 %)
Embedded Multiplier 9-bit elements	0
Total GXB Receiver Channel PCS	0 / 2 (0 %)
Total GXB Receiver Channel PMA	0 / 2 (0 %)
Total GXB Transmitter Channel PCS	0 / 2 (0 %)
Total GXB Transmitter Channel PMA	0 / 2 (0 %)
Total PLLs	0 / 3 (0 %)

Floor plan:



Four logic blocks is used for building the logic of this circuit.



As we can see, we have 4 logic blocks that we can see their number of logic elements of them.

ii.

Testbench:

```
`timescale 1ns/1ns
module final_tb();
    reg serin=0, clk=0, rst=0;
    wire [2:0] cnt_3_out;
    wire [7:0] cnt_8_out;
    wire serOut;
    nt_collector UUT5(serOut,clk,rst,serin,cnt_3_out,cnt_8_out);
    initial forever begin #41;clk=~clk; end
    initial begin
    #82;
        #20;
        #82; serin=0;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1;
        #82; serin=0;
        #82; serin=1;
        #82; serin=1;
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        #82; serin=0;
        #82; serin=0;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1;
        #82; serin=1;
        #100
        $stop;
    end
endmodule
```

Result of the testbench: