In the Name of God

Faculty of Electrical Engineering

Electronics 2
Second Semester 22-23
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1 Transistor Simulation

1.1 NPN

I_c	1μ	10μ	100μ	$1m$	$10m$
$V_{BE}(on)$	$0.476v$	$0.535v$	$0.595v$	$0.654v$	$0.716v$
$V_{CE}(sat)$	$10mv$	$44mv$	$99mv$	$186mv$	$281mv$

1.2 PNP

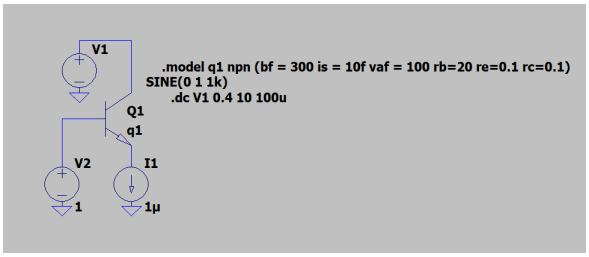
I_c	1μ	10μ	100μ	$1m$	$10m$
$V_{BE}(on)$	$-0.476v$	$-0.535v$	$-0.595v$	$-0.654v$	$-0.715v$
$V_{CE}(sat)$	$-22mv$	$-44mv$	$-99mv$	$-187mv$	$-219mv$

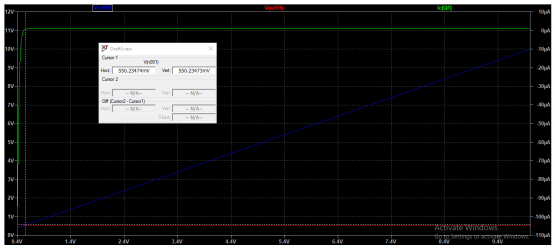
1.3 Calculating $V_{BE}(on)$

Based on the image below, to calculate the base emitter voltage in the on state of the circuit, only op space simulation is used.

1.4 Calculating $V_{CE}(sat)$

To calculate the value of saturation voltage, first we use a bias of the transistor as follows, then by plotting the current curve, we can read the saturation point by finding the values of the collector and emitter voltages.





2 Amplifier

2.1 Amplifier Circuit

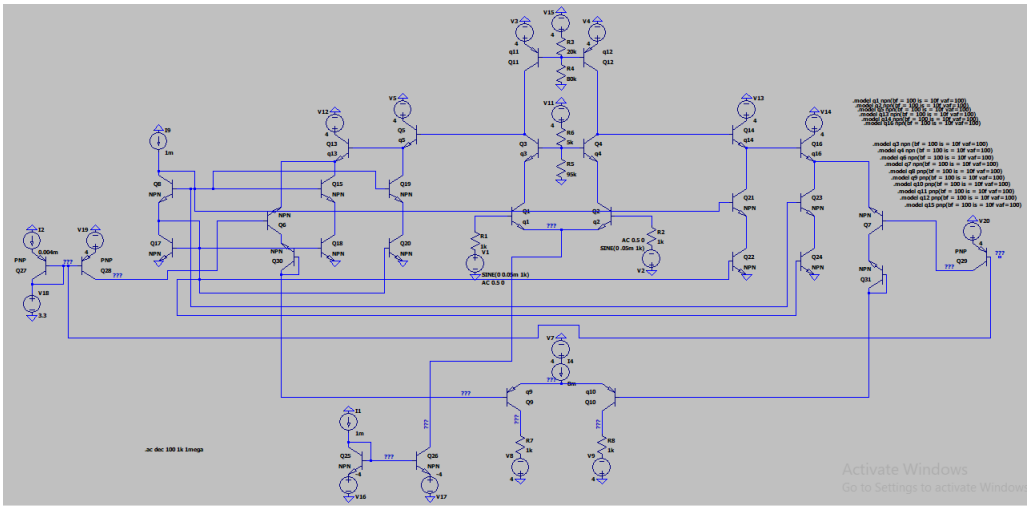


Figure 1: Circuit Illustration

2.2 Gain Stages

First, we generate a considerable amount of gain using a differential stage. It should be noted that instead of resistors, we should use a pnp transistor stage at the output of the second stage to increase the output resistance. This stage has a constant CMR value ranging from -4 to 2.9. Then, due to the low output resistance of this stage, a buffer is used. However, because this buffer also experiences low output resistance in its emitter, it has low gain. Therefore, another buffer is used to increase the resistance. But using two buffers in succession drastically reduces our gain, so we use a bias in the base path to increase the gain. Ultimately, using a shift level is connected to the output stage to adjust the output swing, and the gain and output swing values are obtained with the help of SPICE.

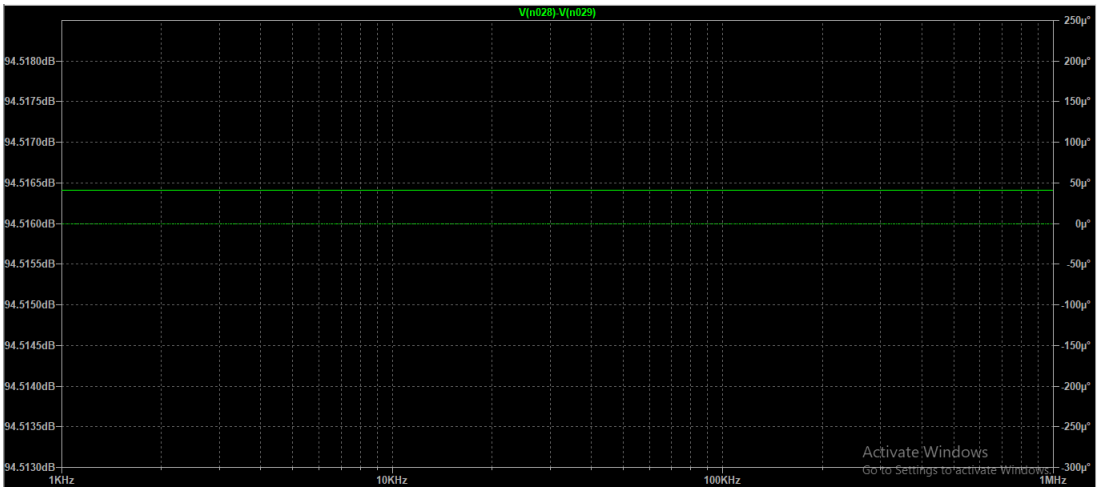


Figure 2: Differential Amplification with $99.4dB$ gain

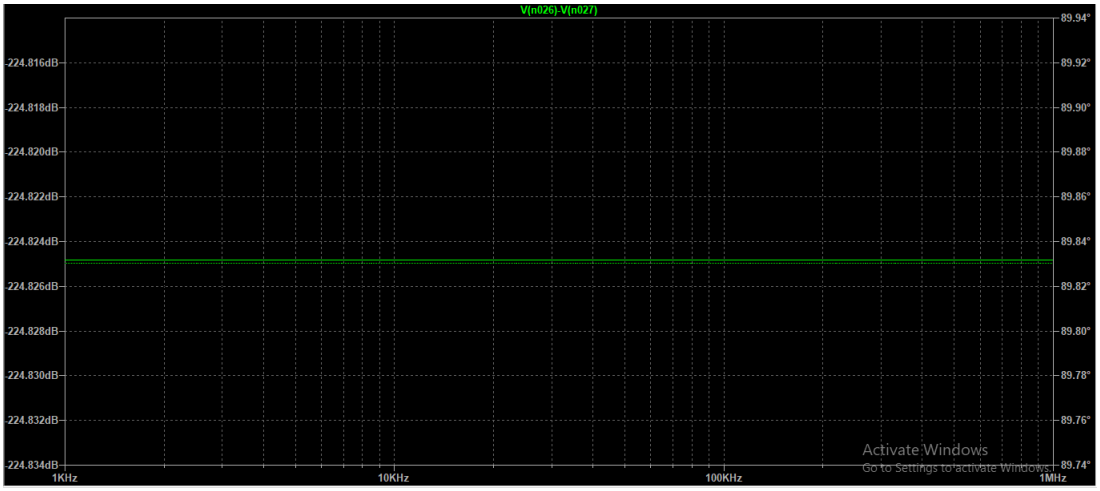


Figure 3: Common Mode Amplification with $-224dB$ gain

2.3 Swing

In order to achieve a swing greater than $6V$, we need to adjust the output stage current to $4mA$, so that at zero input, the output provides a swing close to 4 and -4 volts.

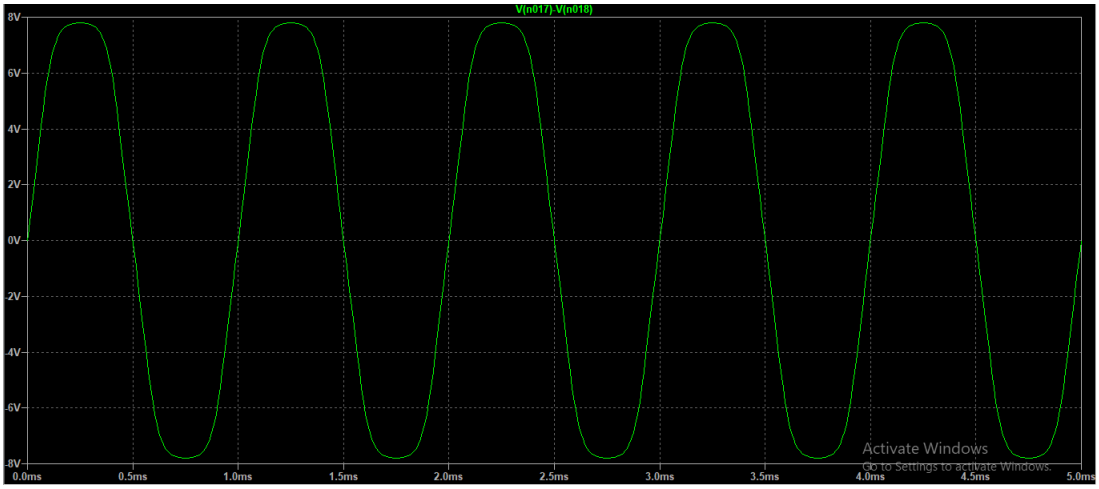


Figure 4: Swing $7.5V$

2.4 Power

The power required by the problem is met.

The power value obtained in the image below is the generated power, and its negative value shows the circuit's consumed power.

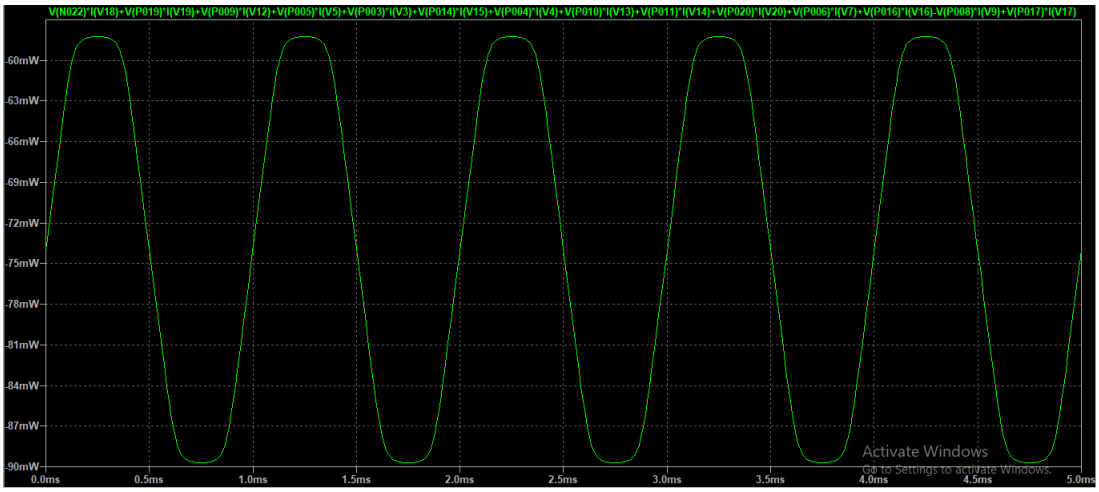


Figure 5: power(max) = 90mw

2.5 CMR

Due to the limited saturation voltages of the transistors and diodes available, the input CMR value may range from -3.8 to 2.7, which satisfactorily meets the input requirement.

2.6 CMRR

The CMRR value is $256dB$.

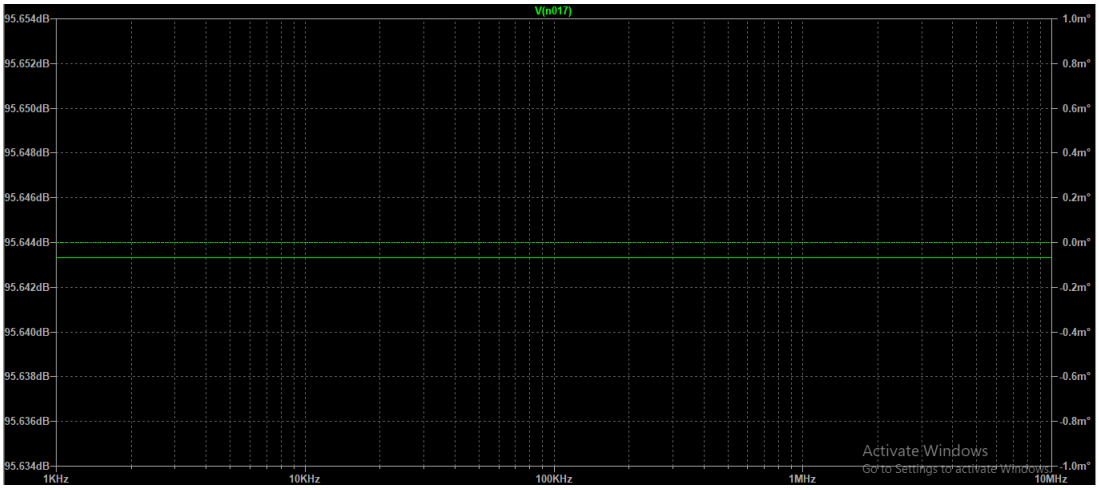


Figure 6: Single-ended Differential Output

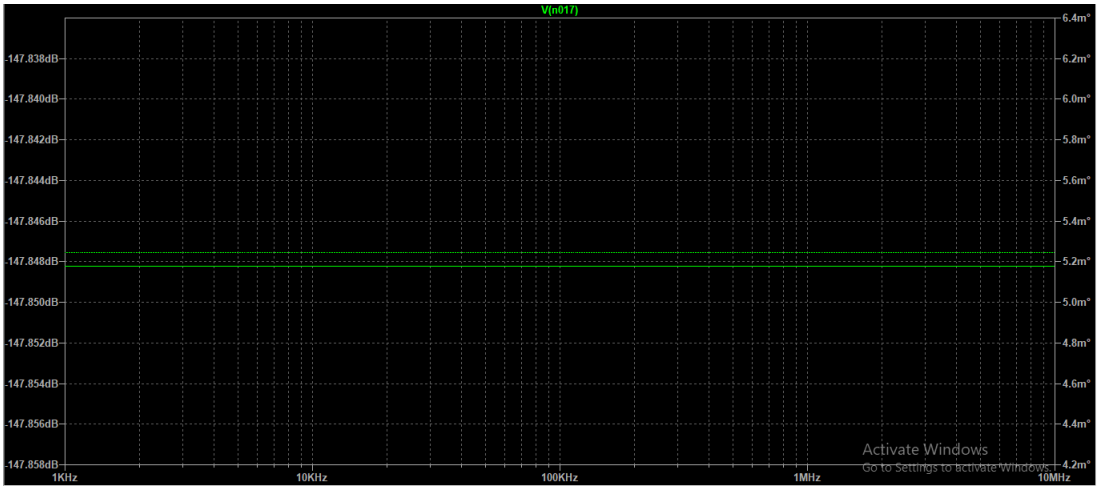


Figure 7: Single-ended Output with Common Mode

3 THD

Using SPICE Fourier analysis, we plot the THD of the circuit for a swing of 5 volts.

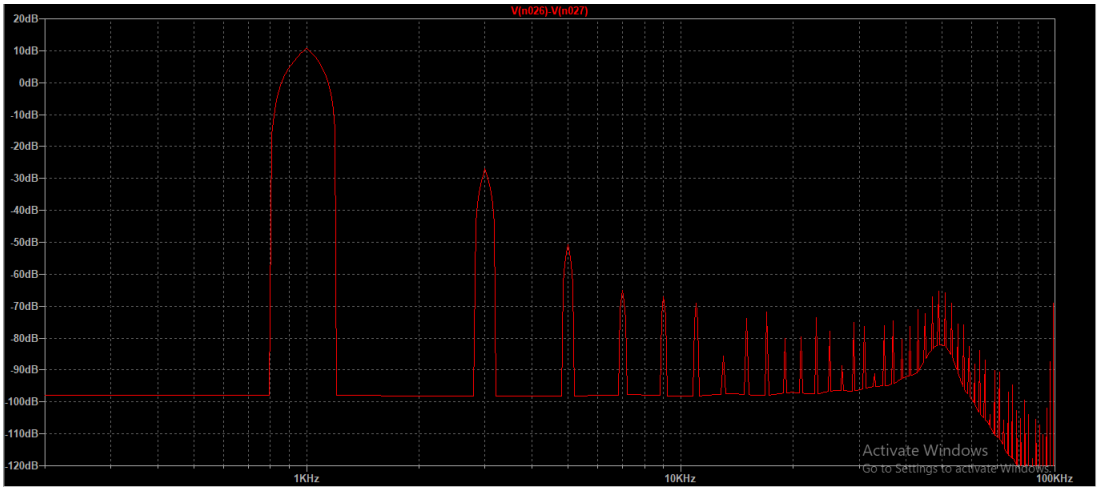

V(n026)-V(n027)
20dB
10dB
0dB
-10dB
-20dB
-30dB
-40dB
-50dB
-60dB
-70dB
-80dB
-90dB
-100dB
-110dB
-120dB
1KHz
10KHz
100KHz
Activate Windows
Go to Settings to activate Windows.

Figure 8: THD