

Q1_Module Project Status (04/06/2024 - 20:40:09)			
Project File:	IP_Core.xise	Parser Errors:	No Errors
Module Name:	Q1_Module	Implementation State:	Placed and Routed
Target Device:	xc7a100t-1csg324	• Errors:	No Errors
Product Version:	ISE 14.7	• Warnings:	111 Warnings (1 new)
Design Goal:	Balanced	• Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	All Constraints Met
Environment:	System Settings	• Final Timing Score:	0 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	450	126,800	1%	
Number used as Flip Flops	450			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	391	63,400	1%	
Number used as logic	334	63,400	1%	
Number using O6 output only	170			
Number using O5 output only	7			
Number using O5 and O6	157			
Number used as ROM	0			
Number used as Memory	38	19,000	1%	
Number used as Dual Port RAM	0			
Number used as Single Port RAM	0			
Number used as Shift Register	38			
Number using O6 output only	38			
Number using O5 output only	0			
Number using O5 and O6	0			
Number used exclusively as route-thrus	19			
Number with same-slice register load	19			
Number with same-slice carry load	0			

Number with other load	0			
Number of occupied Slices	167	15,850	1%	
Number of LUT Flip Flop pairs used	477			
Number with an unused Flip Flop	119	477	24%	
Number with an unused LUT	86	477	18%	
Number of fully used LUT-FF pairs	272	477	57%	
Number of unique control sets	3			
Number of slice register sites lost to control set restrictions	8	126,800	1%	
Number of bonded IOBs	106	210	50%	
IOB Latches	2			
Number of RAMB36E1/FIFO36E1s	0	135	0%	
Number of RAMB18E1/FIFO18E1s	0	270	0%	
Number of BUFG/BUFGCTRLs	1	32	3%	
Number used as BUFGs	1			
Number used as BUFGCTRLs	0			
Number of IDELAYE2/IDELAYE2_FINEDELAYs	0	300	0%	
Number of ILOGICE2/ILOGICE3/ISERDESE2s	0	300	0%	
Number of ODELAYE2/ODELAYE2_FINEDELAYs	0			
Number of OLOGICE2/OLOGICE3/OSERDESE2s	2	300	1%	
Number used as OLOGICE2s	2			
Number used as OLOGICE3s	0			
Number used as OSERDESE2s	0			
Number of PHASER_IN/PHASER_IN_PHYs	0	24	0%	
Number of PHASER_OUT/PHASER_OUT_PHYs	0	24	0%	
Number of BSCANs	0	4	0%	
Number of BUFHCEs	0	96	0%	
Number of BUFRs	0	24	0%	
Number of CAPTUREs	0	1	0%	
Number of DNA_PORTs	0	1	0%	
Number of DSP48E1s	4	240	1%	
Number of EFUSE_USRs	0	1	0%	
Number of FRAME_ECCs	0	1	0%	
Number of IBUFDS_GTE2s	0	4	0%	
Number of ICAPs	0	2	0%	

Number of IDELAYCTRLs	0	6	0%	
Number of IN_FIFOs	0	24	0%	
Number of MMCME2_ADVs	0	6	0%	
Number of OUT_FIFOs	0	24	0%	
Number of PCIE_2_1s	0	1	0%	
Number of PHASER_REFs	0	6	0%	
Number of PHY_CONTROLS	0	6	0%	
Number of PLLE2_ADVs	0	6	0%	
Number of STARTUPs	0	1	0%	
Number of XADCs	0	1	0%	
Number of RPM macros	1			
Average Fanout of Non-Clock Nets	2.22			

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0, Component Switching Limit: 0)	Pinout Data:	Pinout Report	
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report	
Timing Constraints:	All Constraints Met			

Detailed Reports						[-]
Report Name	Status	Generated	Errors	Warnings	Infos	
Synthesis Report	Current	Sat Apr 6 20:23:55 2024	0	3 Warnings (1 new)	3 Infos (2 new)	
Translation Report	Current	Sat Apr 6 20:38:45 2024	0	0	0	
Map Report	Current	Sat Apr 6 20:39:33 2024	0	108 Warnings (0 new)	7 Infos (0 new)	
Place and Route Report	Current	Sat Apr 6 20:39:54 2024	0	0	0	
Power Report						
Post-PAR Static Timing Report	Current	Sat Apr 6 20:40:07 2024	0	0	3 Infos (0 new)	
Bitgen Report						

Secondary Reports			[-]
Report Name	Status	Generated	

ISIM Simulator Log

Out of Date

Sat Apr 6 05:58:41 2024

Date Generated: 04/06/2024 - 20:40:09