EE25266 – ASIC/FPGA Chip Design

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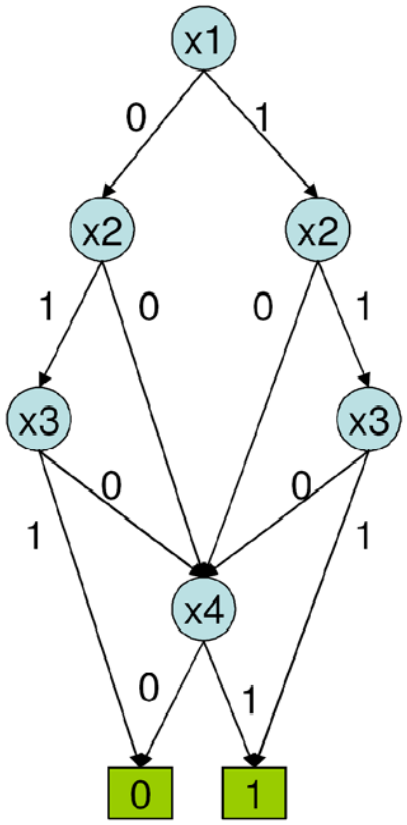
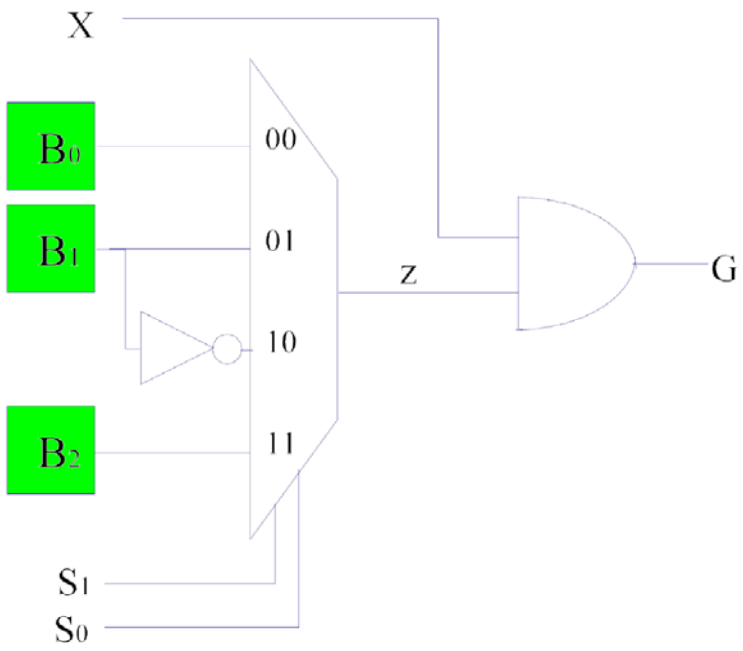
Assignment #6 - Spring 2024

1 - For the following Reduced Ordered BDD (ROBDD) find the best variable ordering you can and show the resulting ROBDD. Look at different representations of the logic function this ROBDD represents to gain insight into which variable ordering produces the smallest graph. Show your work, but do not provide BDDs for all 24 possible variable ordering sequences.



2- Consider the following logic structure:



The characteristic equation for this structure is:

$$F = \left(B_0 + S_1 + S_0 + \overline{z}\right)\left(\overline{B}_0 + S_1 + S_0 + z\right)\left(B_1 + S_1 + \overline{S}_0 + \overline{z}\right)\left(\overline{B}_1 + S_1 + \overline{S}_0 + z\right)$$
$$\left(\overline{B}_1 + \overline{S}_1 + S_0 + \overline{z}\right)\left(B_1 + \overline{S}_1 + S_0 + z\right)\left(B_2 + \overline{S}_1 + \overline{S}_0 + \overline{z}\right)\left(\overline{B}_2 + \overline{S}_1 + \overline{S}_0 + z\right)$$
$$\left(\overline{x} + \overline{z} + G\right)\left(z + \overline{G}\right)\left(x + \overline{G}\right)$$

Suppose you were to use a SAT solver to identify which of the following functions can be mapped into the above structure. Indicate which functions would be mapped successfully, and for those that do not identify the clauses that cause a conflict.

i) $f = XS_1S_0 + XS_1\underline{S}_0 + X\underline{S}_1\underline{S}_0$

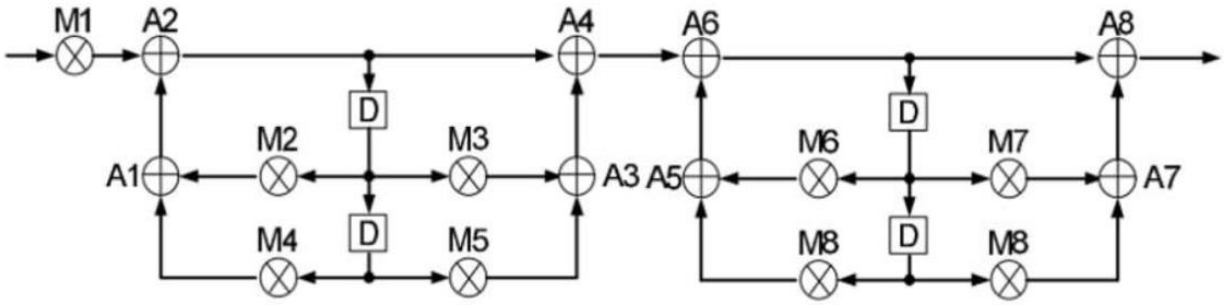
ii) $f = XS_1S_0$

3- Consider the following function:

$$f = \sum m(0, 1, 2, 3, 4, 6, 8, 10, 11, 15)$$

a) Implement the following function as an ROBDD. The resulting BDD should be as compact as possible.
b) Optimize its final logical representation using Quine-McCluskey method.

4- Consider the circuit below which is a 4th order IIR-filter made by placing two 2nd order IIR-filters in series. Suppose each multiplier has a delay of two nanoseconds and each adder has a delay of one nanosecond.



1- Show the critical path and calculate the maximum clock frequency in this circuit.
2- Change the circuit using pipeline and retiming methods in such a way that the minimum critical path delay is achieved and calculate the maximum clock frequency in the new circuit.