

FIR_Filter_Resource_Share Project Status (05/06/2024 - 22:30:44)			
Project File:	cccc.xise	Parser Errors:	No Errors
Module Name:	FIR_Filter_Resource_Share	Implementation State:	Placed and Routed
Target Device:	xc7a100t-1csg324	• Errors:	No Errors
Product Version:	ISE 14.7	• Warnings:	50 Warnings (50 new)
Design Goal:	Balanced	• Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	All Constraints Met
Environment:	System Settings	• Final Timing Score:	0 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	214	126,800	1%	
Number used as Flip Flops	214			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	189	63,400	1%	
Number used as logic	174	63,400	1%	
Number using O6 output only	163			
Number using O5 output only	0			
Number using O5 and O6	11			
Number used as ROM	0			
Number used as Memory	0	19,000	0%	
Number used exclusively as route-thrus	15			
Number with same-slice register load	15			
Number with same-slice carry load	0			
Number with other load	0			
Number of occupied Slices	74	15,850	1%	
Number of LUT Flip Flop pairs used	249			
Number with an unused Flip Flop	51	249	20%	
Number with an unused LUT	60	249	24%	
Number of fully used LUT-FF pairs	138	249	55%	

Number of unique control sets	4			
Number of slice register sites lost to control set restrictions	10	126,800	1%	
Number of bonded IOBs	48	210	22%	
Number of RAMB36E1/FIFO36E1s	0	135	0%	
Number of RAMB18E1/FIFO18E1s	0	270	0%	
Number of BUFG/BUFGCTRLs	1	32	3%	
Number used as BUFGs	1			
Number used as BUFGCTRLs	0			
Number of IDELAYE2/IDELAYE2_FINEDELAYs	0	300	0%	
Number of ILOGICE2/ILOGICE3/ISERDESE2s	0	300	0%	
Number of ODELAYE2/ODELAYE2_FINEDELAYs	0			
Number of OLOGICE2/OLOGICE3/OSERDESE2s	0	300	0%	
Number of PHASER_IN/PHASER_IN_PHYs	0	24	0%	
Number of PHASER_OUT/PHASER_OUT_PHYs	0	24	0%	
Number of BSCANs	0	4	0%	
Number of BUFHCEs	0	96	0%	
Number of BUFRs	0	24	0%	
Number of CAPTUREs	0	1	0%	
Number of DNA_PORTs	0	1	0%	
Number of DSP48E1s	1	240	1%	
Number of EFUSE_USRs	0	1	0%	
Number of FRAME_ECCs	0	1	0%	
Number of IBUFDS_GTE2s	0	4	0%	
Number of ICAPs	0	2	0%	
Number of IDELAYCTRLs	0	6	0%	
Number of IN_FIFOs	0	24	0%	
Number of MMCME2_ADVs	0	6	0%	
Number of OUT_FIFOs	0	24	0%	
Number of PCIE_2_1s	0	1	0%	
Number of PHASER_REFs	0	6	0%	
Number of PHY_CONTROLS	0	6	0%	
Number of PLLE2_ADVs	0	6	0%	
Number of STARTUPs	0	1	0%	
Number of XADCs	0	1	0%	

Average Fanout of Non-Clock Nets	5.08		
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Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	Pinout Data:	Pinout Report	
Routing Results:	All Signals Completely Routed	Clock Data:	Clock Report	
Timing Constraints:	All Constraints Met			

Detailed Reports						[-]
Report Name	Status	Generated	Errors	Warnings	Infos	
Synthesis Report	Current	Mon May 6 22:28:44 2024	0	0	0	
Translation Report	Current	Mon May 6 22:28:55 2024	0	0	0	
Map Report	Current	Mon May 6 22:29:45 2024	0	50 Warnings (50 new)	5 Infos (5 new)	
Place and Route Report	Current	Mon May 6 22:30:20 2024	0	0	3 Infos (3 new)	
Power Report						
Post-PAR Static Timing Report	Current	Mon May 6 22:30:42 2024	0	0	4 Infos (4 new)	
Bitgen Report						

Secondary Reports			[-]
Report Name	Status	Generated	

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