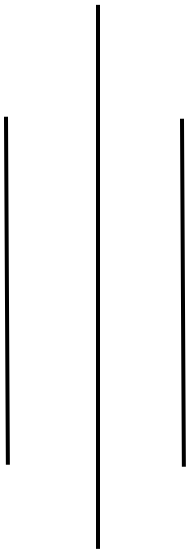
SHAID SMARAK COLLEGE

Kirtipur, Kathmandu



Lab no: 4 of Digital logics

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1st semester

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LAB 4: DECODER

Objective:

- To implement a full adder circuit with a decoder.

Discussion:

Discrete quantities of information are represented in digital system with binary code. A binary code of n bits is capable of representing up to 2^n distinct elements of the coded information.

Decoder:

It is a combinational circuit that converts binary information from n inputs lines to a maximum of 2^n unique output lines. It the n-bit decoded information has unused or don't care combination, the decoder output will have fewer than 2^n outputs. The n-to-m line decoders have $m<=2^n$.

X	Y	Z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Table: *Truth table of 3 to 8 decoder*.

- **Combinational Logic Implementation**
  1. A decoder provides the 2^n minterms of n input variables. Since any Boolean function can be expressed in SOP canonical form, one can use a decoder to generate the minterms and an external OR gate to form the sum.
  2. Any combinational circuit with n input and m output can be implemented with an n-to-2^n line decoder and m OR gate.
  3. Boolean function of the decoder implemented circuit are expressed in SOP. This form can be easily obtained from the truth table or by expanding the functions to their sum of minterms.

Example: - 3-to 8-line decoder

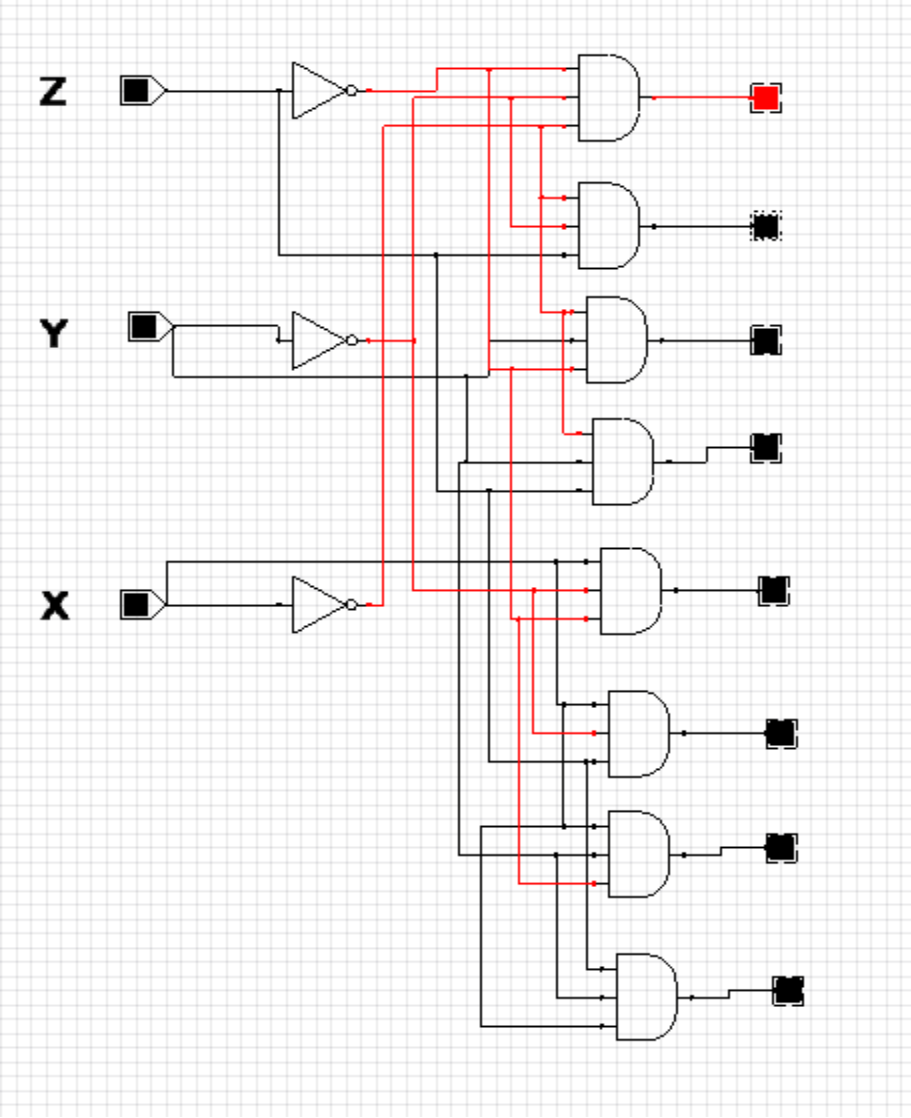

Fig: 3-to-8-line decoder.

The above figure represents that the 3 inputs are decoded into 8 outputs, each output represents one of the minterms.

Question: - Implement a full adder circuit with a decoder

From the truth table of the full adder:

$$S\ (X, Y, Z) = \sum (1, 2, 4, 7)$$

$$C\ (X, Y, Z) = \sum (3, 5, 6, 7)$$

Since, there are 3 inputs and a total of 8 outputs we need 3-to-8-line decoder.

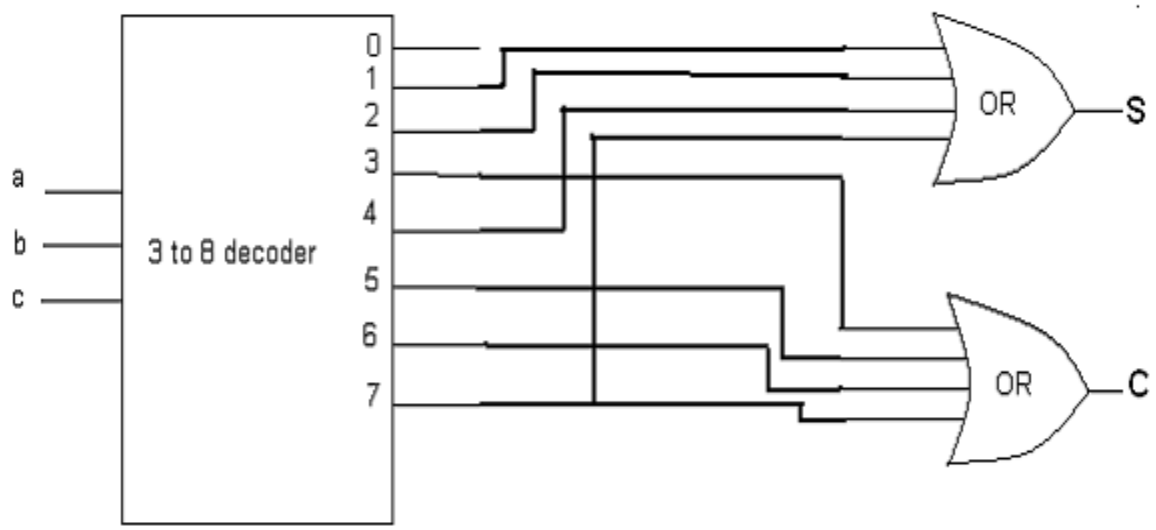

Fig: Implementation of full adder with decoder.