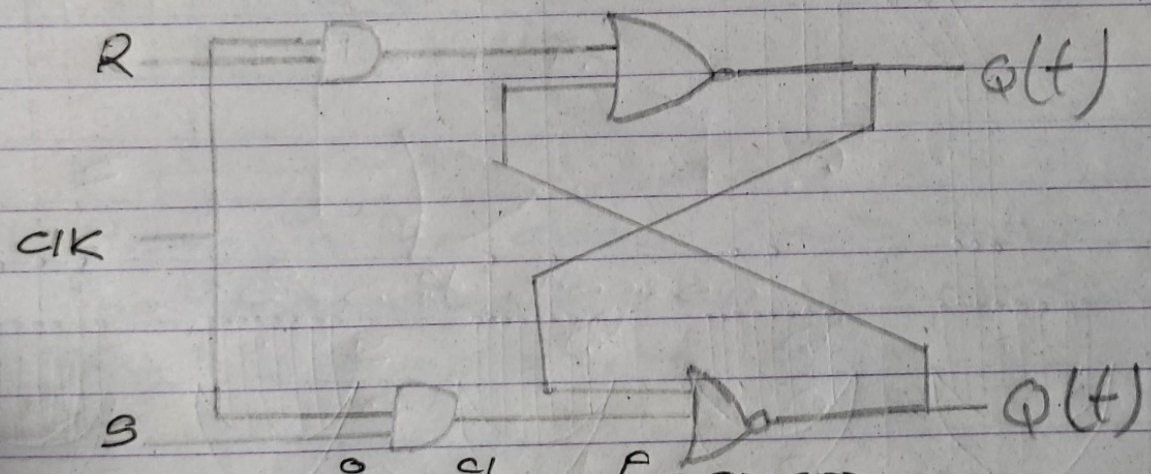
Assignment → 6

x) Describe the concept of flip flop with a circuit diagram & characteristic table. How RS flip flop is different from SR flip flop. Explain with circuit diagram.

↳ A flip ~~fff~~ flop is a device which stores a single bit of data; one of its two states represents a "One" & the other represents a "zero". Such data storage can be used for storage of state & such a circuit is described as sequential logic in electronics.



Circuit diagram

If two ~~NAND~~ NOR gates & the input of both the gates is connected to ~~the~~ different output It is connected in a way that both the inputs are interlocked with one another. So, it basically produces a toggle action & work on it.

S	R	Q_n
0	1	0
0	1	1
1	0	0
1	0	1

clock	R	S	Q	state
↓ or 0 or ⊥	x	x	last state	Hold
↑	0	0	11	Hold
↑	0	1	1	set
↑	1	0	0	Reset
↑	1	1	?	Forbidden

The above figure suggest a RS flip-flop, the functionality of SET & RESET remain the same i.e. when S is high, Q is set to 1 & when R is high Q is reset to 0.

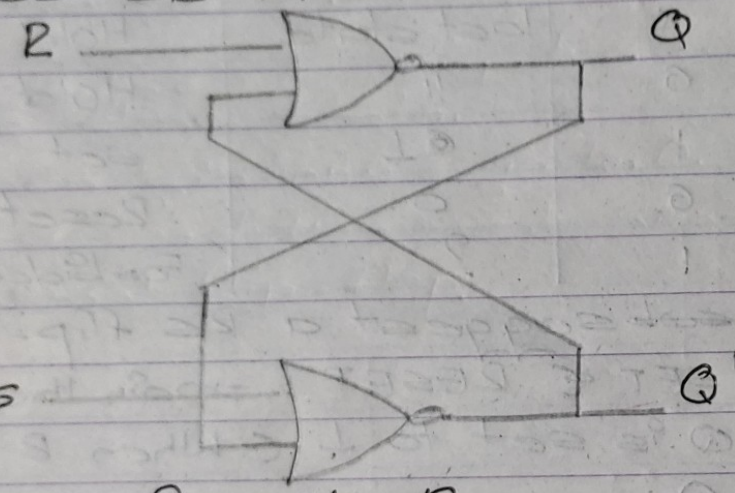
There are a total of 4 types of flip-flops which are mentioned below:

1. SR flip-flop
2. D flip-flop
3. JK flip-flop
4. T flip-flop

x) How is RS flip-flop different from SR flip-flop? Explain with diagram.

↳ The common difference is that, in SR latch NOR gates are used & in RS latch NAND gates are used. The output also differ from one another.

- For SR latch



Circuit diagram

S	R	Q	Q'
1	0	1	0
0	0	1	0
0	1	0	1
0	0	0	1
1	1	0	0

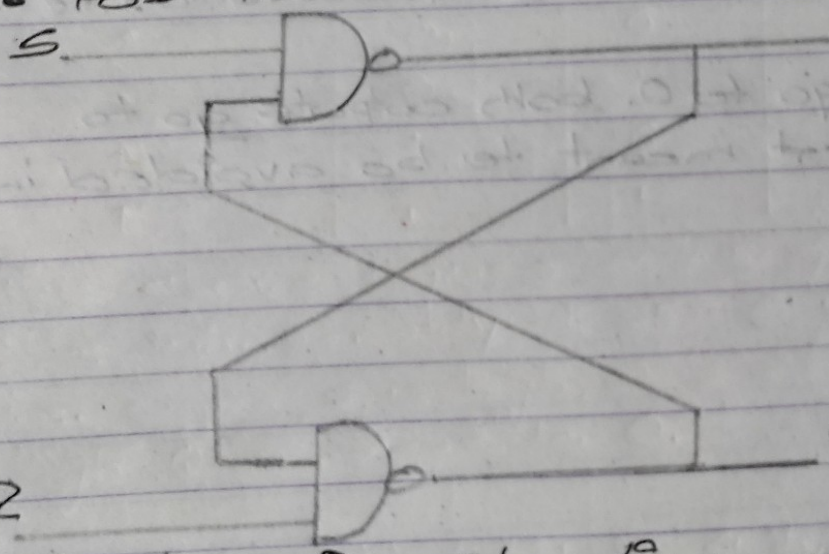
When, $S=1$, $R=0$, $Q=0$ & $Q'=1$

When, $S=0$, $R=0$, $Q=0$ & $Q'=1$

When 1 in reset input changes Q to 0 & Q' to. So, here the actuan input actuans to 0, the outputs do not change.

When a 1 is applied to both ~~sides~~ set & the reset inputs, both Q & Q' outputs go to 0. This condition violates the fact that output Q & Q' are the complements of each other. In normal ~~conditions~~ operation, this operation must be avoided by making sure that not 1's are applied.

- For RS latch.



circuit diagram

S	R	Q	Q'
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	1	1

→ The NAND basic flip-flop circuit operates with both inputs normally at 1 unless the state of the flip flop has to be changed.
→ The application of a momentary 0 to the set input causes output Q to go to 1 & Q' to go to 0, thus putting the flip-flop in to set state.
→ After the set input returns to 1, a momentary 0 to the reset input causes a transition to the clear state.
→ When both inputs go to 0. both outputs go to 1, a condition ~~not~~ meant to be avoided in normal flip-flop.