

The number 526 that can be seen in the picture above is related to a number of gates before minimizing the circuit and using simple circuit logic and Regardless of the minimum hardware.

The waveform related to the first circuit before and after Synthesize can be seen above.

```
C:\windows\system32\cmd.exe
2.23. Printing statistics.

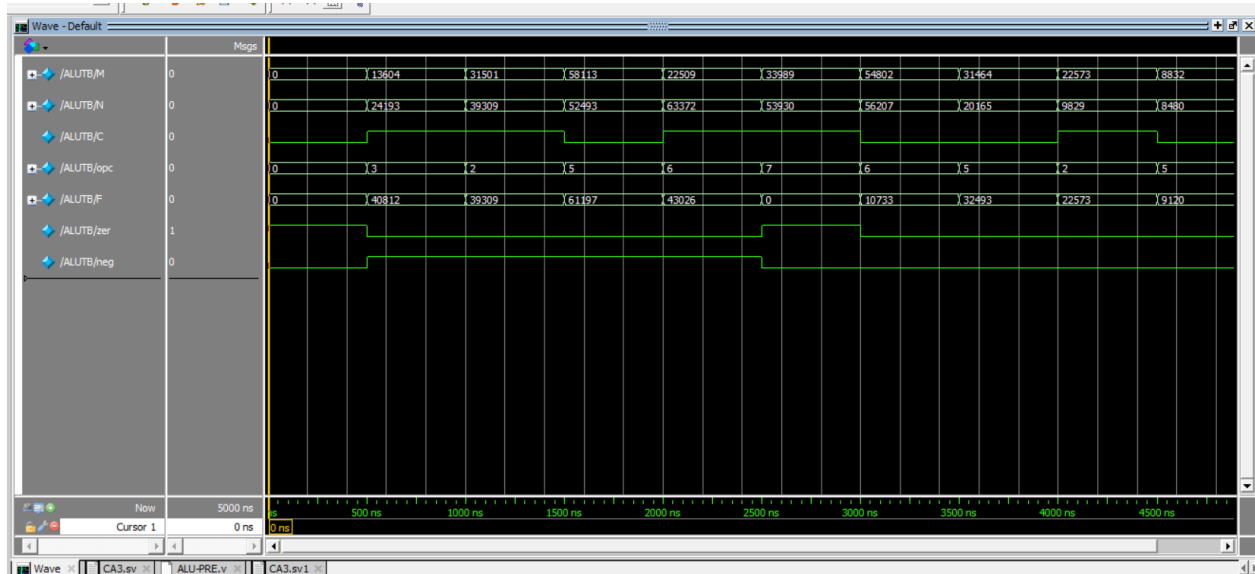
=== ALU ===

Number of wires:          516
Number of wire bits:      563
Number of public wires:   7
Number of public wire bits: 54
Number of memories:       0
Number of memory bits:    0
Number of processes:      0
Number of cells:          526

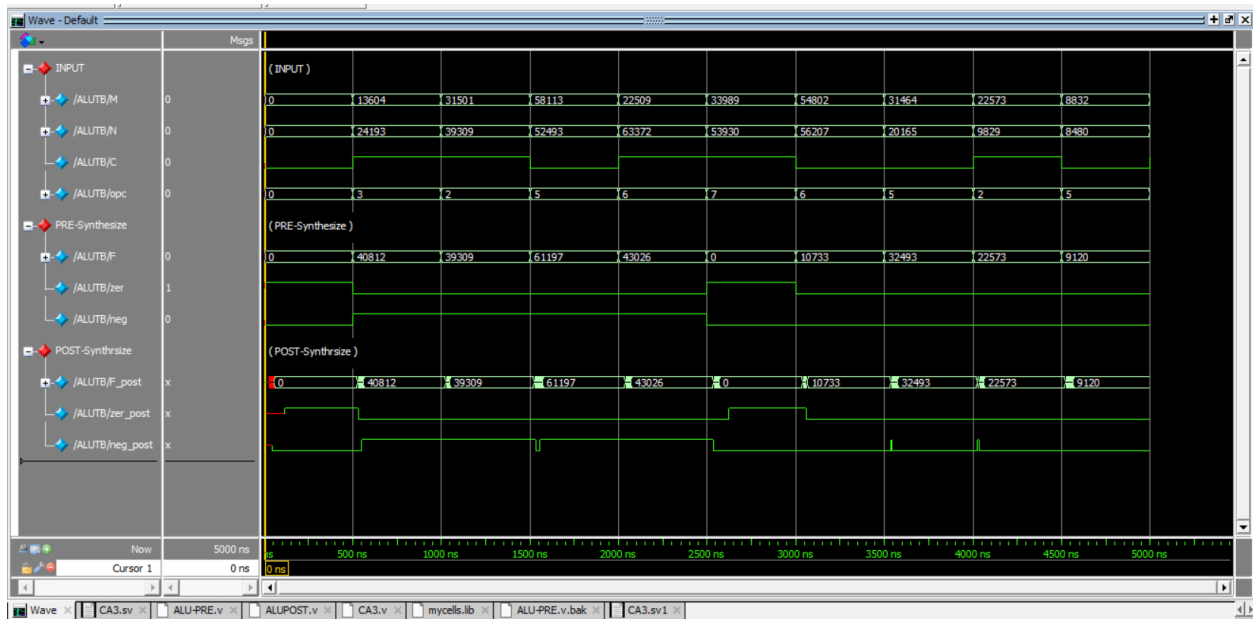
$.AND_          58
$.AOI3_         91
$.AOI4_          3
$.MUX_          16
$.NAND_         31
$.NOR_          85
$.NOT_          41
$.OAI3_         66
$.OAI4_         18
$.OR_           32
$.XNOR_         62
$.XOR_          31

2.24. Executing CHECK pass (checking for obvious problems).
checking module ALU..
found and reported 0 problems.

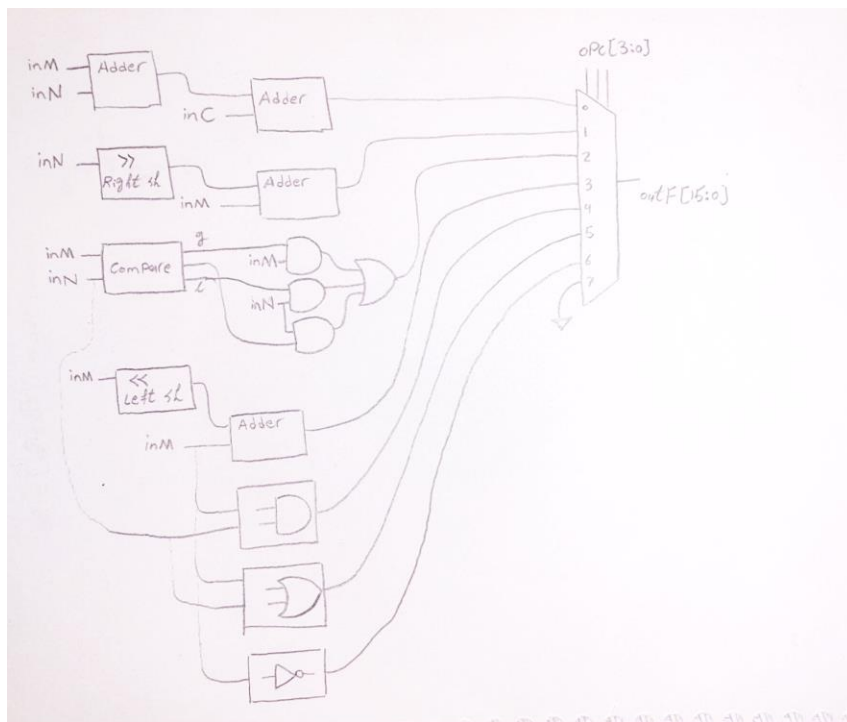
yosys> |
```



As you can see, after synthesizing the delay values change a bit and there is a reason for this delay is for the gates defined in the library.



Circuit built in part 1 - Too Many Adders so too many gates.



After combining all adders into one, we can see that number of cells shown in yosys is decreased to

```
C:\windows\system32\cmd.exe
3.21.4. Executing OPT_CLEAN pass (remove unused cells and wires).
Finding unused cells or wires in module \ALU_Post_Synth..
removing unused non-port wire \Mx.
removing unused non-port wire \adder.
removing unused non-port wire \incr.
removed 3 unused temporary wires.

3.21.5. Finished Fast OPT passes.

3.22. Executing HIERARCHY pass (managing design hierarchy).

3.22.1. Analyzing design hierarchy..
Top module: \ALU_Post_Synth

3.22.2. Analyzing design hierarchy..
Top module: \ALU_Post_Synth
Removed 0 unused modules.

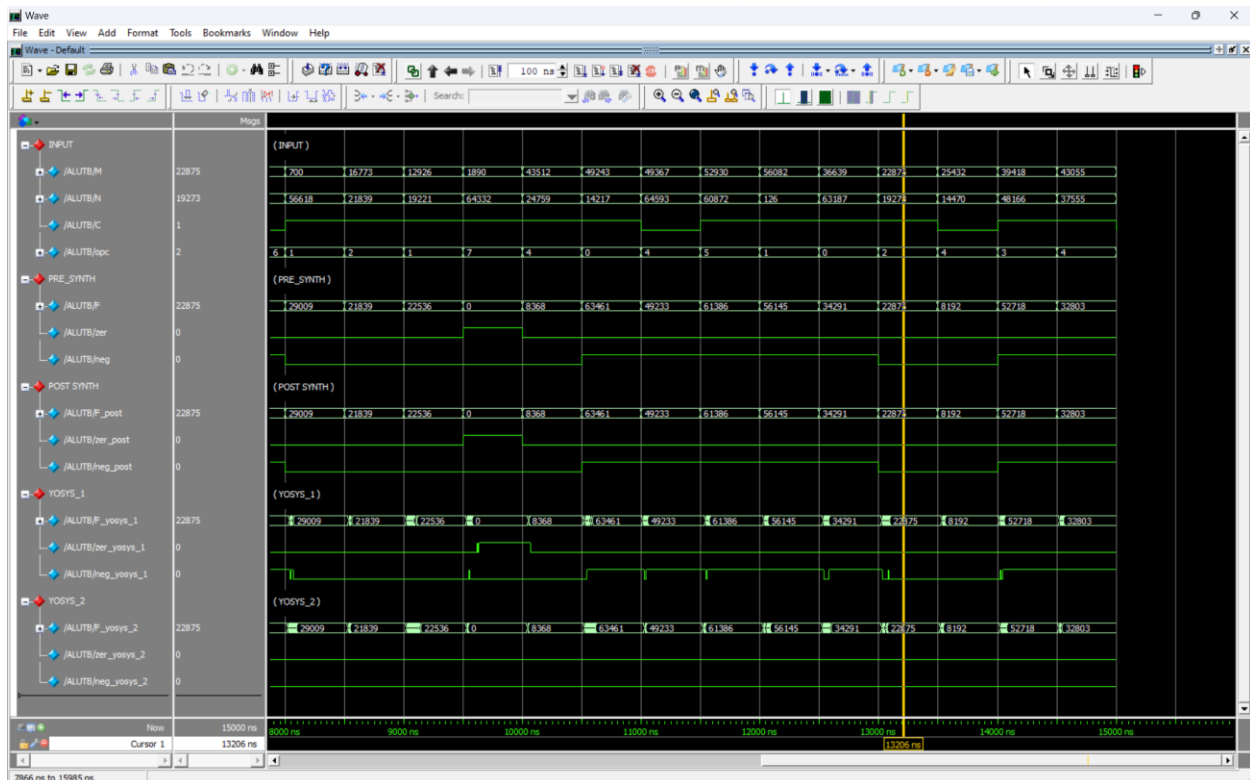
3.23. Printing statistics.

=== ALU_Post_Synth ===
Number of wires:      391
Number of wire bits:  467
Number of public wires: 9
Number of public wire bits: 85
Number of memories:   0
Number of memory bits: 0
Number of processes:  0
Number of cells:      398
$ _AND_                35
$ _AOI3_               36
$ _AOI4_                2
$ _MUX_                60
$ _NAND_               34
$ _NOR_                68
$ _NOT_                47
$ _OAI3_               37
$ _OAI4_               16
$ _OR_                 13
$ _XNOR_               43
$ _XOR_                7

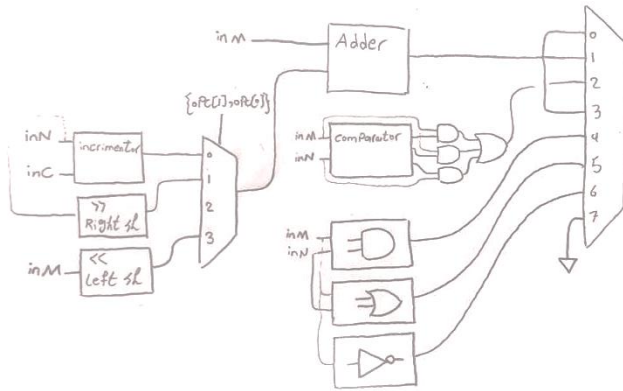
3.24. Executing CHECK pass (checking for obvious problems).
checking module ALU_Post_Synth..
found and reported 0 problems.

yosys> |
```

398. About 100 less than previous version.



After synthesizing the delay values increase and simulation speed decreases. The reason for this delay is for the gate delays defined in the library.



Bonus : simulation time before synthesizing : 328961 microseconds per iteration

Yosys : 538751 microseconds per iteration

simulation time after synthesizing : 283319 microseconds per iteration

Yosys : 287661 microseconds per iteration

In both situations simulation time for Yosys is more than mine because Yosys has a bigger file and more wires so simulation takes more time.