UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367, 1402-03
Computer Assignment 4
Flip-Flops, Registers, Shifters
Week 12

Name:
Date:

1. Write SystemVerilog description for a 4-bit register with active high asynchronous reset, rst, a clock-enable input, cen, rising edge clock, clk, and 4-bit parallel input and output.
   a. Write the description, develop a testbench for testing the register.
   b. Show functionality of asynchronous resetting and enabling and disabling the clock.

2. Using the register of Part 1, write a shifter module that shifts 4-bit data in eight shift stages. This unit has a 4-bit si[3:0] and a 4-bit so[3:0].
   a. Use **generate** statements to build this circuit. Tying the cen of the individual registers, forms a shift-enable, shn, input.
   b. Write a testbench to test this multi-bit shifter unit. Show that when shifting is enabled, a rising-edge of the clock moved a 4-bit data only one place to the right.

3. In a module, declare a two-dimensional array for shifting 4-bit data within the depth of the array. Using a clocked **always** statement write a shifter for shifting si[3:0] one place to the right within the array when shn is 1.
   a. Use a non-blocking assignment in a **for-loop** for performing this operation. Write a testbench to test this shifter circuit.
   b. Use a blocking assignment in a **for-loop** for performing this operation. Write a testbench to test this shifter circuit.
   c. Compare results of Part a and Pat b and explain the differences.

Deliverables:

- For all parts show the circuit, partial timing diagrams and the timings.
- For parts that you are examining the operation of the shift register, hand-draw the waveforms you are applying and the expected outputs.
- Be able to justify all timings of the simulation waveforms.

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastnameStudentnumber-CAnn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.