UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367 / Digital Systems I, ECE 894
Spring 1402-03
Computer Assignment 1
Basic Switch and Gate Structures in SystemVerilog
Week 3

Name:
Date:

1. Generate a 2-input CMOS NOR gate and verify its timing and functionality. Write the SystemVerilog description of this structure using NMOS and PMOS transistors. Use #(3, 4, 5) delay for the NMOS transistors and #(5, 6, 7) for the PMOS transistors. Generate a testbench for this circuit in SystemVerilog and examine it for various input changes. Among the various input changes, make sure you test the circuit for the worst-case delay of its output making To1 and To0 transitions. Make sure the time distance between your input changes is much larger than the gate delay values.

2. Generate a pass-transistor based 2-to-1 multiplexer using two NMOS transistors and an inverter (this uses an NMOS and a PMOS). Generate a testbench for this circuit in SystemVerilog and examine it for various input changes. Among the various input changes, make sure you test the circuit for the worst-case delay of its output making To1, To0, and ToZ transitions. Make sure the time distance between your input changes is much larger than the gate delay values.

3. Using NOR gates with as many inputs as needed based on that of Problem 1, generate a 4-to-1 MUX with two select inputs, *s1* and *s0*, and four data inputs *a*, *b*, *c*, and *d*. Deduce gate delays based on your findings of Problem 1. Generate a testbench for this circuit in SystemVerilog and examine it for various input changes. Among the various input changes, make sure you test the circuit for the worst-case delay of its output making To1 and To0. Make sure the time distance between your input changes is much larger than the gate delay values.

4. Using several 2-to-1 multiplexers of Problem 2, generate a 4-to-1 MUX with two select inputs, *s1* and *s0*, and four data inputs *a*, *b*, *c*, and *d*. Generate a testbench for this circuit in SystemVerilog and examine it for various input changes. Among the various input changes, make sure you test the circuit for the worst-case delay of its output making To1 and To0 transitions. Make sure the time distance between your input changes is much larger than the gate delay values.

5. In a testbench, instantiate the MUX circuits of Part 3 and Part 4 and compare the timing of these circuits. Explain the differences between these two circuits as far as the number of transistors and other physical parameters such as power consumption.

Deliverables:

Generate a report that includes item discussed below for each of the five parts of this CA.

A. Show the circuit diagram that you are analyzing. Show gates and/or transistors according to the specified delays.
B. Hand-simulate the circuit you have shown in Part A and write your expected values. For example, indicate what values you expect for the worst-case delays and express your reason for that.
C. Show your SystemVerilog description of the design you are simulating and the testbench for it. Best is to use the Snip tools to get the image from Notepad++. This way you see all keywords and indentations. Make sure your SV codes are properly indented and all line-up rules are followed.
D. Show an image of the project that you have created in ModelSim for the simulation of your circuit.
E. When simulation is complete, or even if you have a partial simulation, include an image of the output waveform showing signal names being displayed.

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastnameStudentnumber-CAn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.