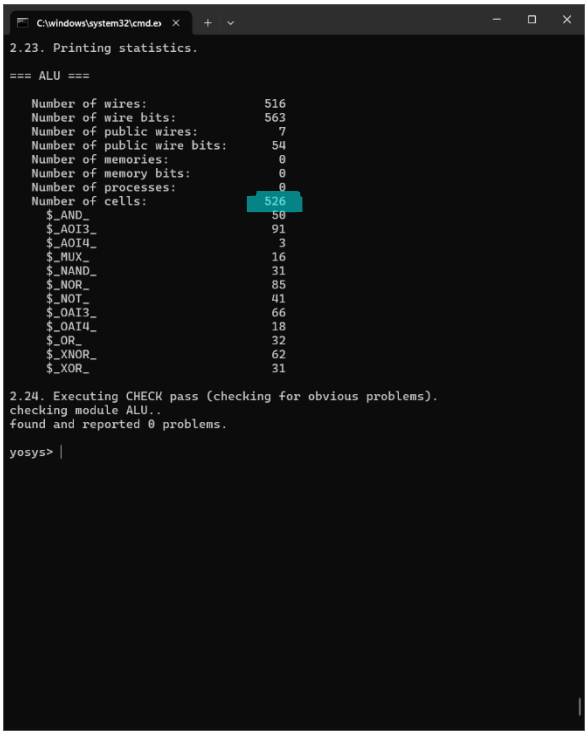
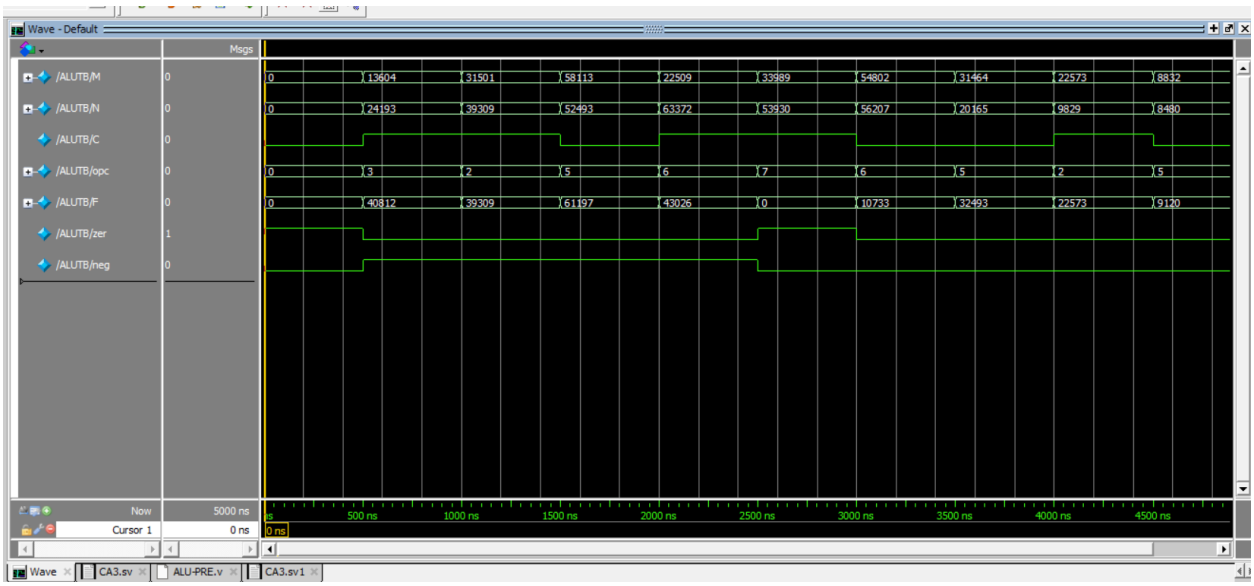
The number 526 that can be seen in the picture above is related to a number of gates before minimizing the circuit and using simple circuit logic and Regardless of the minimum hardware.

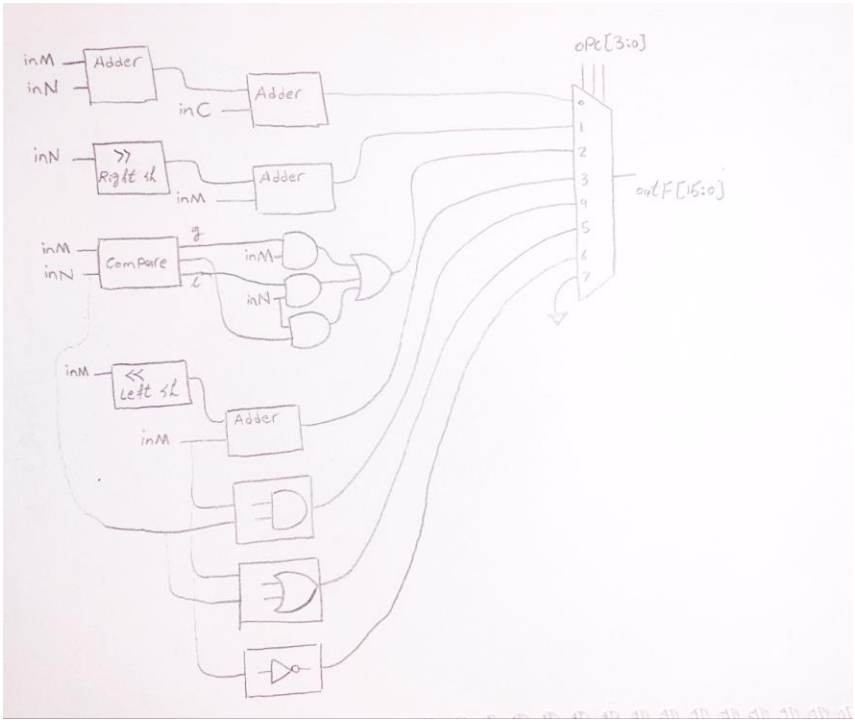
The waveform related to the first circuit before and after Synthesize can be seen above.



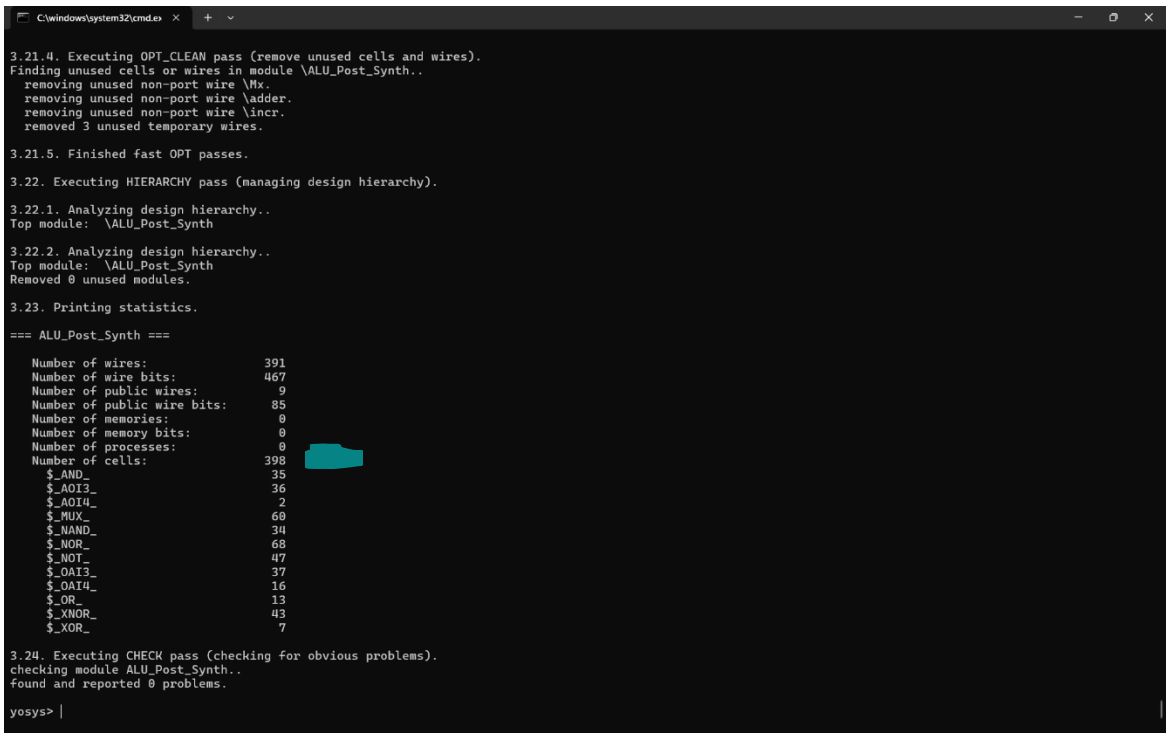


As you can see, after synthesize the delay values change a bit and there is a reason for this delay is for the gates defined in the library.

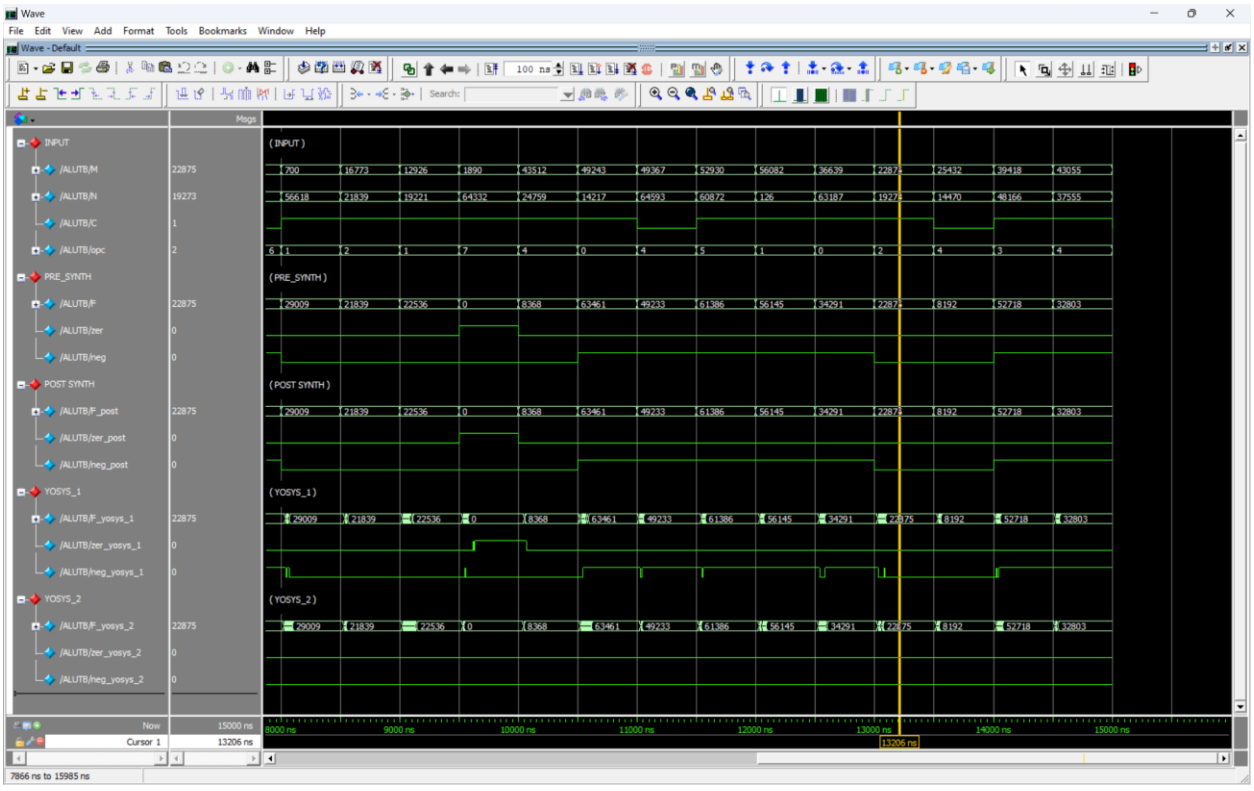
Circuit built in part 1 - Too Many Adders so too many gates.



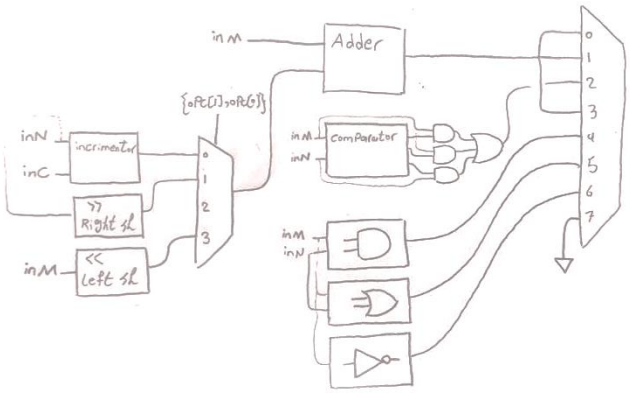
After combining all adders into one, we can see that number of cells shown in yosys is decreased to



398. About 100 less than previos version.



After synthesize the delay values increases and simulation speed decreases .the reason for this delay is for the gate delays defined in the library.



Bonus : simulation time before synthesize : 328961 microseconds per iteration

Yosys : 538751 microseconds per iteration

simulation time after synthesize : 283319 microseconds per iteration

Yosys : 287661 microseconds per iteration

In both situations simulation time for yosys is more than mine because yosys has a bigger file and more wires so simulation takes more time.