UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367 / Digital Systems I, ECE 894
Spring 1402-03
Computer Assignment 2
Extended expressions and synthesis
Week 6

Name:
Date:

In this assignment you will use the NOR gates of Assignment 1 for building a 5-variable function, and also building the same function using the pass-transistor based multiplexers of this assignment. You are to compare delay values and transistor counts of the two circuits.

Input of a five-input, three-output circuit are a1, a0, b1, b0, c0, and its outputs are c2, s1, and s0. Inputs a1 and a0 are treated as the bits of a two-bit number A, where a1 is the most and a0 is the least significant bit. Similarly, b1 and b0 are treated as the bits of a two-bit number B, where b1 is the most and b0 is the least significant bit. The third number is C and its only bit is c0. The output of the circuit is the three-bit number CS, the most to least significant bits of which are c2, s1, and s0 in this order. The CS output of the circuit is calculated by adding A, B and C together. For example, if A is 3, i.e., 11; B is 2, i.e., 10; and C is 1; then SC becomes 3+2+1 that is 110.

1. Using the NOR gates of Computer Assignment 1, build a circuit to calculate SC in terms of A, B, and C. Write a testbench, simulate this circuit, and find its worst-case delay based on the transistor delays of Assignment 1. You can use inverters as needed.
2. Write an **assign** statement to perform the add operation on the circuit inputs (a1, a0, b1, b0, c0) and calculate the output bits (c2, s1, s0). You can use {a2, a1} to form the 2-bit number, A, from a2 and a1. Use the worst-case delay from Part 1.
3. Using the pass-transistor based multiplexers of Computer Assignment 1, build a circuit to calculate SC in terms of A, B, and C. Write a testbench, simulate this circuit, and find its worst-case delay based on the transistor delays of Assignment 1. You can build an AND, an OR, and an XOR using a 2-to-1 multiplexer. You can use inverters as needed.
4. Write an **assign** statement to perform the add operation on the circuit inputs (a1, a0, b1, b0, c0) and calculate the output bits (c2, s1, s0). You can use {a2, a1} to form the 2-bit number, A, from a2 and a1. Use the worst-case delay from Part 3.
5. Write a testbench to test and compare the two circuits of Part 1 and Part 2. Compare timings and explain advantages and disadvantages of each circuit.
6. Write an **assign** statement similar to that of Part 2 without delay values. Use this in a Verilog module and use the Yosys synthesis tool for synthesizing your module. Use two and three input

NOR gates and inverters for your library elements. Use delay values for the library elements according to those of Assignment 1. In a testbench, perform post-synthesis simulation of your circuit.

7. Compare the results of Part 6 with your own hand design of Part 1.

Deliverables:

Generate a report that includes items discussed below for each of the four parts of this CA.

A. In Part 1, Show the circuit diagram that you are analyzing. Show how the NOR gates are wired together to form the structure you are designing.
B. In Part 3, Show the circuit diagram that you are analyzing. Show how the multiplexers are wired together to form the structure you are designing.
C. Hand-simulate the circuit you have shown in each part and write your expected values. For example, indicate what values you expect for the worst-case delays and express your reason for that.
D. Show your Verilog description of the design you are simulating and the testbench for it. Best is to use the Snip tools to get the image from Notepad++. This way you see all keywords and indentations. Make sure your Verilog codes are properly indented and all line-up rules are followed.
E. Show an image of the project that you have created in ModelSim for the simulation of your circuit.
F. When simulation is complete, or even if you have a partial simulation, include an image of the output waveform showing signal names being displayed.
G. For Yosys synthesis show all command line screens that you use. Show results from Yosys.

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastnameStudentnumber-CAn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.