Object Oriented Electronic Modeling - CA#1 Report

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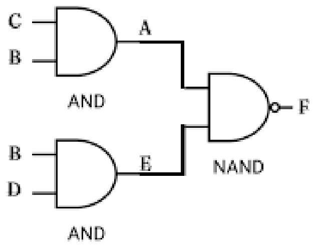
In this project, we simulated a digital circuit using an event-driven model in C++. We reused the *Wire* and *Gate* classes from our previous project, where basic gate behavior and signal management were already implemented. The first new component we added was the *IO* class, which handled parsing input files, testbenches, and managing user interaction. Then, we implemented a *Circuit* class to organize gates and wires into a complete circuit structure, connecting everything based on the input netlist. The core of the simulation lies in the *simulate* function, which processes time-ordered input transitions and propagates changes through the circuit while maintaining correct timing behavior. The simulation also supports unknown values ('X') when gate delays exceed testbench timing, ensuring realistic modeling.



Some Simple Logic Circuit

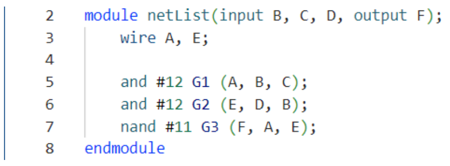
We simulated the Above Circuit just for test. In this Example Delay values are like this , AND : 11 , NAND :12

Hand Simulation :

A is Ready at : 12 , E is Ready at : 12

So F will be Ready at : 11 + 12 = 23ns

So the worth-case delay is 23ns.

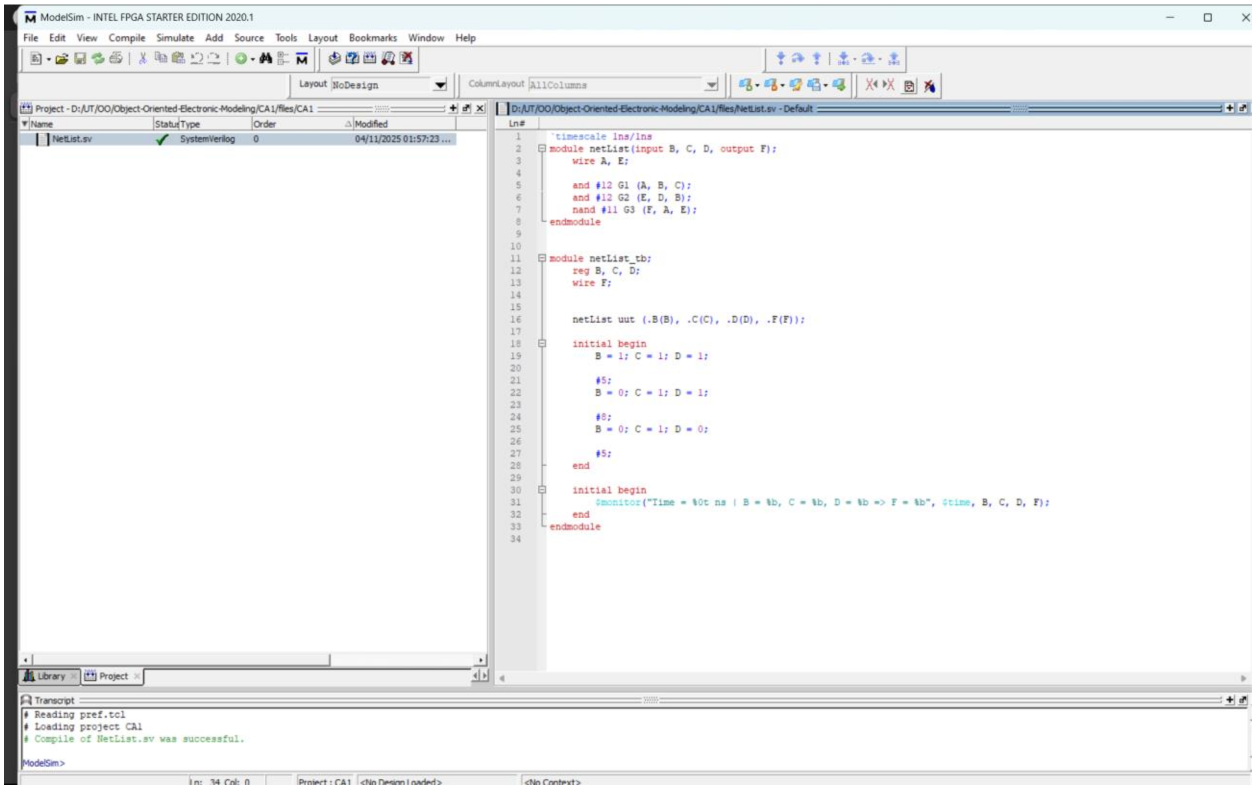


```
module netList(input B, C, D, output F);
    wire A, E;

    and #12 G1 (A, B, C);
    and #12 G2 (E, D, B);
    nand #11 G3 (F, A, E);
endmodule
```

The SystemVerilog Description of mentioned Circuit.

```
module netList_tb;
    reg B, C, D;
    wire F;


    netList uut (.B(B), .C(C), .D(D), .F(F));

    initial begin
        B = 1; C = 1; D = 1;

        #5;
        B = 0; C = 1; D = 1;

        #8;
        B = 0; C = 1; D = 0;

        #5;
    end

    initial begin
        $monitor("Time = %0t ns | B = %b, C = %b, D = %b => F = %b", $time, B, C, D, F);
    end
endmodule
```

Also the testbench



ModelSim - INTEL FPGA STARTER EDITION 2020.1

Project - D:/UT/OO/Object-Oriented-Electronic-Modeling/CA1/files/CA1

Name	Status	Type	Order	Modified
NetList.sv	✓	SystemVerilog	0	04/11/2025 01:57:23 ...

D:/UT/OO/Object-Oriented-Electronic-Modeling/CA1/files/NetList.sv - Default

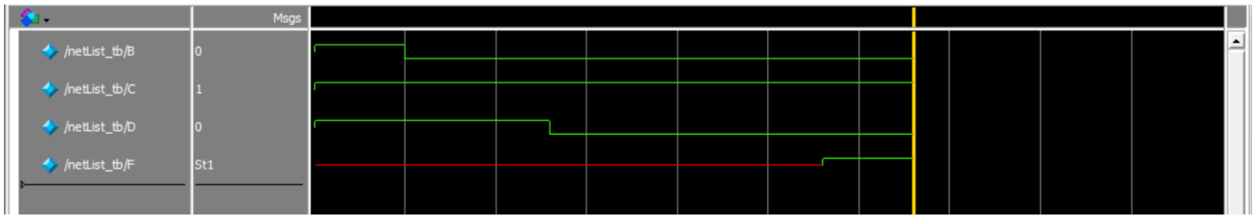
```
`timescale 1ns/1ns
module netList(input B, C, D, output F);
    wire A, E;

    and #12 G1 (A, B, C);
    and #12 G2 (E, D, B);
    nand #11 G3 (F, A, E);
endmodule


module netList_tb;
    reg B, C, D;
    wire F;


    netList uut (.B(B), .C(C), .D(D), .F(F));

    initial begin
        B = 1; C = 1; D = 1;

        #5;
        B = 0; C = 1; D = 1;

        #8;
        B = 0; C = 1; D = 0;

        #5;
    end

    initial begin
        $monitor("Time = %0t ns | B = %b, C = %b, D = %b => F = %b", $time, B, C, D, F);
    end
endmodule
```

Transcript

```
# Reading pref.tcl
# Loading project CA1
# Compile of NetList.sv was successful.

ModelSim>
```

Ln: 34 Col: 0 Project : CA1 <No Design Loaded> <No Context>

ModelSim Project



Simulation Result