UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Object-Oriented Modeling of Electronic Circuits, Spring 1404
Computer Assignment 1
Gate Level Event-based Simulation

Name **Date**

In this assignment you will develop an event driven gate-level simulator with Verilog netlist input in C++. The input netlist is a line-oriented Verilog gate-level description that only uses NOT, AND, NAND, OR, NOR, and XOR primitives with a single delay value. Primitive Gate instantiations are considered concurrent statements, and no assumption is made as to ordering of the gates. The netlist includes gate delay values using the # notation. There is no feedback in the circuit, and all circuit examples are combinational. The input file is free format. An example circuit from the ISCAS'85 benchmark circuits1 is made available for you to use for testing your programs.

The circuit under test (CUT) has a testbench in a separate file than the Verilog netlist. Test vectors in this file are line oriented. Each line (test vector) begins with a # followed by time of vector application and followed by a binary vector with logic values for the circuit inputs. Values for the inputs appear according to their order in the Verilog description. When generating the output value file, use the same format as the test input file.

1. Write a C++ program for reading the input Verilog description and generating an internal data structure for even-driven simulation.
2. Write a gate-level simulator for the Verilog description, not considering the gate delays, but considering that all instantiations are concurrent statements. This timing is referred to as unit-delay timing.
3. Write a gate-level simulator for the Verilog description, considering the gate delays and concurrent operation of gate instances.
4. In Part 2 and Part 3, read the input file with the format specified above and write the output file in the same fashion.
5. Optional: Generate the output in VCD format (or get an Open Source VCD write) and link it to your simulator.

Deliverables:

Generate a report that includes items discussed below for each of the five parts of this assignment.

A. Show the circuit diagram that you are analyzing. Show gates and/or transistors according to the specified delays.
B. Hand-simulate the circuit you have shown in Part A and write your expected values. For example, indicate what values you expect for the worst-case delays and express your reason for that.
C. Show your SystemVerilog description of the design you are simulating and the testbench for it. Best is to use the Snipping Tool to get the image from Notepad++. This way you see

[1] The ISCAS'85 benchmark circuits are ten combinational networks provided to authors at the 1985 International Symposium on Circuits And Systems. They subsequently have been used by many researchers as a basis for comparing results in the area of test generation.

all keywords and indentations. Make sure your SV codes are properly indented, and all line-up rules are followed.

D. Show an image of the project that you have created in ModelSim for the simulation of your circuit.
E. When simulation is complete, or even if you have a partial simulation, include an image of the output waveform showing signal names being displayed.

Make a PDF file of your report and name it with the format shown below:
FirstinitialLastnameStudentnumber-CAn-ECEmmm

Where nn is a two-digit number for the Computer Assignment, mmm is the three-digit course number under which you are registered, and hopefully you know the rest. For the Firstinitial use only one character. For Lastname and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the Studentnumber field of the report file name.