University of Tehran

Electrical and Computer Engineering Department

ECE (8101) 342

Object Oriented Modeling of Electronic Circuits – Spring 1404

Homework 2: C++ Gate Modeling
Due Date: Last day of 1403

C++ gate-level netlist
C++ procedural gate-level simulation.

In this homework you will use the C++ environment and C++ gate classes to develop a hardware gate-level simulation.

Instead of forming an event-queue or using a timing wheel simulation, develop a circuit class that consists of an unordered list of logic gate classes to be simulated in a way that mimics concurrent simulation of the gate classes. For this purpose, the circuit class consists of gate objects and their interconnections, and evl() functions for each of the gate classes. A gate class consists of a flag that indicates if the output value has changed in the last call of the evl() function.

The circuit class of gates has an evl() function that has a loop of all evl() functions of gates used in the logic class. The loop takes the input values and continues to call all evl() functions for as long as there is at least one gate change in the run. The loop stops when there is no more gate change in any of the evl() functions. There may be a hierarchy of circuits.

Use a wire class and gate classes as discussed in class.