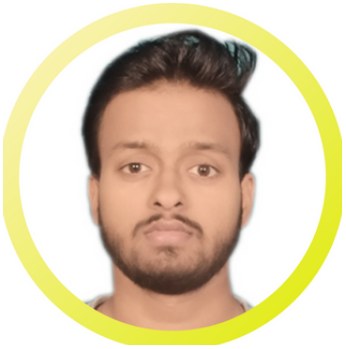

Amir Sharfuddin

Campus Recruitment Coordinator
NIT Srinagar

+918808886588
amir_04mtech20@nitsri.net

ABOUT ME

Seeking a challenging position in a reputed organization where I can learn new skills, and leverage my learning. To get an opportunity where I can make the best of my potential and contribute to the organizations's growth.

SKILLS & PROFICIENCIES

- Language: C, Java, VHDL and Verilog
- Development Tools : Xilinx (Vivado & ISIM), Silvaco Atlas (2D Structure) , LT Spice, & Scilab.
- OS : Windows & Linux

CERTIFICATION & VOLUNTEER WORK

- Covid-19 volunteer at Sharjah, UAE
- Participate TedEx Poloview, Srinagar
- Cleared National level exam Gate-2020.
- Certified in "Lead Summit" organised by IIT-BHU at Varanasi,
- Certified in "E-Cell" sponsored by IIT Bombay at Lucknow,
- Certified in "Digital photography & Image Editing Technology" sponsored by the National Science & Technology Entrepreneurship Development Board (NSTEDB), Department of Science & Technology.
- Member of "The Flying Club" in 2014-2017.

EDUCATIONAL BACKGROUND

National Institute of Technology, Srinagar
Srinagar, J & K
CGPA: 8.1
Stream: M.Tech in Microelectronics
2020-Present

Dr A.P.J Abdul Kalam Technical University, Lucknow
Lucknow U.P
CGPA: 7.5
B.Tech in Electronics & Communication Engg.
2013-2017

Children Higher Sen. Sec. School
Azamgarh U.P
CGPA: 7.5
PCM
2011-2013

ACADEMIC PROJECT

- **Modelling and Simulation of Double Gate Electronically doped Field Effect Transistor (EDTFET): (Dec 2021- Present)**

The Structure of EDTFET is gate-source and gate-drain overlaps are used. So, that able to achieve ON and OFF current ratio higher and subthreshold slope also higher. In the device, doping less (or lightly doped) Si is used, and the formation of the drain (D)–channel–source (S) is achieved with the application of appropriate bias at polarity gates (PGs) (i.e., electrically doped) yield p+ and n+ S/D regions. I used the Silvaco Atlas tool.

- **Cryptographic Coprocessor Design using VHDL : (Jan 2022 - Present)**

The coprocessor provides standard instructions and dedicated function units are specific for security. The co-processor is designed and implemented in VHDL, but the N-bit Adder in the ALU unit is implemented in Verilog. Which is capable of selecting different algorithms through programming, and performing crypto operations such as key management, data encryption, and decryption

- **Modelling and Simulation of Double Gate Tunnel Field Effect Transistor (DGTFET): (Oct 2021- Dec 2021)**

2D device simulations with the help of Silvaco Atlas, Implement the XOR and XNOR logic functions. The Structure of XOR is designed the band to band tunnelling (BTBT) occurs at the boundary of the gates rather than at the source-channel junction. And XNOR function, the gate-source and gate-drain overlaps are used. So, that able to achieve ON and OFF current ratio higher and subthreshold slope also higher.

- **Error Detection & Correction using Verilog: (Jan 2017 - July 2017)**

Hamming code in RTL design & perform timing simulation & synthesis and also analyze the error probability that is occurring during transmission. Here, Xilinx ISE 14.7 Simulator has been used for simulating Verilog Codes of Hamming encoder & decoder.

- **Radia Control Aircraft: (Sep 2016 - Jan 2017)**

Worked on an RC Plane project that involved the building of glider type remote control planes. Our major role was designing, creating, and assembling such planes using Foam/Balsa wood. They were usually of two types: Rubber powered, Battery powered and resembled catapult-launch gliders. After multiple successful flights, we tried adding more components to it like GPS, Range Finder, Camera, etc.

INTERN

VLSI Intern, IIT-BHU Varanasi (May 2016 – July 2016): Analog Design with the help of the "Silvaco TCAD 2D device Simulation" framework that enables simulation of the electrical, optical & thermal behaviour of semiconductor devices.