1. Description

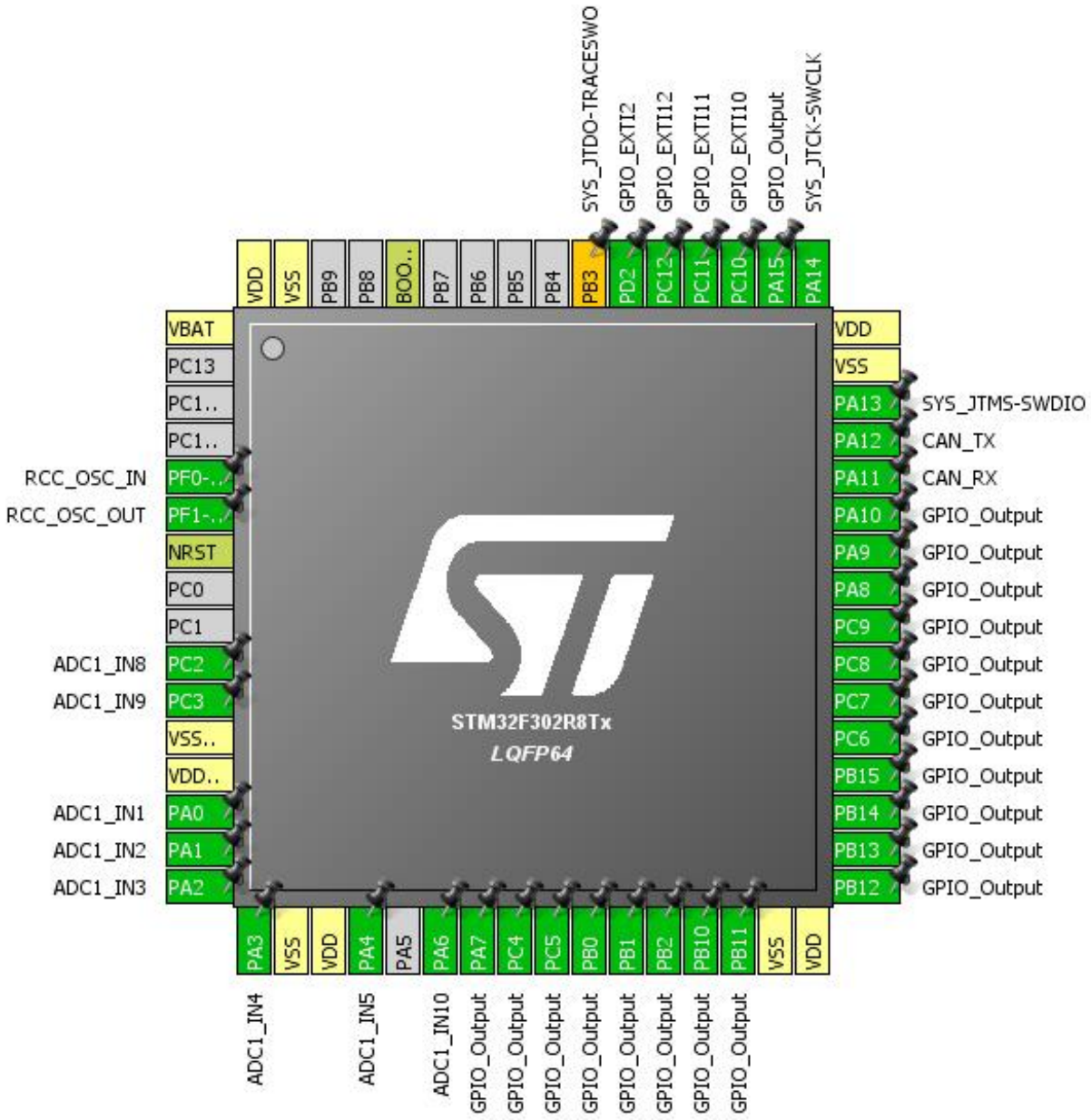
1.1. Project

Project Name	PDM
Board Name	PDM
Generated with:	STM32CubeMX 4.27.0
Date	11/29/2018

1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F302
MCU name	STM32F302R8Tx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



3. Pins Configuration

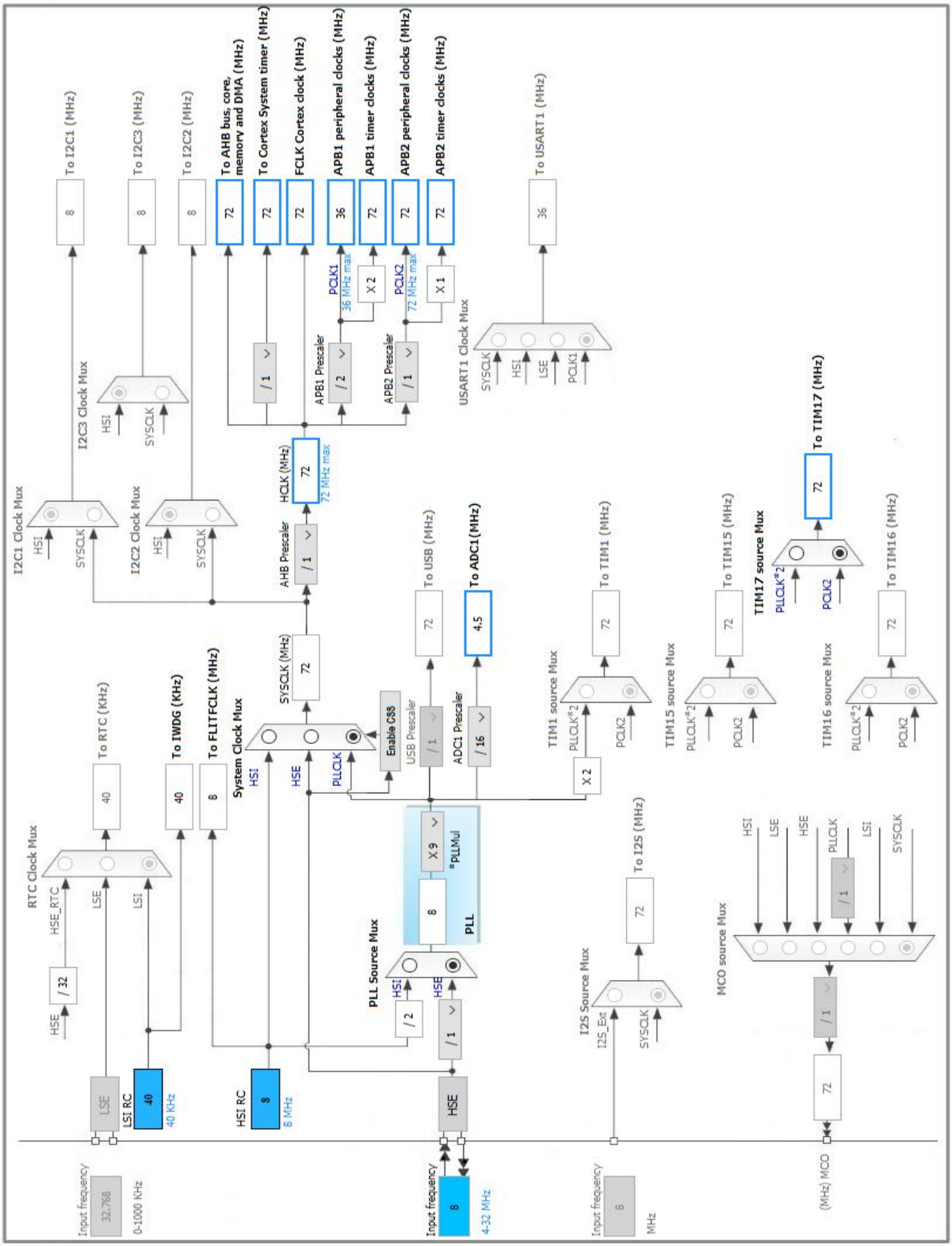
Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
10	PC2	I/O	ADC1_IN8	
11	PC3	I/O	ADC1_IN9	
12	VSSA/VREF-	Power		
13	VDDA/VREF+	Power		
14	PA0	I/O	ADC1_IN1	
15	PA1	I/O	ADC1_IN2	
16	PA2	I/O	ADC1_IN3	
17	PA3	I/O	ADC1_IN4	
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	ADC1_IN5	
22	PA6	I/O	ADC1_IN10	
23	PA7 *	I/O	GPIO_Output	
24	PC4 *	I/O	GPIO_Output	
25	PC5 *	I/O	GPIO_Output	
26	PB0 *	I/O	GPIO_Output	
27	PB1 *	I/O	GPIO_Output	
28	PB2 *	I/O	GPIO_Output	
29	PB10 *	I/O	GPIO_Output	
30	PB11 *	I/O	GPIO_Output	
31	VSS	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Output	
34	PB13 *	I/O	GPIO_Output	
35	PB14 *	I/O	GPIO_Output	
36	PB15 *	I/O	GPIO_Output	
37	PC6 *	I/O	GPIO_Output	
38	PC7 *	I/O	GPIO_Output	
39	PC8 *	I/O	GPIO_Output	
40	PC9 *	I/O	GPIO_Output	
41	PA8 *	I/O	GPIO_Output	
42	PA9 *	I/O	GPIO_Output	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
43	PA10 *	I/O	GPIO_Output	
44	PA11	I/O	CAN_RX	
45	PA12	I/O	CAN_TX	
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
50	PA15 *	I/O	GPIO_Output	
51	PC10	I/O	GPIO_EXTI10	
52	PC11	I/O	GPIO_EXTI11	
53	PC12	I/O	GPIO_EXTI12	
54	PD2	I/O	GPIO_EXTI2	
55	PB3 **	I/O	SYS_JTDO-TRACESWO	
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

IN1: IN1 Single-ended
IN2: IN2 Single-ended
IN3: IN3 Single-ended
IN4: IN4 Single-ended
IN5: IN5 Single-ended
IN8: IN8 Single-ended
IN9: IN9 Single-ended
IN10: IN10 Single-ended
mode: Temperature Sensor Channel
mode: Vrefint Channel
mode: Vbat Channel

5.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**8 ***
External Trigger Conversion Source	**Timer 2 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	**2 ***
Channel	**Channel 2 ***
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**3 ***
Channel	

	Channel 3 *
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**4 ***
Channel	**Channel 4 ***
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**5 ***
Channel	**Channel 5 ***
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**6 ***
Channel	**Channel 8 ***
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**7 ***
Channel	**Channel 9 ***
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**8 ***
Channel	**Channel 10 ***
Sampling Time	**4.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	1
Channel	Channel 1
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

5.2. CAN

mode: Mode

5.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**8 ***
Time Quantum	**222.22222222222223 ***
Time Quanta in Bit Segment 1	**7 Times ***
Time Quanta in Bit Segment 2	1 Time
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	**Enable ***
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	**Enable ***
Receive Fifo Locked Mode	**Enable ***
Transmit Fifo Priority	**Enable ***

Advanced Parameters:

Operating Mode	Normal

5.3. IWDG

mode: Activated

5.3.1. Parameter Settings:

Watchdog Clocking:

IWDG counter clock prescaler	**256 ***
IWDG window value	**31 ***
IWDG down-counter reload value	**31 ***

5.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

5.5. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.6. TIM2

Clock Source : Internal Clock

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**14400 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***

5.7. TIM6

mode: Activated

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**640 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.8. TIM17

mode: Activated

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**65535 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC2	ADC1_IN8	Analog mode	No pull up pull down	n/a	
	PC3	ADC1_IN9	Analog mode	No pull up pull down	n/a	
	PA0	ADC1_IN1	Analog mode	No pull up pull down	n/a	
	PA1	ADC1_IN2	Analog mode	No pull up pull down	n/a	
	PA2	ADC1_IN3	Analog mode	No pull up pull down	n/a	
	PA3	ADC1_IN4	Analog mode	No pull up pull down	n/a	
	PA4	ADC1_IN5	Analog mode	No pull up pull down	n/a	
	PA6	ADC1_IN10	Analog mode	No pull up pull down	n/a	
CAN	PA11	CAN_RX	Alternate Function Push Pull	No pull up pull down	**High ***	
	PA12	CAN_TX	Alternate Function Push Pull	No pull up pull down	**High ***	
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
Single Mapped Signals	PB3	SYS_JTDO-TRACESWO	n/a	n/a	n/a	
GPIO	PA7	GPIO_Output	**Output Open Drain ***	**Pull up ***	Low	
	PC4	GPIO_Output	**Output Open Drain ***	**Pull up ***	Low	
	PC5	GPIO_Output	**Output Open Drain ***	**Pull up ***	Low	
	PB0	GPIO_Output	Output Push Pull	No pull up pull down	Low	
	PB1	GPIO_Output	**Output Open Drain ***	**Pull up ***	Low	
	PB2	GPIO_Output	**Output Open Drain ***	**Pull up ***	Low	
	PB10	GPIO_Output	**Output Open Drain ***	**Pull up ***	Low	
	PB11	GPIO_Output	**Output Open Drain ***	**Pull up ***	Low	
	PB12	GPIO_Output	**Output Open Drain ***	**Pull up ***	Low	
	PB13	GPIO_Output	**Output Open Drain ***	**Pull up ***	Low	
	PB14	GPIO_Output	**Output Open Drain ***	**Pull up ***	Low	
	PB15	GPIO_Output	**Output Open Drain ***	**Pull up ***	Low	
	PC6	GPIO_Output	**Output Open Drain ***	**Pull up ***	Low	
	PC7	GPIO_Output	**Output Open Drain ***	**Pull up ***	Low	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC8	GPIO_Output	**Output Open Drain ***	**Pull up ***	Low	
	PC9	GPIO_Output	**Output Open Drain ***	**Pull up ***	Low	
	PA8	GPIO_Output	**Output Open Drain ***	**Pull up ***	Low	
	PA9	GPIO_Output	**Output Open Drain ***	**Pull up ***	Low	
	PA10	GPIO_Output	Output Push Pull	**Pull up ***	Low	
	PA15	GPIO_Output	Output Push Pull	**Pull up ***	Low	
	PC10	GPIO_EXTI10	**External Interrupt Mode with Falling edge trigger detection**	No pull up pull down	n/a	
	PC11	GPIO_EXTI11	External Interrupt Mode with Rising edge trigger detection	No pull up pull down	n/a	
	PC12	GPIO_EXTI12	**External Interrupt Mode with Rising/Falling edge**	No pull up pull down	n/a	
	PD2	GPIO_EXTI2	**External Interrupt Mode with Falling edge trigger detection**	No pull up pull down	n/a	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Channel1	Peripheral To Memory	**High ***

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	**Word ***

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line2 and Touch Sense controller	true	0	0
DMA1 channel1 global interrupt	true	0	0
CAN TX and USB high priority interrupts	true	0	0
CAN RX0 and USB low priority interrupts	true	0	0
CAN RX1 interrupt	true	0	0
TIM1 trigger, commutation and TIM17 interrupts	true	0	0
TIM2 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	0	0
TIM6 global interrupt, DAC interrupts	true	0	0
PVD interrupt through EXTI line16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 interrupt	unused		
CAN SCE interrupt	unused		
Floating point unit interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F3
Line	STM32F302
MCU	STM32F302R8Tx
Datasheet	025147_Rev7

7.2. Parameter Selection

Temperature	25
Vdd	3.6

8. Software Project

8.1. Project Settings

Name	Value
Project Name	PDM
Project Folder	C:\Users\thekenu\UBC Formula Electric\Consolidated-Firmware\src\PDM
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F3 V1.10.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

9. Software Pack Report