1. Description

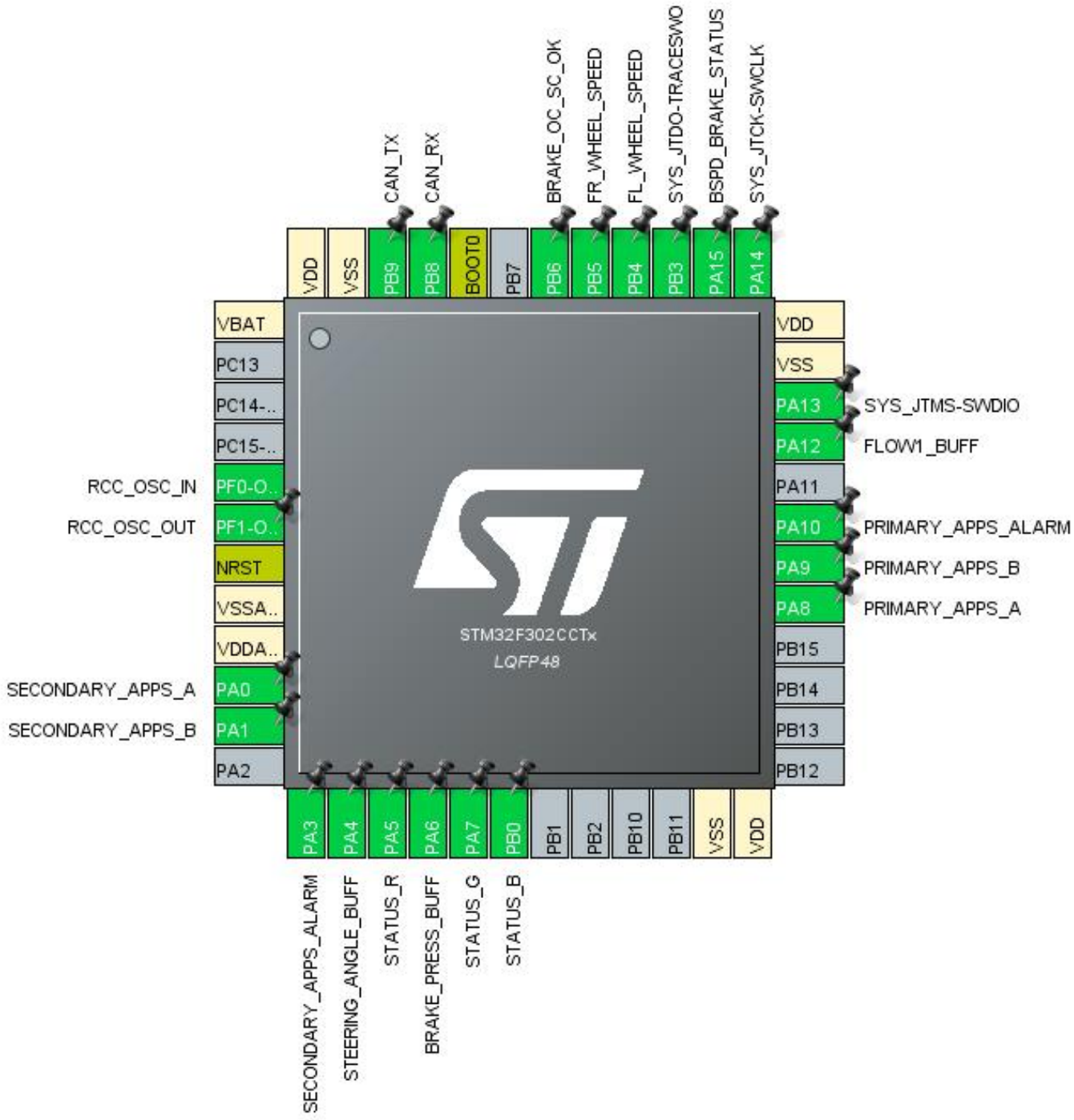
1.1. Project

Project Name	FSM_old
Board Name	custom
Generated with:	STM32CubeMX 5.3.0
Date	02/11/2023

1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F302
MCU name	STM32F302CCTx
MCU Package	LQFP48
MCU Pin number	48

2. Pinout Configuration

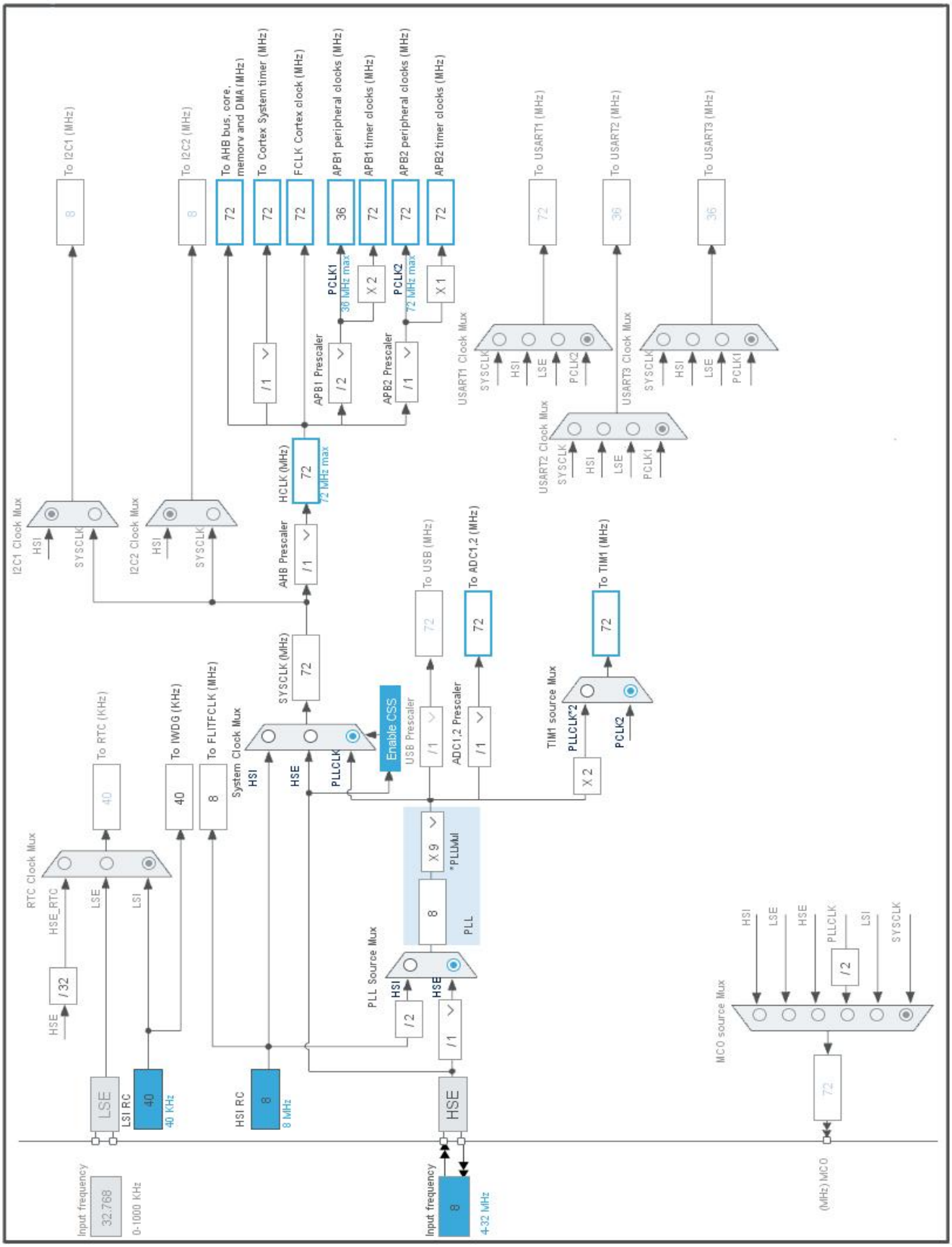


3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA/VREF-	Power		
9	VDDA/VREF+	Power		
10	PA0	I/O	TIM2_CH1	SECONDARY_APPS_A
11	PA1	I/O	TIM2_CH2	SECONDARY_APPS_B
13	PA3 *	I/O	GPIO_Input	SECONDARY_APPS_ALARM
14	PA4	I/O	ADC2_IN1	STEERING_ANGLE_BUFF
15	PA5 *	I/O	GPIO_Output	STATUS_R
16	PA6	I/O	ADC2_IN3	BRAKE_PRESS_BUFF
17	PA7 *	I/O	GPIO_Output	STATUS_G
18	PB0 *	I/O	GPIO_Output	STATUS_B
23	VSS	Power		
24	VDD	Power		
29	PA8	I/O	TIM1_CH1	PRIMARY_APPS_A
30	PA9	I/O	TIM1_CH2	PRIMARY_APPS_B
31	PA10 *	I/O	GPIO_Input	PRIMARY_APPS_ALARM
33	PA12	I/O	TIM4_CH2	FLOW1_BUFF
34	PA13	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	
38	PA15	I/O	GPIO_EXTI15	BSPD_BRAKE_STATUS
39	PB3	I/O	SYS_JTDO-TRACESWO	
40	PB4	I/O	TIM16_CH1	FL_WHEEL_SPEED
41	PB5	I/O	TIM17_CH1	FR_WHEEL_SPEED
42	PB6 *	I/O	GPIO_Input	BRAKE_OC_SC_OK
44	BOOT0	Boot		
45	PB8	I/O	CAN_RX	
46	PB9	I/O	CAN_TX	
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	FSM_old
Project Folder	C:\Users\jessi\Documents\School\Grade_13\fsae\Consolidated-
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F3 V1.10.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F3
Line	STM32F302
MCU	STM32F302CCTx
Datasheet	025186_Rev7

6.2. Parameter Selection

Temperature	25
Vdd	3.6

7. IPs and Middleware Configuration

7.1. ADC2

IN1: IN1 Single-ended

IN3: IN3 Single-ended

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	ADC Asynchronous clock mode
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data overwritten
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	**2 ***
External Trigger Conversion Source	**Timer 3 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 1
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0
Rank	**2 ***
Channel	**Channel 3 ***
Sampling Time	**61.5 Cycles ***
Offset Number	No offset
Offset	0

ADC_Injected_ConversionMode:

Enable Injected Conversions	Enable
Number Of Conversions	0

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. CAN

mode: Mode

7.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**9 ***
Time Quantum	**250.0 ***
Time Quanta in Bit Segment 1	**6 Times ***
Time Quanta in Bit Segment 2	1 Time
ReSynchronization Jump Width	**4 Times ***

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	**Enable ***
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	**Enable ***
Receive Fifo Locked Mode	**Enable ***
Transmit Fifo Priority	**Enable ***

Advanced Parameters:

Operating Mode	Normal

7.3. IWDG

mode: Activated

7.3.1. Parameter Settings:

Watchdog Clocking:

IWDG counter clock prescaler	4
IWDG window value	IWDG_WINDOW_DISABLE_VALUE
IWDG down-counter reload value	**LSI_FREQUENCY / IWDG_PRESCALER / IWDG_RESET_FREQUENCY ***

7.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.5. SYS

Debug: Trace Asynchronous Sw

Timebase Source: TIM6

7.6. TIM1

Combined Channels: Encoder Mode

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**71 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**TIM1_AUTO_RELOAD_REG ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1

____ Parameters for Channel 1 ____

Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**3 ***
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	**3 ***

7.7. TIM2

Combined Channels: Encoder Mode

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**TIM2_AUTO_RELOAD_REG ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.8. TIM3

Clock Source : Internal Clock

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**TIM3_PRESCALER - 1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**(TIMx_FREQUENCY / TIM3_PRESCALER / ADC_FREQUENCY) - 1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	**Update Event ***

7.9. TIM4

Channel2: Input Capture direct mode

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**TIM4_PRESCALER ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**TIM4_AUTO_RELOAD_REG ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.10. TIM16

mode: Activated

Channel1: Input Capture direct mode

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**TIM16_PRESCALER ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**TIM16_AUTO_RELOAD_REG ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.11. TIM17

mode: Activated

Channel1: Input Capture direct mode

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**TIM17_PRESCALER ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**TIM17_AUTO_RELOAD_REG ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.12. FREERTOS

Interface: CMSIS_V1

7.12.1. Config parameters:

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	**Static ***

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	**Enabled ***
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	**Option2 ***

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	**Enabled ***
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

7.12.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	**Enabled ***
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	**Enabled ***
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC2	PA4	ADC2_IN1	Analog mode	No pull up pull down	n/a	STEERING_ANGLE_BUFF
	PA6	ADC2_IN3	Analog mode	No pull up pull down	n/a	BRAKE_PRESS_BUFF
CAN	PB8	CAN_RX	Alternate Function Push Pull	No pull up pull down	**High ***	
	PB9	CAN_TX	Alternate Function Push Pull	No pull up pull down	**High ***	
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PB3	SYS_JTDO-TRACESWO	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull up pull down	Low	PRIMARY_APPS_A
	PA9	TIM1_CH2	Alternate Function Push Pull	No pull up pull down	Low	PRIMARY_APPS_B
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	No pull up pull down	Low	SECONDARY_APPS_A
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull up pull down	Low	SECONDARY_APPS_B
TIM4	PA12	TIM4_CH2	Alternate Function Push Pull	**Pull down ***	Low	FLOW1_BUFF
TIM16	PB4	TIM16_CH1	Alternate Function Push Pull	No pull up pull down	Low	FL_WHEEL_SPEED
TIM17	PB5	TIM17_CH1	Alternate Function Push Pull	No pull up pull down	Low	FR_WHEEL_SPEED
GPIO	PA3	GPIO_Input	Input mode	No pull up pull down	n/a	SECONDARY_APPS_ALARM
	PA5	GPIO_Output	Output Push Pull	No pull up pull down	Low	STATUS_R
	PA7	GPIO_Output	Output Push Pull	No pull up pull down	Low	STATUS_G
	PB0	GPIO_Output	Output Push Pull	No pull up pull down	Low	STATUS_B
	PA10	GPIO_Input	Input mode	No pull up pull down	n/a	PRIMARY_APPS_ALARM
	PA15	GPIO_EXTI15	External Interrupt Mode with Rising edge trigger detection	No pull up pull down	n/a	BSPD_BRAKE_STATUS
	PB6	GPIO_Input	Input mode	No pull up pull down	n/a	BRAKE_OC_SC_OK

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC2	DMA2_Channel1	Peripheral To Memory	Low

ADC2: DMA2_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
USB high priority or CAN_TX interrupts	true	5	0
USB low priority or CAN_RX0 interrupts	true	5	0
CAN RX1 interrupt	true	5	0
TIM1 update and TIM16 interrupts	true	5	0
TIM1 trigger, commutation and TIM17 interrupts	true	5	0
TIM3 global interrupt	true	5	0
TIM4 global interrupt	true	5	0
Timer 6 interrupt and DAC underrun interrupts	true	0	0
DMA2 channel1 global interrupt	true	5	0
PVD interrupt through EXTI line16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 interrupts	unused		
CAN SCE interrupt	unused		
TIM1 break and TIM15 interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
Floating point unit interrupt	unused		

*** User modified value**

9. Software Pack Report