Experiment 1 - Clock and Periodic Signal Generation

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Abstract: In this experiment we learned different methods of generating clock signal and their pros and cons besides getting know to 7400 series ICs.

Keywords: *clock generation - digital logic gates– counter – frequency divider – duty cycle – IC's*

I. EXPERIMENTS

A. Ring Oscillator

A 74LS04 is an IC that has 6 inverters inside by connecting odd terminals of the IC and connecting the output of the last inverter to the input of the next one, the output of each inverter will oscillate.

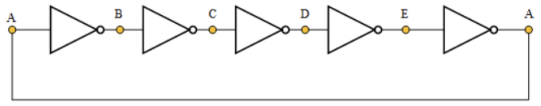

Fig.1: Ring oscillator circuit [1]

By connecting 5 terminals of the IC (5 inverters) we will have a ring oscillator with a frequency of about 13 MHz (as shown below).

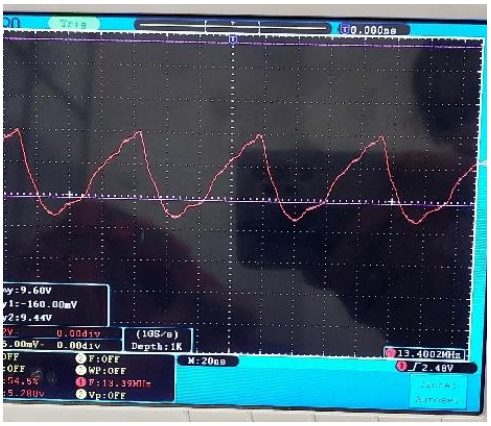

Fig. 2: Ring oscillator output

We can calculate the delay of a single inverter using a ring oscillator, to measure the propagation delay of the chain, we should measure the time from the 50% point of input to the 50% point of output. This period is equal to half of period time of the output, that is about 40 ns

Using ring oscillator period time formula, we can have the delay of a single inverter:

$$T_{ring\ oscillator} = 2N\Delta \ ; \quad \Delta: Inverter\ delay$$

$$40=2*5*\Delta$$

$$\rightarrow \Delta = 4\ ns$$

B. LM555 Timer

This IC operates in three mode : Monostable, Bistable and Astable. And can be used for generating clock signal or delays. In astable mode it operates as an oscillator and in this experiment we will use astable mode.

Figure 3: LM555 timer pin-out

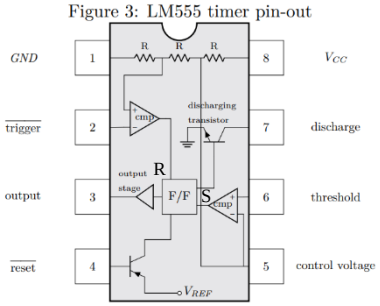

Fig. 3: LM555 timer pin-out [1]

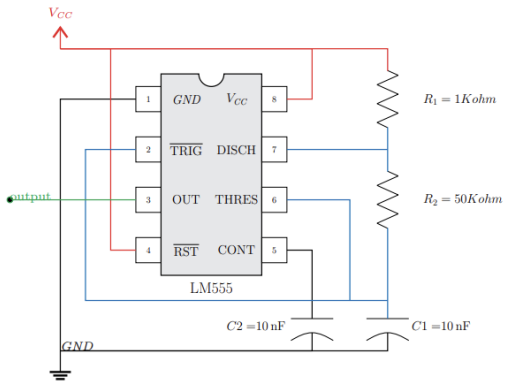

Fig. 4: LM555 in astable mode [1]

At first capacitor C1 is empty and starts to charge. In this state the FF reset to 0, Then output is 1 (duo to inverter at FF output). When C1 charges until %66 of VCC FF sets to 1 and output is 0. C1 charges from R1+R2 and discharges through R2. Therefor the charge period is more than discharge period and we have a duty cycle above %50.

We can change R1, R2, C1 values to reach desired frequency and duty cycle. By default, values of R1, R2, C1 are set based on Fig.4 :

$$T = 0.693(R_1 + 2R_2)C_1 \rightarrow \ T = 699.93\ \mu s$$

$$f = \frac{1}{T} \rightarrow f = 1.428\ KHz$$

$$duty\ cycle = \frac{R_1 + R_2}{R_1 + 2R_2} = 0.50 = \%50$$

Then we have the output:

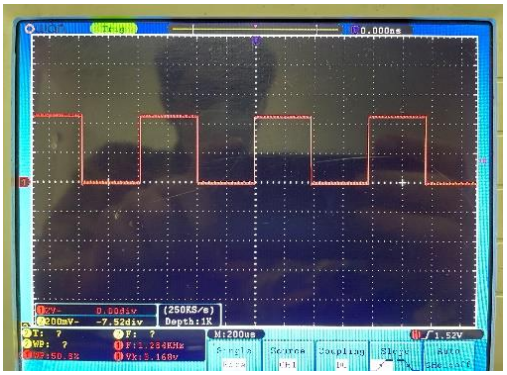

Fig. 5: LM555 output waveform

As we see in waveform above, Output has a 1.284KHz frequency and about %50.3 duty cycle. There is a little bit difference between real life and calculations. That's because of circuit disturbance and oscilloscope accuracy. By changing R۲ value, we will have different frequencies and duty cycles according to calculations above:

The results that were calculated are also attached in the following.

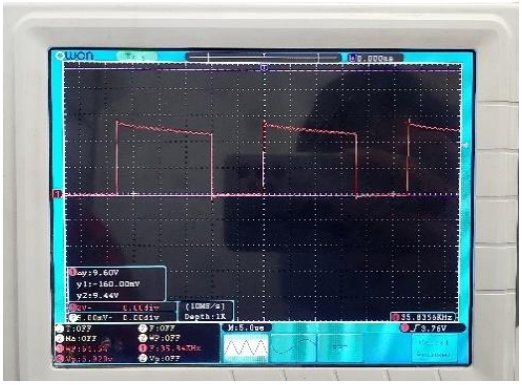

Fig. 6: LM555 output with 1KΩ resistor

For 1kΩ resistor:

Observations: T = 28us, T1=18, F = 35.8KHz

Duty Cycle = T1/T=18/23= 64%

Theoretical: T = 0.693 * (1 + 2)*10^3 * 10*10^-9 = 20.79us
Duty Cycle = 2/3 = 66.6%

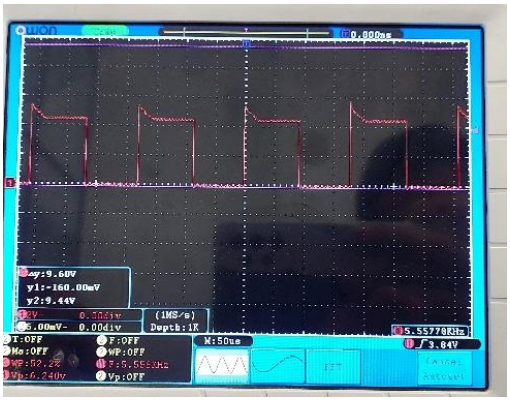

Fig. 7: LM555 output with 10KΩ resistor

For 10kΩ resistor:

Observations: T = 200us,T1=90 us, F=5.5KHz

Duty Cycle = T1/T=90/200= 45%

Theoretical: 0.693 * (1 + 20)*10^3 * 10*10^-9 = 145.5us

Duty Cycle = 11/21 = 52.3%

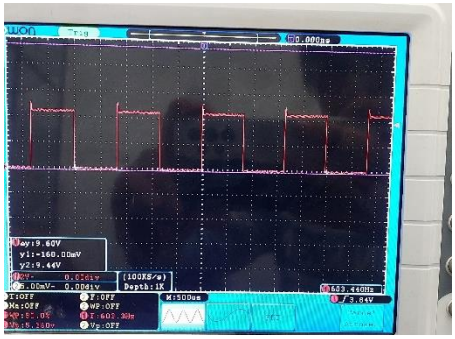

Fig. 8: LM555 output with 100KΩ resistor

For 100kΩ resistor:

Observations: T = 1600us,T1=800 us, F = 0.603KHz Duty Cycle = T1/T=800/1600= 50%

%Theoretical: T = 0.693 * (1 + 400)*10^3 * 10*10^-9 = 2.78ms

Duty Cycle = 201/401 = 50.1%

Table I. LM555 freq. and duty cycle change duo to R۲ value

Resistor (KΩ)	1	10	100
Frequency (KHz)	35.8	5.5	0.603
Duty cycle	64%	52.3%	50.1%

As we see the more R2 increases the less frequency and duty cycle we have.

Note that the difference between calculations and real life is due to circuit disturbance and oscilloscope accuracy.

C. Schmitt Trigger Oscillator

Using one inverter of 74HCT14, we can shape a Schmitt Trigger Oscillator.

If we connect the output and the input of the Schmitt trigger by a resistor and it's input to the ground using a capacitor, according to figure 9, V_{out} should oscillate.

The frequency of clock cycle is equal to $\frac{\alpha}{RC}$ which α is a constant that depends on IC model.

Let's consider the capacitor has no charge at first. V_{in} would be zero and V_{out} must be equal to V_{cc}. Then the capacitor starts to charge until its voltage becomes V_{Th+}. At this point V_{out} will become zero and the capacitor starts to discharge. It will continue till its charge gets to V_{Th-}. This process would repeat and repeat and as we expected, we'll see a square wave at V_{out}.

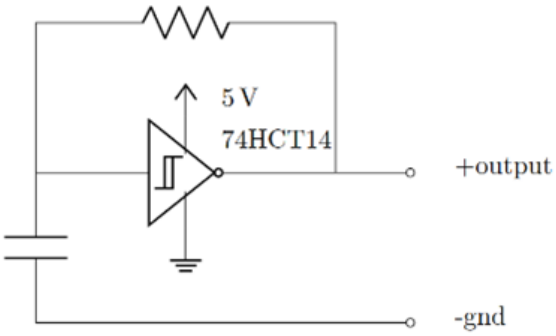

Fig. 10: Schmitt inverter oscillator circuit [1]

The function of this circuit is based on charging and discharging of the capacitor. Higher time constant (τ) leads to much taken time to oscillate.

Using a 74HCT14 we assembled the circuit with and by changing the resistors, we measured the different frequencies and α. The results can be seen in the table below.

Table II. measurement of α

Resistor (Ω)	**470**	**1000**	**2200**
Frequency (KHz)	129.6	63	23
α	0.69	0.63	0.5

The upcoming pictures are waveform results of this experiment.

Fig. 10: Schmitt trigger with 470Ω resistor

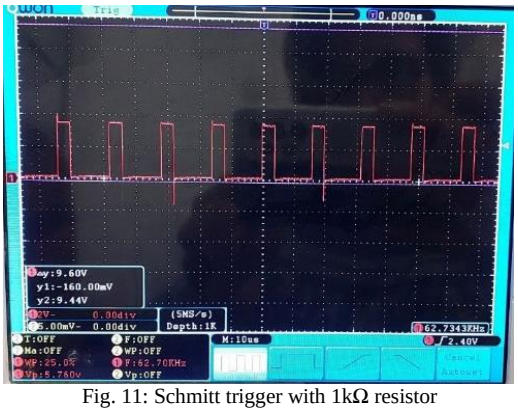

Fig. 11: Schmitt trigger with 1kΩ resistor

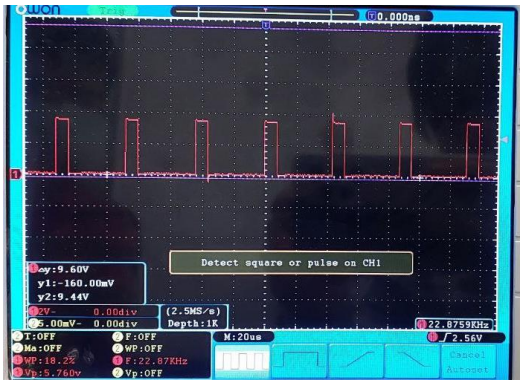

Fig. 12: Schmitt trigger with 2.2kΩ resistor

D. Synchronous Counter as a Frequency Divider

We are about to cascading two 4-bit counters and in this case the maximum value that can be reached is $2^8 = 256$. On the other hand, we should build a divide-by-200 frequency divider, so we must put $256 - 200 = 56$ which is 00111000 on parallel inputs. We assembled the circuit and connected corresponding inputs to gnd and V_{cc} as it was said in the manual. For the primary initialization, using a 74HC08 IC, we added an AND gate to the load pin to have a preset pin. By connecting the output of the Ring Oscillator to the input of the first counter, the carry out pin of the first counter to the clock input of the second counter and the carry

out pin of the second counter to both load inputs, the circuit will divide the frequency by the given value.

As we saw in the first part, the frequency of the Ring Oscillator was about 21.6MHz. It can be seen that the output frequency is about 107KHz. As we expected the frequency was divided by 200.

So, this is a better device to generate lower frequencies clock cycles.

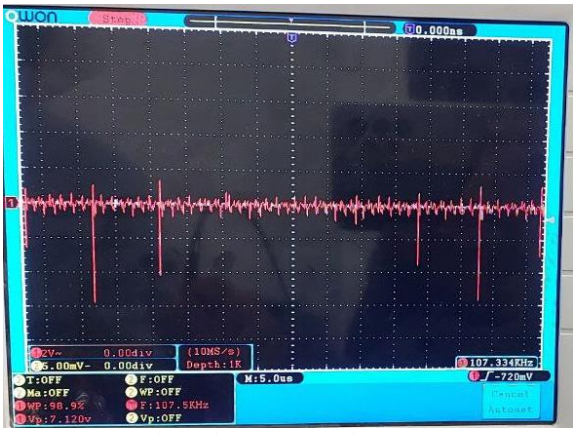

Fig. 13: Waveform of carry out pin of the MSB counter

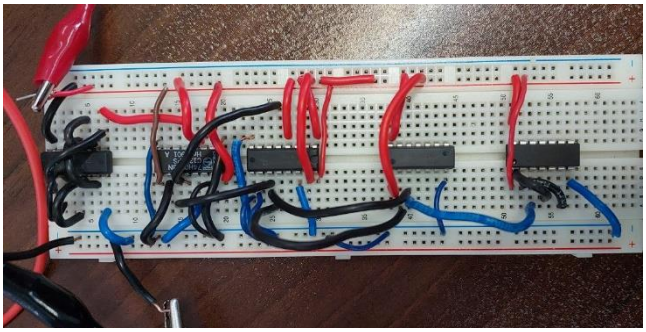

Fig. 14: Circuit of Frequency Divider

E. T Flip-Flop

By converting a D flip-flop to T flip-flop and connect the output of frequency divider to the TFF input we can reach %50 duty cycle in the output.

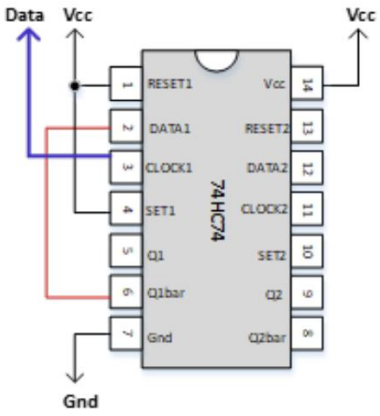

Fig. 15: D flip-flop connection [1]

Using a 74HC74 and wire pin2 and pin6 we will have TFF operation via DFF. At positive edge of clock, Q1bar toggles until next edge. Therefore, we have a %50 duty cycle at the output.

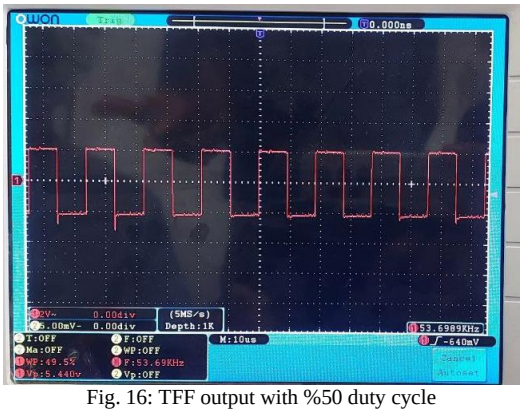

Fig. 16: TFF output with %50 duty cycle

Using a TFF will reduce the frequency up to 50% (from 107.33 KHz to 53.6KHz).

II. CONCLUSIONS

In this experiment, we tried different clock generating methods, by using 74 Series Basic Logic Gates (Inverter, DFF, etc.), Frequency division with counters, And use T flip-flop to generate %50 duty cycle.

As we can see, using more area score leads into better shape of clock cycles and again we reach to point that “There is no free lunch” in hardware design.

III. REFERENCES

[1] Katayoon Basharkhah and Zahra Jahanpeim and Prof. Zain Navabi, *Digital Logic Laboratory*, University of Tehran, Fall 1401.