Computer Assignment #3-Phase 2 – QM Simulation

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In this assignment, QM method is used to minimize assign statements and then a circuit using CA1 is designed.

QM:

An assign expression is passed to this class. This class finds zero cube and strores it in a 3D vector. Then using zero cube, one cube is formed and this process is continued till no other higher cube can be created. Then the terms which were not involved in forming cubes are selected and related terms to them are found. An algorithm finds unique terms and delete relevant terms from other vectors. While the whole vector is clear, this algorithm continues processing.

Gates:

There are and, or and not gates. And and Or gates can have multiple inputs and the gate delay is log2 of number of inputs multiplied by the delay of a 2-input gates.

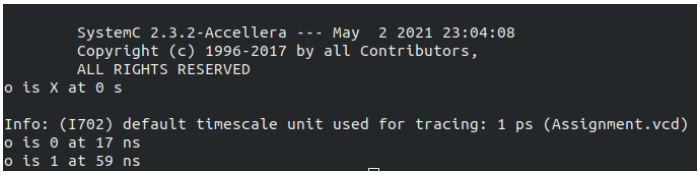
Compiler:

Creates gates from expressions and stores them in logic object.

Logic:

It does the calculations similar to CA1.

SystemC output:



EOST output:

As expected, the results values are the same and there are differences in timings.