UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Object-Oriented Modeling of Electronic Circuits, Spring 1400
Computer Assignment 1, Week 2-3
Gate Level Simulator (Preliminary)

Name:
Date:

You are to write a simple gate-level simulator in C++. This simulator is a line-oriented SystemVerilog gate-level description that only uses **and**, **nand**, **or**, **nor**, and **xor** primitives. The simulator stimuli are specified in a text file with each line specifying an input test value set at a given time, e.g., #17 0010, for 0010 applied to the inputs 17 time units after the previous one. The simulator generates a file similar the input file. The order of the inputs and outputs are as declared in the SV file.

Shown below is an SV file that your simulator accepts as input description. This is followed by a corresponding input stimuli file. Note that timing of input changes is such that the previous stimulus has had enough time to propagate through the entire circuit.

```
module mux (a, b, s, y);
input a;
input b;
input c;
output y;

wire sbar;
wire aa;
wire bb;

nand #(3,5) U1 (sbar, s, s);
nand #(3,5) U2 (aa, a, sbar);
nand #(3,5) U3 (bb, b, s);
nand #(3,5) U4 (y, aa, bb);

endmodule
```

```
#00 000
#21 001
#31 101
#19 010
```