UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Object-Oriented Modeling of Electronic Circuits, Spring 1400
Computer Assignment 4, Week 10-12
RTL and BFM in SystemC

Name:
Date:

The focus of this assignment is on RTL and BFM and the comparison of the two modeling schemes.

RTL SystemC Modeling. Show RTL design and SystemC description of a stack handler that operates on a memory block with 512-word address space and 16-bit word length. The memory has a bidirectional input-output bus, an address bus and appropriate control inputs as described next.

The memory is an SDRAM block with a fixed wait-state of 5 clock cycles. An RTL timer has to be built to generate *memReady* when memory read or write is being done. The SDRAM block has a *clk* input, a *readMem*, and *writeMem* inputs. When *readMem* becomes 1, the addressed data will be read and become available when *memReady* is issued. When *memWrite* becomes 1, data on the memory input bus will be written to the addressed location after elapse of five clock cycles. As in reading, you can use your timer to create the necessary pulse on *memReady*.

The stack handler circuit using this memory has *push*, *pop*, *tos* inputs and *full* and *empty* outputs, as well as a 16-bit *dataIn* input and a 16-bit *dataOut* output. The push operation pushes *dataIn* to the top location of the stack; the pop operation removes the top location of the stack and makes it available on *dataOut*, and the top-of-stack operation reads the top-of-stack without altering the contents of the stack. The *empty* output is asserted when the stack is empty, and the *full* output is asserted when the stack is full.

a. Write the SystemC RTL description of the wait-state timer.
b. Show the datapath of the stack controller, and the way it interfaces with the memory block and the timer.
c. Show the stack handler's controller state diagram.
d. Write SystemC description of the stack handler circuit using its datapath and controller SystemC descriptions.
e. Show the complete SystemC description of the stack handler, its memory, and the wait-state timer. You can use the memory SystemC description from class presentations.
f. Write a testbench for exercising this circuit.

BFM SystemC Modeling.

Write a BFM model of the stack and the wait-state timer described above using functional SystemC constructs. You can use C++ containers and iterators where possible.

a. Write the SystemC BFM description of the stack handler and wait-state timer.
b. Show the complete SystemC description of the combined description of the stack handler – wait-state timer and the stack SDRAM.
c. Write a testbench for exercising the above circuit.
d. In a testbench, instantiate the two descriptions of the complete RTL stack and the BFM stack. Compare the operation of the two circuits.