Computer Assignment #6- System Modeling with CPU and Analog

Amirmahdi Joudi
810197487

2021-07-19

In this assignment, an embedded system is designed with abstract bracketting method and ISS method.

Sensor1FrontEnd:

This is pack of squarewave, sensor1, ADC, converter and register.

Sensor2FrontEnd:

This is pack of squarewave, sensor2, ADC, converter and register.

Timer:

This is what informs CPU of each millisecond passing.

BusInterface:

This is what interconnects processor and other commponents.

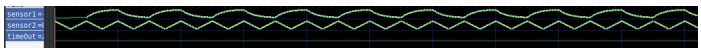
ProcessorBracketting:

This is the program in C.

embSys1:

All components are connected to each other here.

```
Info: (I702) default timescale unit used for tracing: 1 ns (EmbeddedSystem1.vcd)
1000001 ns
0.957397 1.96005e-06
Sensor1: Passed.
Sensor2: Passed.
2000001 ns
0.957397 1.96005e-06
Sensor1: Passed.
Sensor2: Passed.
3000001 ns
0.957397 1.96005e-06
Sensor1: Passed.
Sensor2: Passed.
4000001 ns
0.957397 1.96005e-06
Sensor1: Passed.
Sensor2: Passed.
5000001 ns
0.957397 1.96005e-06
Sensor1: Passed.
Sensor2: Passed.
6000001 ns
0.957397 1.96005e-06
Sensor1: Passed.
Sensor2: Passed.
7000001 ns
0.957397 1.96005e-06
Sensor1: Passed.
Sensor2: Passed.
8000001 ns
0.957397 1.96005e-06
Sensor1: Passed.
Sensor2: Passed.
9000001 ns
0.957397 1.96005e-06
Sensor1: Passed.
Sensor2: Passed.
10000001 ns
0.957397 1.96005e-06
Sensor1: Passed.
Sensor2: Passed.
```



Part 1 Outputs

Now we do what did in last part using ISS:

```
0101000000010001
0101000000010111
0101000000101001
0101111111111100
0110001111111100
0101000110000010
0110111111110010
0101000100010011
0110111111110011
0101000101010100
0110111111110100
0101000111100101
0110111111110101
0010011000010010
0010001000100110
0011011101101000
1111000010000001
1111011000011001
0010111111001110
0010001000111010
0010001001001011
1010101011001101
0010011011010101
1010101111001101
0010011011010101
0010111101011110
```

Instructions

```
ammatti@Joudi:~/Object/CA6/SayacISS$ ./embSys.out

        SystemC 2.3.2-Accellera --- May  2 2021 23:04:08
        Copyright (c) 1996-2017 by all Contributors,
        ALL RIGHTS RESERVED


        SystemC AMS extensions 2.3.0-COSEDA Release date: 20200312 2138
        Copyright (c) 2010-2014  by Fraunhofer-Gesellschaft IIS/EAS
        Copyright (c) 2015-2020  by COSEDA Technologies GmbH
        Licensed under the Apache License, Version 2.0


Info: SystemC-AMS:
        9 SystemC-AMS modules instantiated
        2 SystemC-AMS views created
        6 SystemC-AMS synchronization objects/solvers instantiated


Info: SystemC-AMS:
        2 dataflow clusters instantiated
          cluster 0:
                3 dataflow modules/solver, contains e.g. module: sca_linear_solver_0 containing modules:
                systemTest_TB.s1.s1.vin
                systemTest_TB.s1.s1.r
                systemTest_TB.s1.s1.vout
                systemTest_TB.s1.s1.c

                3 elements in schedule list,
                100 ns cluster period,
                ratio to lowest:  1             e.g. module: sca_linear_solver_0
                ratio to highest: 1 sample time  e.g. module: sca_linear_solver_0
                1 connections to SystemC de, 1 connections from SystemC de
          cluster 1:
                3 dataflow modules/solver, contains e.g. module: systemTest_TB.s2.s2
                3 elements in schedule list,
                100 ns cluster period,
                ratio to lowest:  1             e.g. module: systemTest_TB.s2.s2
                ratio to highest: 1 sample time  e.g. module: systemTest_TB.s2.s2
                1 connections to SystemC de, 1 connections from SystemC de

memReady Ready is X
MEM Ready before  is: X
addrBus   XXXXXXXXXXXXXXXX
data is  0101000000010001
data is  0101000000010111
memReady Ready is X
MEM Ready before  is: X
addrBus   XXXXXXXXXXXXXXXX
data is  0101000000010001
data is  0101000000010111
data is  0101000000101001
data is  0101111111111100
data is  0110001111111100
data is  0101000110000010
data is  0110111111110010
data is  0101000100010011
data is  0110111111110011
data is  0101000101010100
data is  0110111111110100
data is  0101000111100101
data is  0110111111110101
data is  0010011000010010
data is  0010001000100110
data is  0011011101101000
data is  1111000010000001
data is  1111011000011001
data is  0010111111001110
data is  0010001000111010
data is  0010001001001011
data is  1010101011001101
data is  0010011011010101
data is  1010101111001101
data is  0010011011010101
data is  0010111101011110

Info: SystemC-AMS:
        ELN solver instance: sca_linear_solver_0 (cluster 0)
                has 4 equations for 4 modules (e.g. systemTest_TB.s1.s1.vin),
                0 inputs and 1 outputs to other (TDF) SystemC-AMS domains,
                1 inputs and 0 outputs to SystemC de.
                100 ns initial time step

memReady Ready is 0
memReady Ready is 0

Info: (I702) default timescale unit used for tracing: 1 ps (system_Main.vcd)
MEM Ready before IR is:1
Ir IS:    0101000000010001
**************MSI Instruction**************
signEximm is:  0000000000000001
[adr]   1
RegFile Write Data Is:  0000000000000001Time :   10 ns
memReady Ready is 1
MEM Ready before  is: 0
addrBus   ZZZZZZZZZZZZZZZZ
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    0101000000010111
```

```
**************MSI Instruction*************
signEximm is:  0000000000000001
[adr]   7
RegFile Write Data Is:  0000000000000001Time :   50 ns
memReady Ready is 1
MEM Ready before  is: 0
addrBus   ZZZZZZZZZZZZZZZZ
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    0101000000101001
**************MSI Instruction*************
signEximm is:  0000000000000010
[adr]   9
RegFile Write Data Is:  0000000000000010Time :   90 ns
memReady Ready is 1
MEM Ready before  is: 0
addrBus   ZZZZZZZZZZZZZZZZ
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    0101111111111100
**************MSI Instruction*************
signEximm is:  1111111111111111
[adr]   12
RegFile Write Data Is:  1111111111111111Time :   130 ns
memReady Ready is 1
MEM Ready before  is: 0
addrBus   ZZZZZZZZZZZZZZZZ
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    0110001111111100
**************MHI Instruction*************
regFile p1:  1111111111111111
regFile p2:  1111111111111111
[adr]   12
RegFile Write Data Is:  0011111111111111Time :   170 ns
memReady Ready is 1
MEM Ready before  is: 0
addrBus   ZZZZZZZZZZZZZZZZ
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    0101000110000010
**************MSI Instruction*************
signEximm is:  0000000000011000
[adr]   2
RegFile Write Data Is:  0000000000011000Time :   210 ns
memReady Ready is 1
MEM Ready before  is: 0
addrBus   ZZZZZZZZZZZZZZZZ
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    0110111111110010
```

```
**************MHI Instruction*************
regFile p1:  0000000000011000
regFile p2:  0000000000011000
[adr]   2
RegFile Write Data Is:  1111111100011000Time :   250 ns
memReady Ready is 1
MEM Ready before  is: 0
addrBus   ZZZZZZZZZZZZZZZZ
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    0101000100010011
**************MSI Instruction*************
signEximm is:  0000000000010001
[adr]   3
RegFile Write Data Is:  0000000000010001Time :   290 ns
memReady Ready is 1
MEM Ready before  is: 0
addrBus   ZZZZZZZZZZZZZZZZ
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    0110111111110011
**************MHI Instruction*************
regFile p1:  0000000000010001
regFile p2:  0000000000010001
[adr]   3
RegFile Write Data Is:  1111111100010001Time :   330 ns
memReady Ready is 1
MEM Ready before  is: 0
addrBus   ZZZZZZZZZZZZZZZZ
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    0101000101010100
**************MSI Instruction*************
signEximm is:  0000000000010101
[adr]   4
RegFile Write Data Is:  0000000000010101Time :   370 ns
memReady Ready is 1
MEM Ready before  is: 0
addrBus   ZZZZZZZZZZZZZZZZ
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    0110111111110100
```

```
**************MHI Instruction*************
regFile p1:  0000000000010101
regFile p2:  0000000000010101
[adr]   4
RegFile Write Data Is:  1111111100010101Time :   410 ns
memReady Ready is 1
MEM Ready before  is: 0
addrBus   ZZZZZZZZZZZZZZZZ
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    0101000111100101
**************MSI Instruction*************
signEximm is:  0000000000011110
[adr]   5
RegFile Write Data Is:  0000000000011110Time :   450 ns
memReady Ready is 1
MEM Ready before  is: 0
addrBus   ZZZZZZZZZZZZZZZZ
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    0110111111110101
**************MHI Instruction*************
regFile p1:  0000000000011110
regFile p2:  0000000000011110
[adr]   5
RegFile Write Data Is:  1111111100011110Time :   490 ns
memReady Ready is 1
MEM Ready before  is: 0
addrBus   ZZZZZZZZZZZZZZZZ
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    0010011000010010
**************STR Instruction*************
regFile p1:  1111111100011000
regFile p2:  0000000000000001
memReady Ready is 1
MEM Ready before  is: 0
addrBus   1111111100011000
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    0010001000100110
```

```
**************Ldr Instruction*************
regFile p1:  1111111100011000
regFile p2:  1111111100011000
memReady Ready is 1
[adr]   6
RegFile Write Data Is:  ZZZZZZZZZZZZZZZ0Time :   650 ns
MEM Ready before  is: 0
addrBus   1111111100011000
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    0011011101101000
**************ANR Instruction*************
regFile p1:  ZZZZZZZZZZZZZZZ0
regFile p2:  0000000000000001
[adr]   8
RegFile Write Data Is:  0000000000000000Time :   690 ns
memReady Ready is 1
MEM Ready before  is: 0
addrBus   ZZZZZZZZZZZZZZZZ
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    1111000010000001
**************CMR Instruction*************
regFile p1:  0000000000000000
regFile p2:  0000000000000001
flags is:   XXXXXXXXXX00XXXX
memReady Ready is 1
MEM Ready before  is: 0
addrBus   ZZZZZZZZZZZZZZZZ
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    1111011000011001
**************BRR Instruction*************
regFile p1:  0000000000000010
regFile p2:  0000000000000010
Case 1
memReady Ready is 1
MEM Ready before  is: 0
addrBus   ZZZZZZZZZZZZZZZZ
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    0010001000111010
**************Ldr Instruction*************
regFile p1:  1111111100010001
regFile p2:  1111111100010001
memReady Ready is 1
[adr]   10
RegFile Write Data Is:  0000000000000000Time :   850 ns
MEM Ready before  is: 0
addrBus   1111111100010001
memReady Ready is 0
MEM Ready before IR is:1
```

```
**************SUR Instruction*************
regFile p1:  0011111111111111
regFile p2:  0000000000000000
[adr]   13
RegFile Write Data Is:  0011111111111111Time :   970 ns
memReady Ready is 1
MEM Ready before  is: 0
addrBus   ZZZZZZZZZZZZZZZZ
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    0010011011010101
**************STR Instruction*************
regFile p1:  1111111100011110
regFile p2:  0011111111111111
memReady Ready is 1
***********************************
***********************************
Display = Failed
***********************************
***********************************
MEM Ready before  is: 0
addrBus   1111111100011110
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    1010101111001101
**************SUR Instruction*************
regFile p1:  0011111111111111
regFile p2:  1110011001100111
[adr]   13
RegFile Write Data Is:  0101100110011000Time :   1090 ns
memReady Ready is 1
MEM Ready before  is: 0
addrBus   ZZZZZZZZZZZZZZZZ
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    0010011011010101
**************STR Instruction*************
regFile p1:  1111111100011110
regFile p2:  0101100110011000
memReady Ready is 1
***********************************
***********************************
Display = Failed
***********************************
***********************************
MEM Ready before  is: 0
addrBus   1111111100011110
memReady Ready is 0
MEM Ready before IR is:1
Ir IS:    0010111101011110
**************JMI Instruction*************
signEximm is:  1111111111110101
[adr]   14
RegFile Write Data Is:  0000000000011010Time :   1210 ns
```