In the name of God

University of Tehran

College of Engineering

School of Electrical and Computer Engineering

Computer Assignment 1

Communication Circuits

Dr. kamarei

Amirmortaza Rezaee

810101429

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Part 1:

1) Inductor Simulation:

The given inductor has been placed in a circuit with a current probe like the one below:

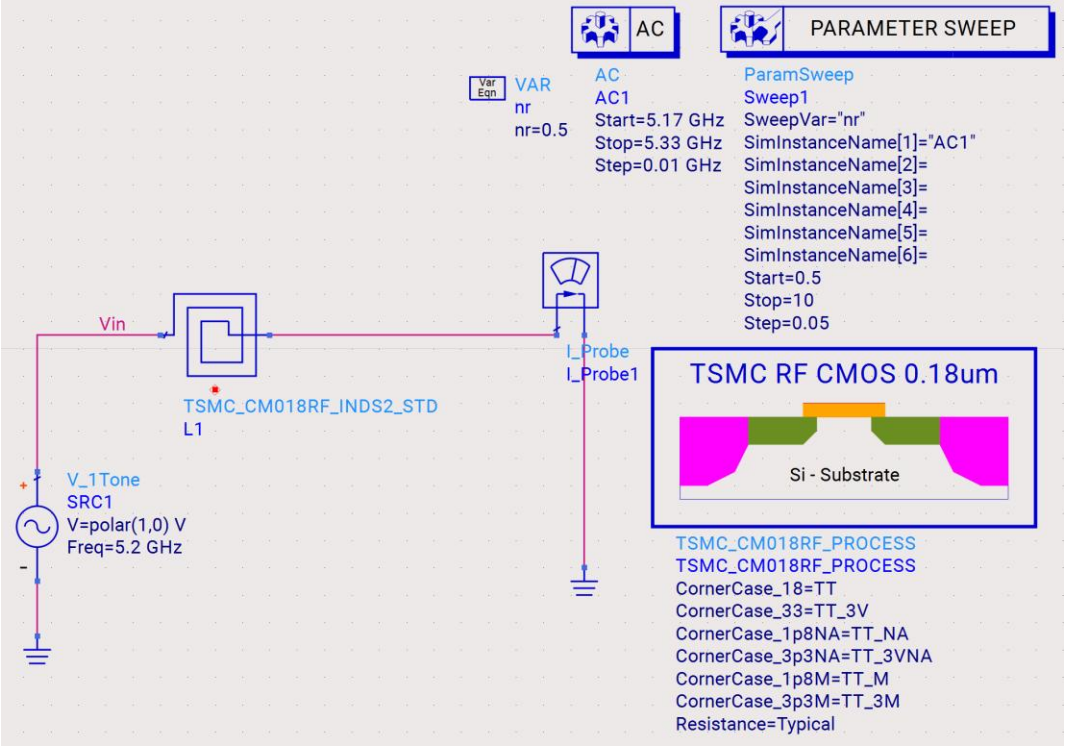

Figure 1. Simulating the TSMC inductor

Having the equations:

$$Z_L = \frac{V_L}{I_L}, \qquad Q = \frac{Im\{Z_L\}}{Re\{Z_L\}}$$

The Q Vs. nr diagram is plotted in the given frequency range:

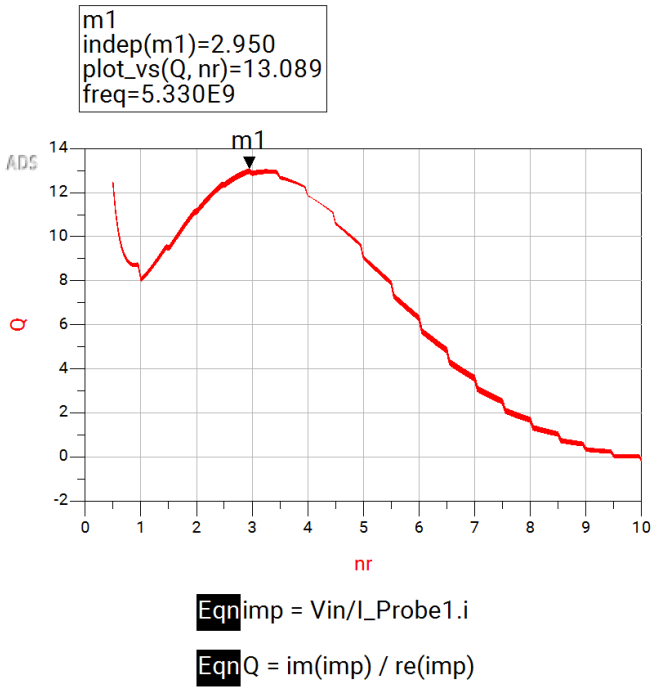

Figure 2. Quality favroe Vs. Nr diagram

As it's observable, the number of turns in which the most quality factor occurs, is 2.950, and the best quality factor we can reach in this frequency range, is 13.089.

As we know, each real-world inductor can be modeled with an ideal inductor in series with a resistor, which can be transferred into a circuit contains the same ideal inductor in parallel with some resistance following the coming equations:

$$L_p \approx L_s$$

$$R_p \approx \frac{{L_s}^2 \cdot \omega^2}{R_s}$$

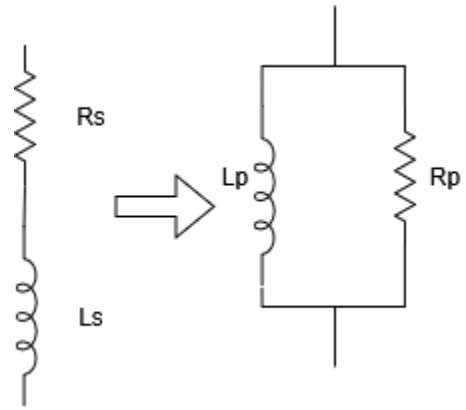

Figure 3. Transmission of series resestor to a parallel resistor for the real-wold inductor

The resistor in the series model, is equal to by the real part of the impedance; also, the value of inductance is derived by dividing the imaginary part of the impedance to the angular velocity. Given the equations the values of the inductance and the resistance in the parallel model are plotted in the diagram below:

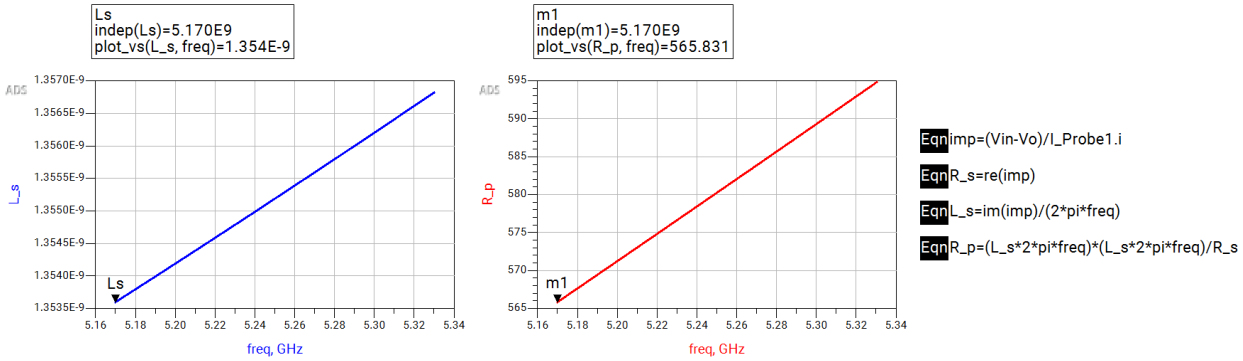

Figure 4. Inductance and equivalent parallel resistor for the simulated inductor

2) NMOS Transistors Simulation:

Putting a NMOS in a bias circuit, fixing its source and gate voltage, we swept the voltage of the drain and plotted the drain current Vs. its voltage.

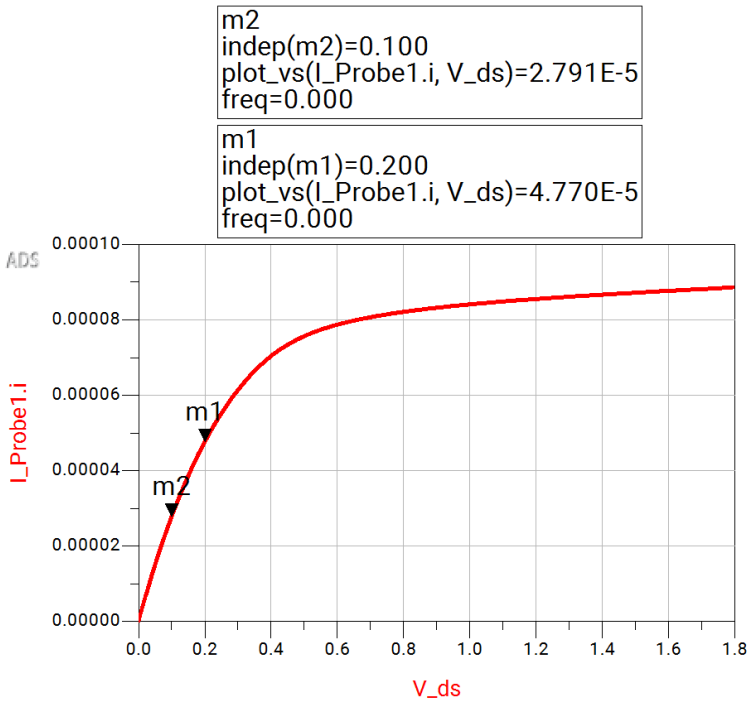

Figure 5. Id Vs. Vd diagram for the simukated NMOS transistor

The drain current in the triode region is given by:

$$i_D = \mu_n C_{ox}\left(\frac{W}{L}\right)\left((v_{GS} - V_t) - \frac{1}{2}v_{DS}\right)\cdot v_{DS}$$

So, solving for two points in the triode region, we'll have:

$$\left.\begin{aligned} 4.770 \times 10^{-5} &= \mu_n C_{ox}\big((1.3 - V_t) - 0.1\big) \times 0.2 \\ 2.791 \times 10^{-5} &= \mu_n C_{ox}\big((1.3 - V_t) - 0.05\big) \times 0.1 \end{aligned}\right\}$$
$$\rightarrow \begin{cases} V_t = 0.906281 \\ \mu_n C_{ox} = 812 \times 10^{-6} \end{cases}$$

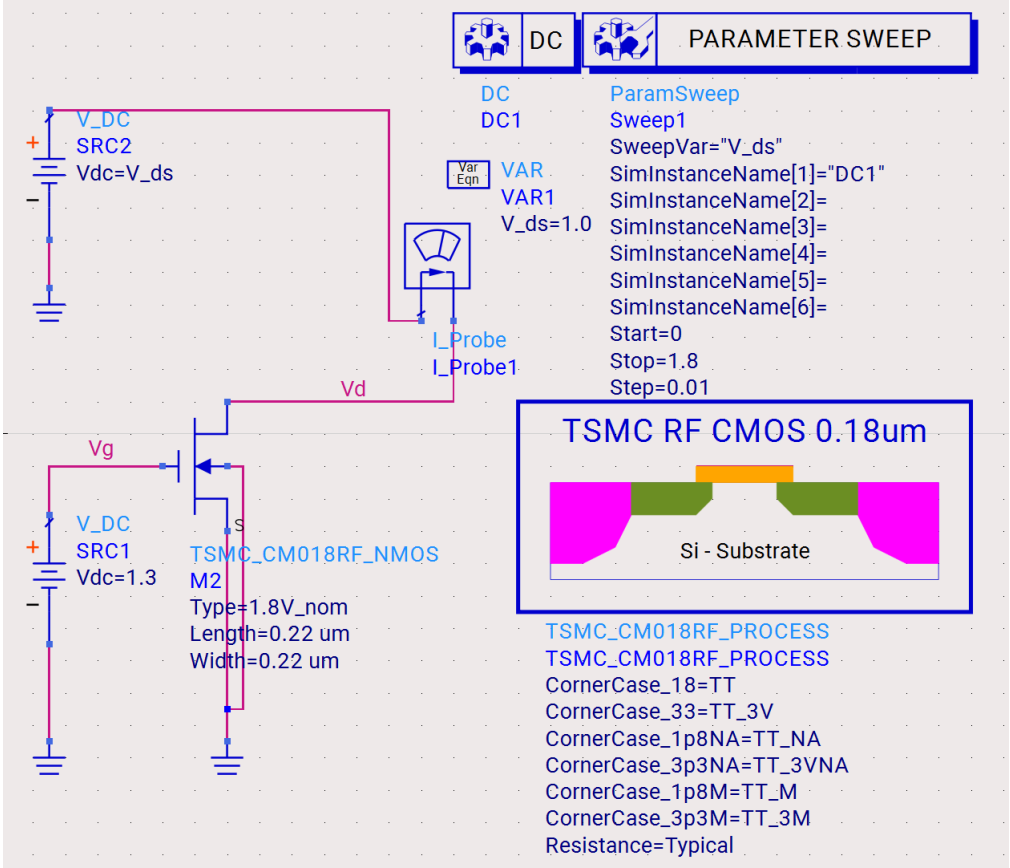

Figure 6. circuit diagram to find NMOS's charactristics

3) Capacitors specifications:

After inserting 3 capacitors in the circuit as it was described on the question, the trial-and-error method was used to find the capacitances that matches the best. The TSMC capacitors were used in this part.

4) Circuit Biasing and Testing:

A 1.8 V DC voltage source and two 1 mA current sources are used for the biasing of the circuit; and also, a 1 V initial condition is given to the Gates of the transistors. The final Schematic is shown in the figure below:

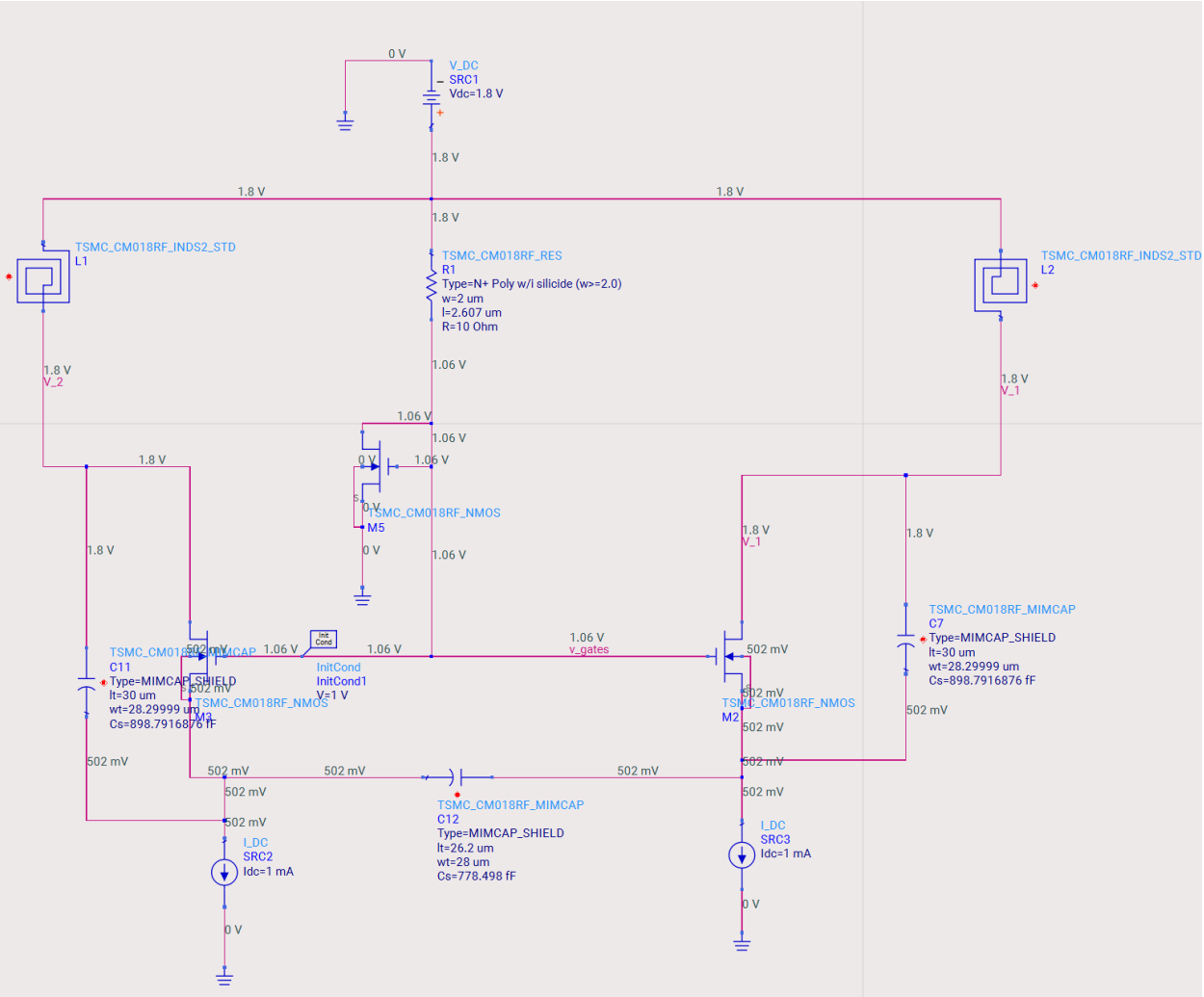

Figure 7. Oscillator's biasings and components' values

The simulation result is shown in the figure below:

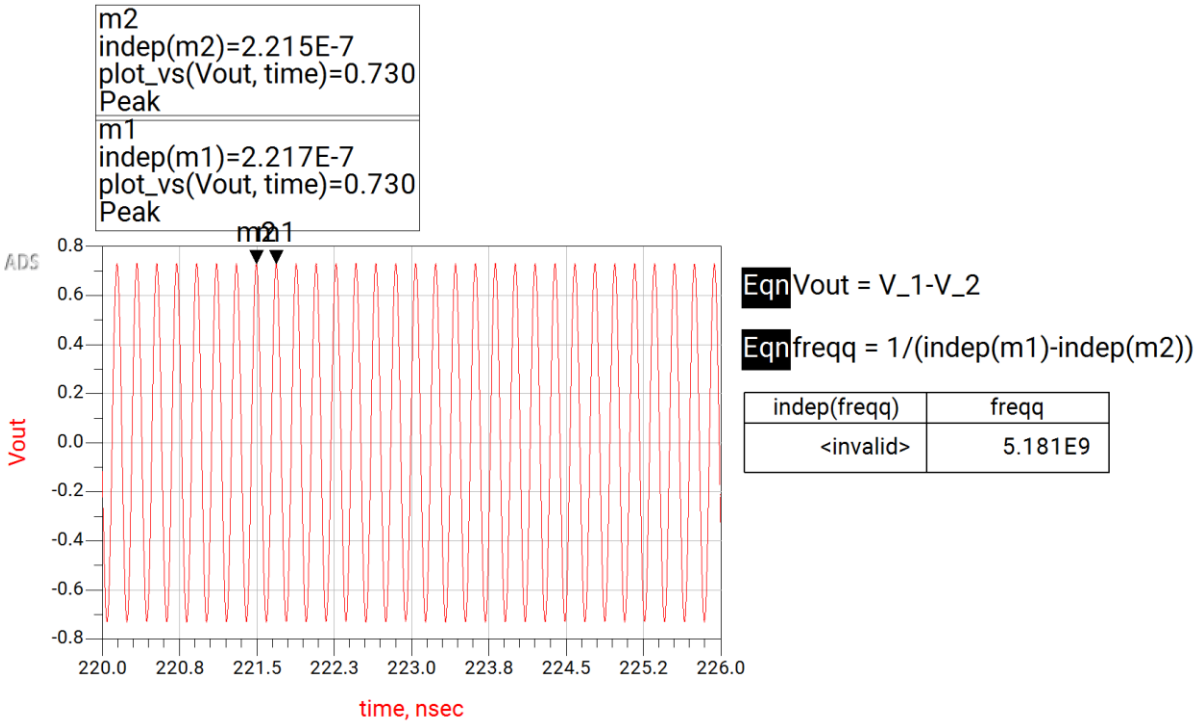

Figure 8. Oscillator's output and its frequency measurment

As it's obvious, the oscillation frequency is 5.18 GHz.

Part 2:

1) Diode Varactor Simulation:

Using the circuit below and the equations provided on the figure, the capacitance of the diode varactor is measured for different values of the bias voltage.

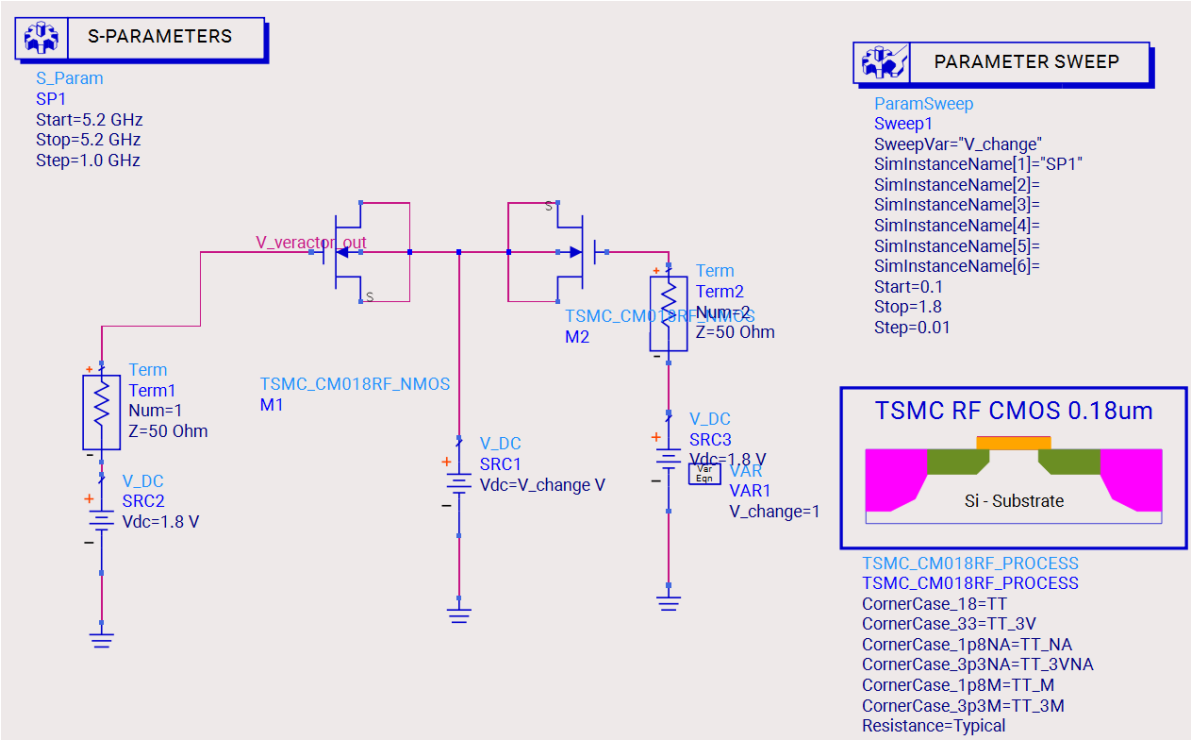

Figure 9. The circuit designe to find Diode Varactor's charactristics

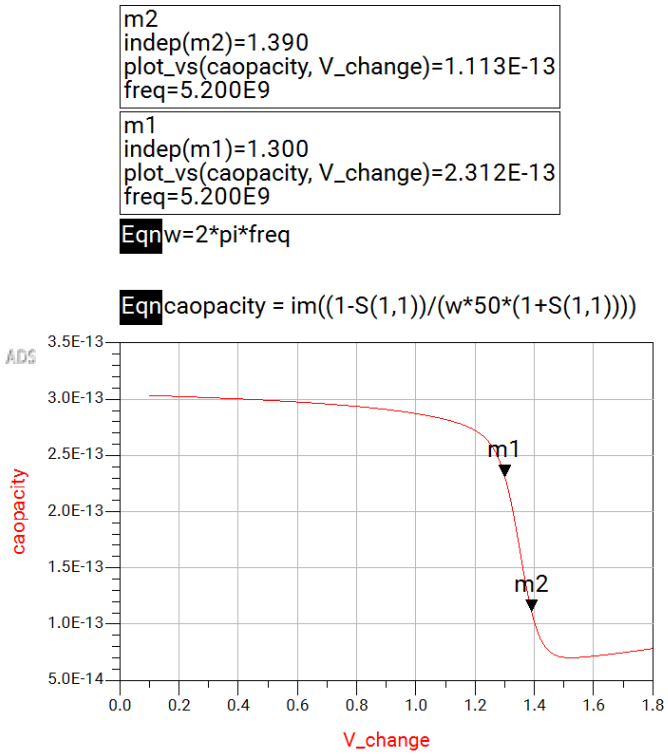

Figure 10. Capacitance of the Diod Varactor Vs. the biasing voltage

As shown in the figure, the region between m1 and m2 (from 111 fF to 231 fF) can be considered linear.

2) Adding diode varactor to the circuit:

Tuning was applied on the capacitor that connects sources, and it was observed that the minimum frequency (5.18 GHz) occurred on the capacitance of 778 fF, and the maximum frequency (5.32 GHz) occurred on the capacitance of 700 fF. So, it can be concluded:

$$700 = C_{const} + C_{varactor_{min}} \rightarrow 700 = C_{const} + 111 \rightarrow C_{const} \approx 667\ fF$$

So, after adding the Diode Varactor to the circuit, and making necessary changes to the capacitors, the circuit will look like the figure below:

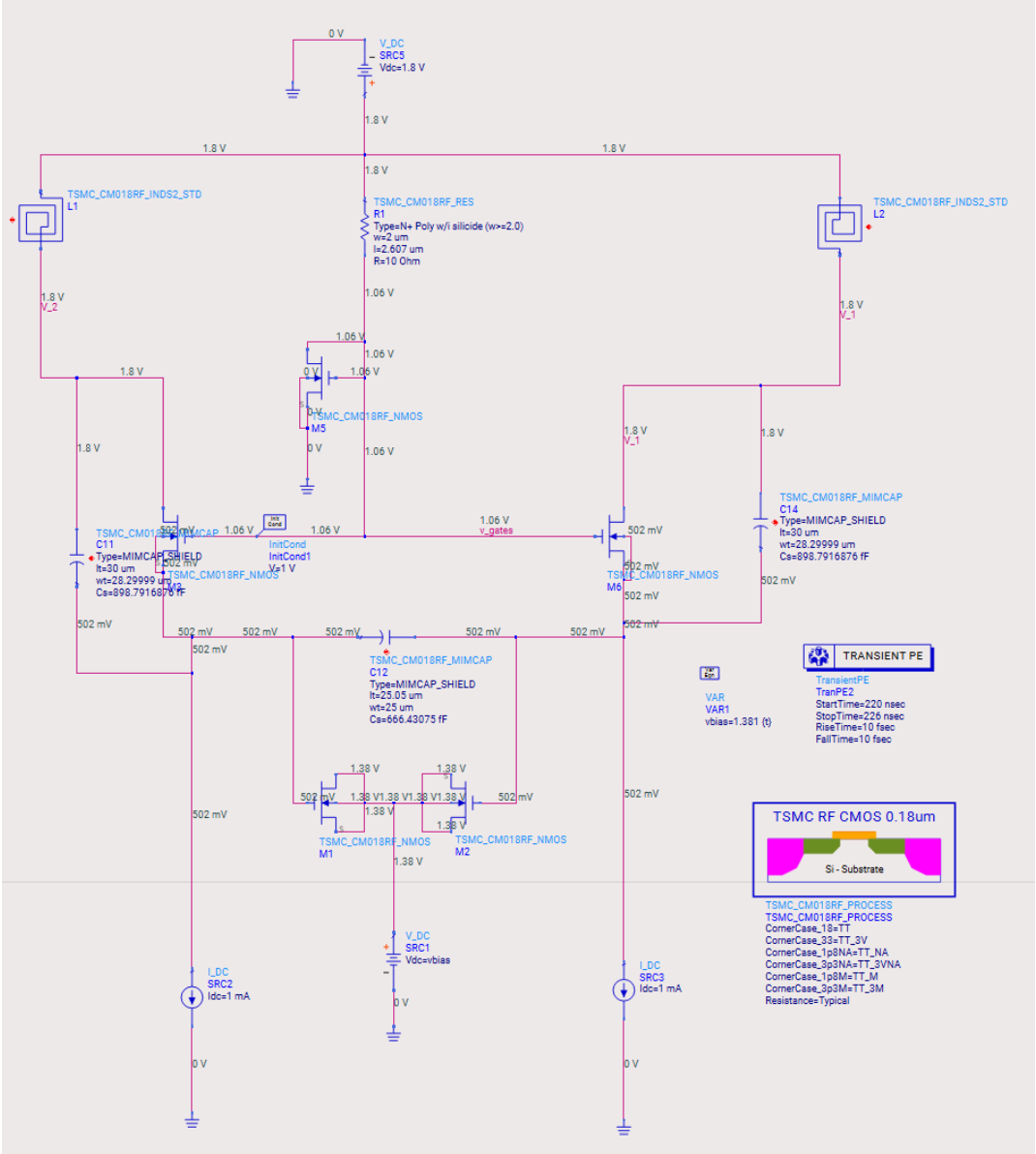

Figure 11. The oscillators circuit containing the diode varactor

The simulation results for 2 different bias voltages are shown in the figures below:

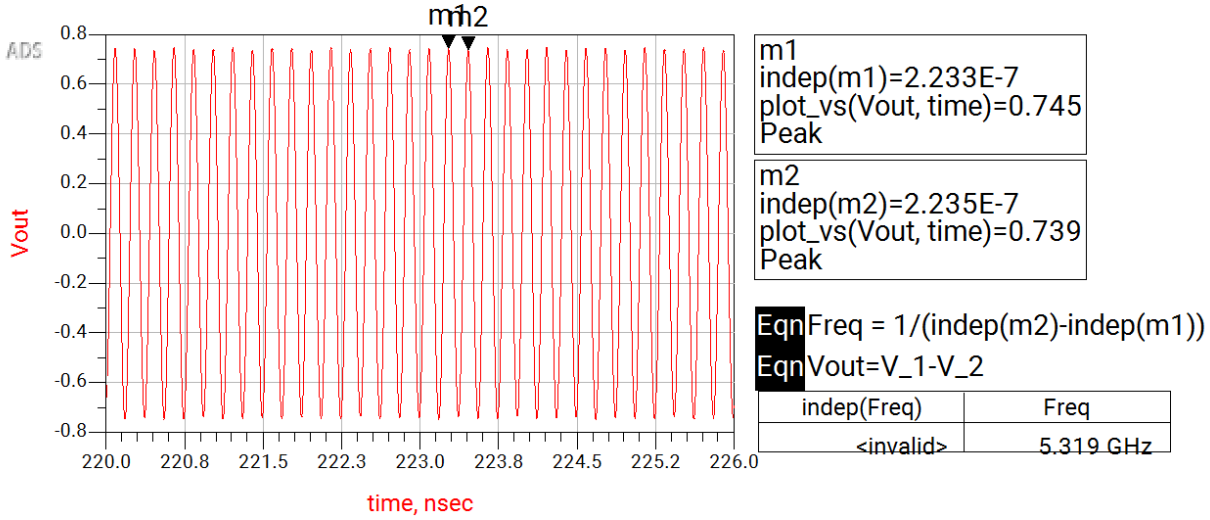

Figure 12. Output voltage and the frequency of the oscillating circuit with diode varactor, Vb = 1.3 V

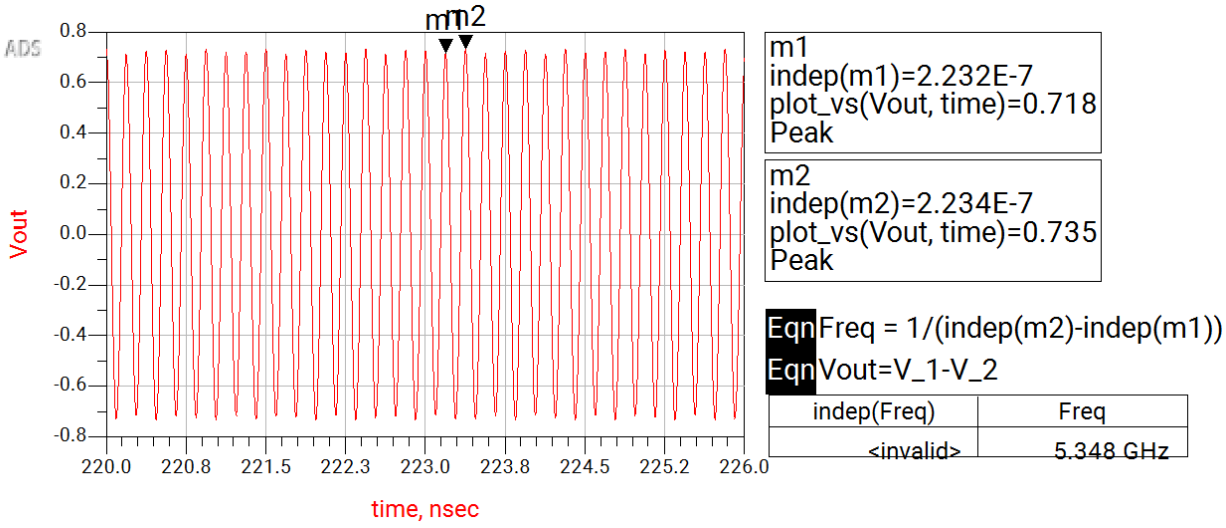

Figure 13. Output voltage and the frequency of the oscillating circuit with diode varactor, Vb = 1.39 V

Part 3:

Designing a Current Mirror:

for a MOSFET current mirror like the circuit below,

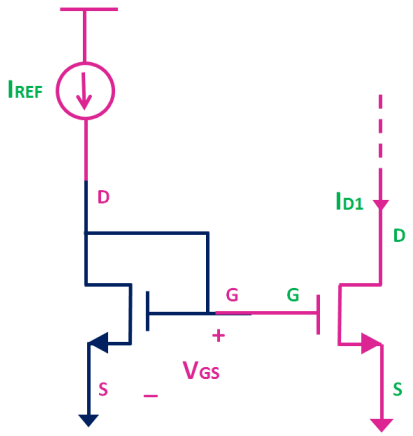

Figure 14. Current mirror sample

We have:

$$I_{D1} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_{REF}} = I_{REf}$$

So, the circuit for this part is designed like the figure below:

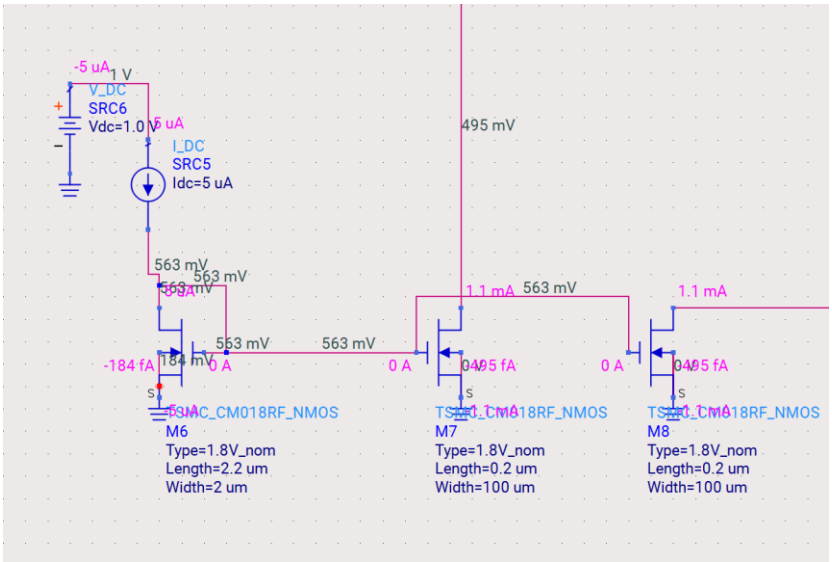

Figure 15. designed current mirror circuit using the TSMC model

The output will be look like:

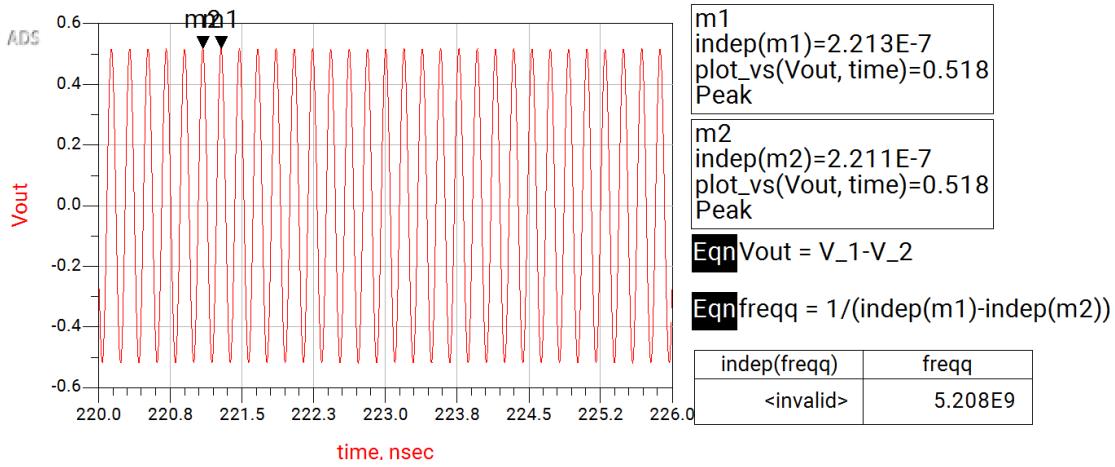

Figure 16. Output and the frequency of the Oscillator biased with a current mirror

Part 4:

Harmonic Balance Simulation:

After adjusting the settings for the Harmonic Balance Simulation, the result is plotted as shown in the figure below:

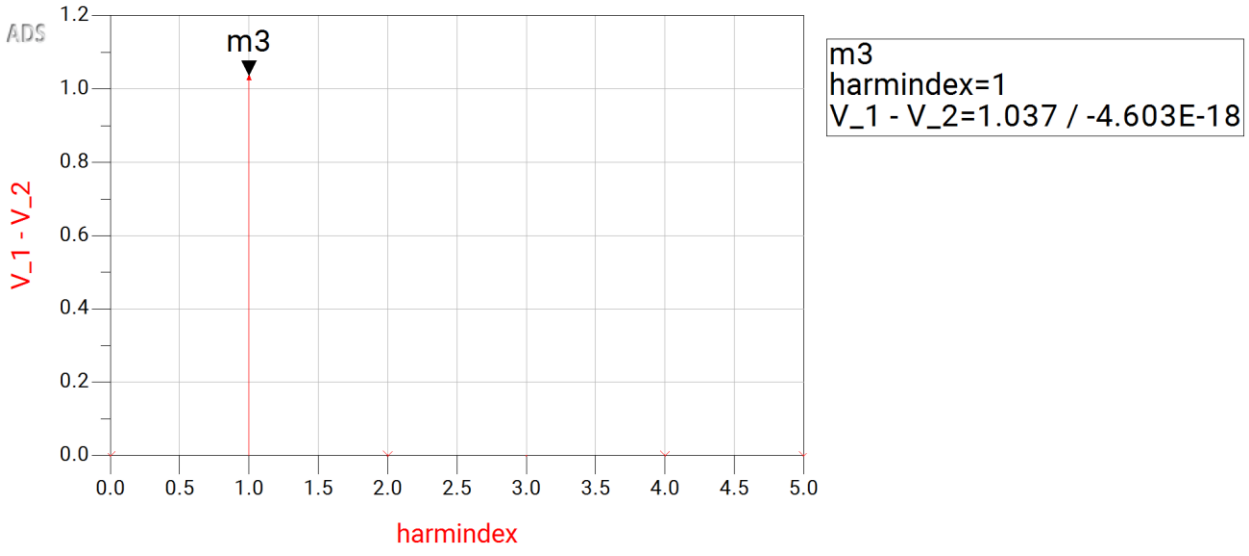

Figure 17. Harmonic Balance's result

As it's obvious, the only harmonic we got is the main one, so the system is designed perfectly!