In the name of God

University of Tehran

College of Engineering

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Computer Assignment 2

Communication Circuits

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1) Biasing the system:

In order to bias the transistors, the gate of the transistor "M1" was connected to a 0.8 V source and a current mirror that was fed by a 0.17 mA current source. Also, the gate of the transistor "M2" was connected to a 1.8 V source. The NMOS device chosen for the current mirror has the width and the length of 1.8 and 0.18 microns respectively.

2) Circuit design:

The NMOS devices are chosen with width of 0.72 microns and length of 0.18 microns.

Having the equation below, the gate source capacitor for main transistors can be calculated:

$$C_{gs_1} = \frac{2}{3} C_{ox} \times W \times L = \frac{2}{3} \times 6 \times \frac{10^{-15}}{10^{-12}} \times 0.72 \times 10^{-6} \times 0.18 \times 10^{-6}$$
$$= 5.184 \times 10^{-16} F$$

The gate source capacitor of the transistor used in current mirror can be calculated as:

$$C_{gs_2} = \frac{2}{3} C_{ox} \times W \times L = \frac{2}{3} \times 6 \times \frac{10^{-15}}{10^{-12}} \times 1.8 \times 10^{-6} \times 0.18 \times 10^{-6}$$
$$= 1.296 \times 10^{-15} F$$

The current in the drain is calculated as follows:

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left(V_{gs} - V_{th}\right)^2 \approx 70\ \mu A$$

So, we have:

$$g_m \sqrt{2 \times \mu_n C_{ox} \frac{W}{L} \times I_D} \approx 0.000411047 \frac{A}{V}$$

The total capacitance observed from the input can be ensued by parallelizing the two of the gate-source capacitors:

$$C_{total} = C_{gs_1} + C_{gs_2} \approx 18.144 \times 10^{-16}\ F$$

The inductors can be derived by the equations below:

$$L_s = \frac{R_s \cdot C_{total}}{g_m} \approx 2.207 \times 10^{-10}\ H$$

$$L_g = \frac{1}{\omega_0^2 \cdot C_{total}} - L_s \approx 2.32559 \times 10^{-6}\ H$$

The values of L_{OM} and C_{OM} should satisfy the equation below:

$$\omega_0 = \frac{1}{\sqrt{L_{OM} \cdot C_{OM}}}$$

So, setting the inductance to 150 nano Henries, led us to set the capacitor to 28.133 femto Farads.

3) Computer design:

Wiring up the system will result in the figure below:

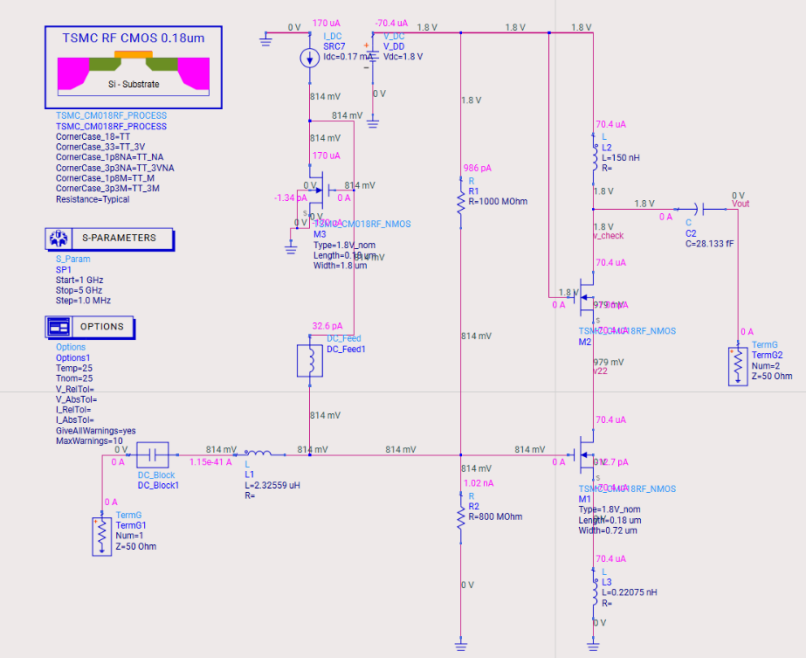

Figure 1. System's schematic in ADS

As it is obvious, a current mirror was used in order to bias the circuit. Also, an "OPTIONS" block is for setting the temperature to a desired value.

Please note that there might be some incompatibilities among the system we've designed and the one which was implemented using ADS; and this is in the result of the fact that some neglectable capacitors were excluded in the hand-driven values!

4) Simulation:

The results of S-param simulation of the system are shown in the plots below:

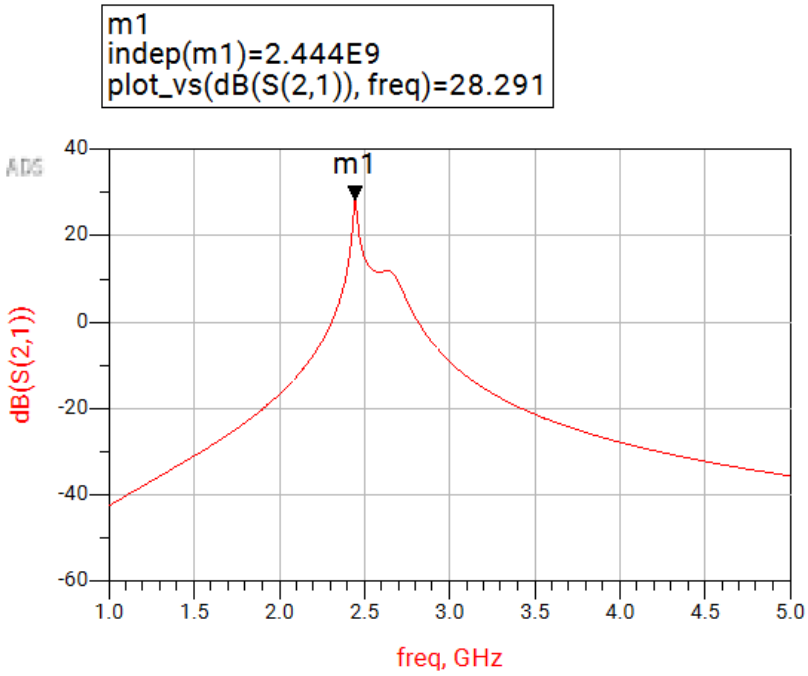

Figure 2. S_2,1 simulation result

Intelligibly, the gain of the system that is equivalent to the s_{21}, is about 28.291 dBs which satisfies the project's wanted.

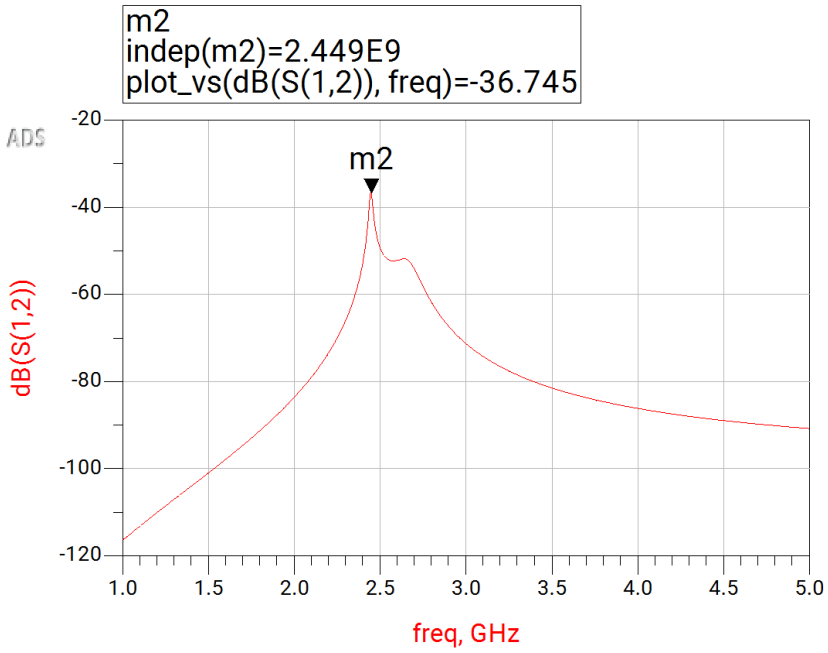

Figure 3. S_1,2 simulation result

Also, the reverse isolation of the system (s_{12}) is around -36 dBs in the working frequency of the circuit; which satisfies our need.

The noise figure (nf) and the minimum Noise Figure are listed for different frequencies. The figure below indicates them in our working frequency range:

2.430 GHz	0.136	2.420 GHz	20.256	9.804
2.440 GHz	0.137	2.430 GHz	20.221	9.695
2.450 GHz	0.137	2.440 GHz	20.517	9.585
2.460 GHz	0.138	2.450 GHz	21.071	9.474
2.470 GHz	0.138	2.460 GHz	21.784	9.362
2.480 GHz	0.139	2.470 GHz	22.573	9.249
2.490 GHz	0.140	2.480 GHz	23.379	9.136
2.500 GHz	0.140	2.490 GHz	24.168	9.022
2.510 GHz	0.141	2.500 GHz	24.923	8.908
2.520 GHz	0.141	2.510 GHz	25.636	8.793

Figure 4. Noise Figures

5) Output and results:

Total power can be calculated by multiplying the voltage in the current of each source.

$$P_{total} = V \cdot I$$
$$= 1.8 \times (70.4 \times 10^{-6} + 986 \times 10^{-12})$$
$$+ (0.17 \times 10^{-3} \times 814 \times 10^{-3}) = 265\,\mu W$$

Note that all simulations were done in the $25℃$, and the noise was set in both S-param and HB simulations in ads.