**In the name of God**

University of Tehran

College of Engineering

School of Electrical and Computer Engineering

# Computer Assignment 3

## Communication Circuits

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# Table of Contents

# Table of Figures

## عنوان مقاله انتخابی

طراحی، شبیه‌سازی و ساخت تقویت‌کننده توان کلاس E پهن‌باند با کنترل هارمونیکی مرتبه دوم و سوم و تکنیک جبران راکتانس دوگانه؛ نویسندگان: اکرم شیخی و علی سجادی

# Introduction

Modern communication systems such as WCDMA, OFDM, LTE, and CDMA2000 demand high-efficiency power amplifiers with good linearity to ensure low power consumption, smaller battery size, and reduced cost. Achieving these requirements, especially wide bandwidth and high data rates, is critical. Among various amplifier classes, Class-E is particularly suitable for microwave circuit design due to its simple structure and high efficiency. First introduced by Sokal in 1972, several methods have since been developed to extend its bandwidth and improve performance. Harmonic control and dual-reactance compensation techniques have been employed in Class-E designs for satellite communications in the UHF band, particularly using GaN transistors. A key challenge in broadband amplifier design is impedance matching across a wide frequency range, which is often addressed with additional output networks—though these may increase circuit size and losses. Recent approaches use dual-reactance compensation without extra networks to simplify design and enhance efficiency. In this study, a Class-E power amplifier is designed with second and third harmonic control circuits and dual-reactance compensation, aiming for broad bandwidth and improved efficiency, especially suited for satellite communication applications.

# Circuit Analysis

## Basic Relations

The schematic diagram of the proposed Class-E power amplifier circuit and its equivalent at the fundamental frequency $f_0$ are shown in Figure 1. At frequency $f_0$, the resonators $L_0 - C_0$ and $L_1 - C_1$ behave as resonant circuits. At frequency $2f_0$, the $L_1 - C_1$ resonator acts like a capacitor and resonates with inductor $L_2$, functioning as a short circuit branch. Similarly, at $3f_0$, the $L_0 - C_0$ resonator behaves like an inductor and resonates with capacitor $C_0'$, forming another short circuit branch at $f_0$.

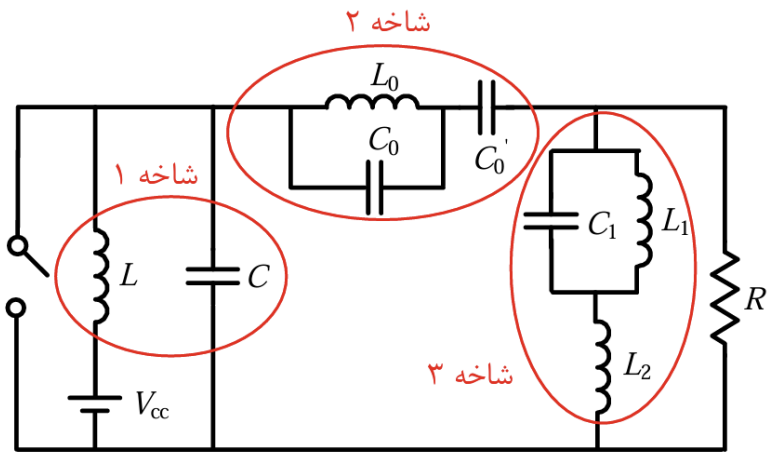


*Figure 1. shows the schematic of the proposed Class-E power amplifier*

The analysis under Class-E zero-voltage switching (ZVS) and zero-voltage derivative switching (ZVDS) conditions uses the following relations:

$$v(t) = 0 \quad \text{at} \quad \omega t = \pi$$

$$\frac{\mathrm{dv(t)}}{\mathrm{dt}} = 0 \quad \text{at} \quad \omega\, \mathrm{t} = \pi$$

These conditions ensure high drain efficiency due to the absence of voltage and current overlap, as shown in Figure 2.

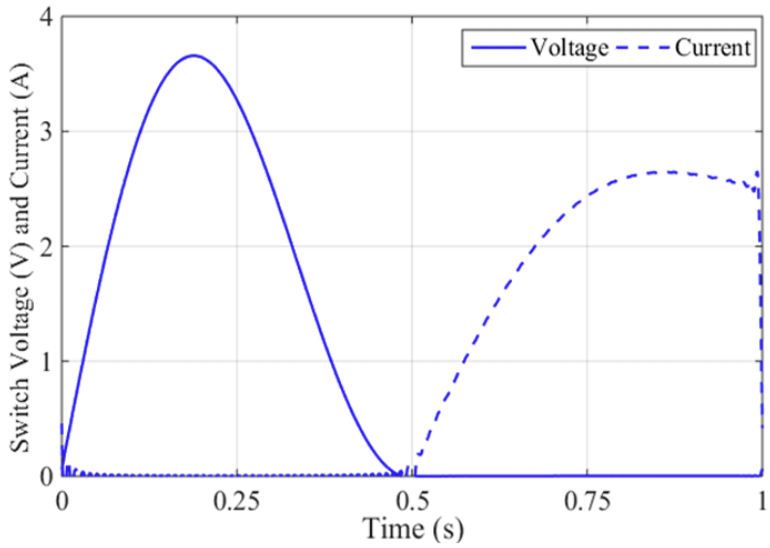


*Figure 2. Ideal voltage and current waveforms of the proposed Class-E power amplifier*

The power of the load network at the fundamental frequency $f_0$, from the drain of the transistor, is calculated as:

$$\tan\phi = \frac{R}{\omega L} - RC\omega$$

To implement dual-reactance compensation with second- and third-order harmonic control, the input admittance of the load network is computed.

Let's denote:

- Branch 1: $L_1 - C_1$
- Branch 2: $L_2$ in parallel with capacitors $C_0$ and $C_0'$

Their impedances are:

$$Z_0 = \frac{jL_0\omega(a)}{1 - \omega^2 C_0 C_0' b + j\omega(C_0 + C_0')}$$

$$Z_1 = \frac{1}{j\omega C_1 - \frac{1}{j\omega L_1}}$$

Where:

$$\omega' = \frac{\omega^2 - \omega_0^2}{\omega}$$

$$a = L_0C_0 + L_0C_0' \quad , \qquad b = L_0C_0$$

The admittance of the load network is:

$$Y_{net} = j\omega C_1 + \frac{1}{j\omega L_1 + Z_A}$$

Where $Z_A$ is:

$$Z_A = \frac{Z_1 Z_2}{Z_1 + Z_2 + R}$$

And:

$$Z_2 = j\omega L_2 + \frac{1}{j\omega C'}$$

By substituting these equations, we get:

$$Z_A = \frac{R(LC_0 a\omega^2 - 1)}{(1 - \omega^2 LC_0') + j\omega RC_0}$$

$$\mathrm{Im}(Z_A) = \frac{RC_0\omega(mD - p)}{p^2 + q^2}$$

Where:

$$p = m\,C\,D\,\omega - 1$$

$$q = m\,D\,\omega$$

$$m = \omega^2 LC'$$

$$D = \frac{a\omega^2 - b}{C_0}$$

For dual-reactance compensation, the susceptance component $B$ of the network must satisfy:

$$\frac{dB}{d\omega} = 0 \quad , \qquad \frac{d^3B}{d\omega^3} = 0$$

By using admittance of the load network and applying conditions mentioned above, we obtain:

$$C + \frac{1}{\omega_0^2 L} - \frac{8C_1 C_0' R^2\omega_0^2 - 9}{4C_0' R^2\omega_0^2} = 0$$

$$\frac{6}{\omega_0^4 L} + \frac{C_1^2}{C_0'\omega_0^2}\cdot\left(\frac{243}{32} + \frac{93}{2}\right) + \frac{359}{8}C_1^3 L_2^2\omega_0^2 + \frac{6C_1}{\omega_0^2} + \frac{C_1}{C_0^2 R^2\omega_0^4}\cdot\left(\frac{729}{4} + \frac{243}{32}\right) + \frac{2187}{432}\frac{1}{C_0^3 R^4\omega_0^6} = 0$$

## Calculation of component values

At $f_0$, the parallel resonator $L_1 - C_1$ is used. From:

$$L = \frac{2}{\omega^2 C}$$

$$C = \frac{1}{\omega^2 L}$$

By substituting:

$$L_2 = \frac{L_1}{3}$$

At $3f_0$, the branch with $L_0 - C_0$ and $C_0'$ behaves as a short circuit, giving:

$$L_X = \frac{L_0}{1 - \omega^2 L_0 C_0}$$

$$C_0' = \frac{1}{\omega^2 L_X}$$

Substituting into:

$$C_0' = \frac{8}{9} C_0$$

Finally, with supply voltage $V_{DD}$ and output power $P_{out}$, optimal element values are:

$$R = \frac{0.732L}{\omega}$$

$$C = \frac{0.685}{R\omega}$$

$$P_{out} = \frac{(V_{DD} - V_{sat})^2}{1.365R}$$

# Simulation Results

## proposed power amplifier

The schematic of the proposed Class-E power amplifier has been simulated using ideal and actual component models in ADS software. The schematics were all wired up in the same way as it was mentioned in the paper. The results were compared in the figures below:

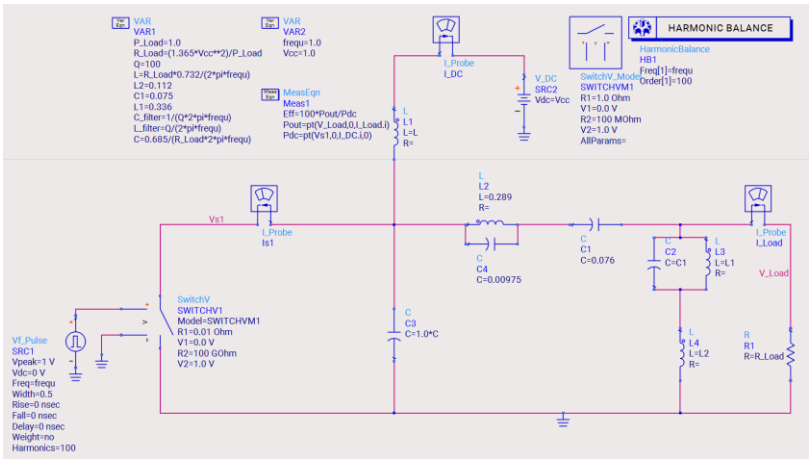


*Figure 3. Schematic diagram of the proposed Class-E power amplifier with ideal switch*

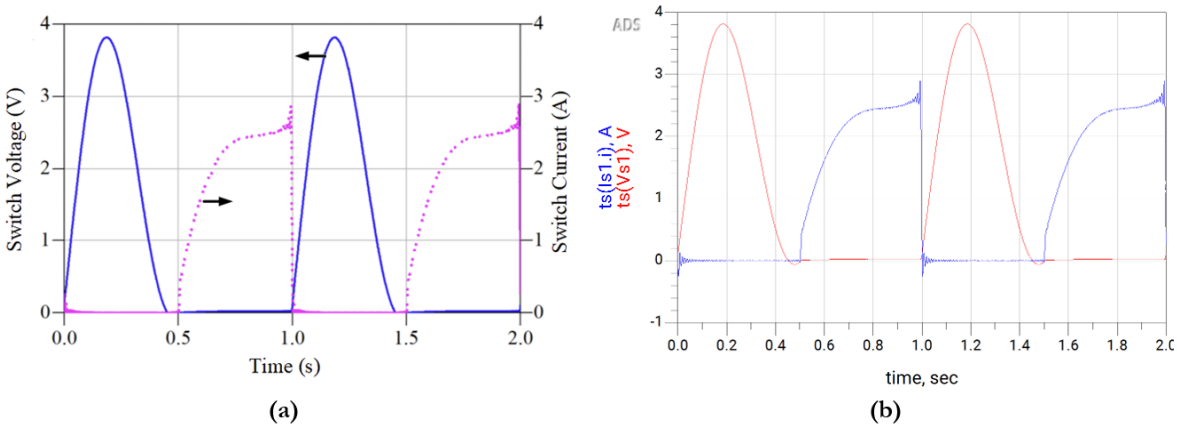


*Figure 4. voltage and current waveforms **(a)** waveforms mentioned in the original paper **(b)** waveforms resulted from my simulations*

As it's obvious, results out of the simulations match to the ones mentioned in the original paper.

## Proposed load network

The load network is designed based on the relationships presented in the previous section, and its impedance is shown in Figure 5. This network is also wired up in the same way as it was mentioned in the paper.

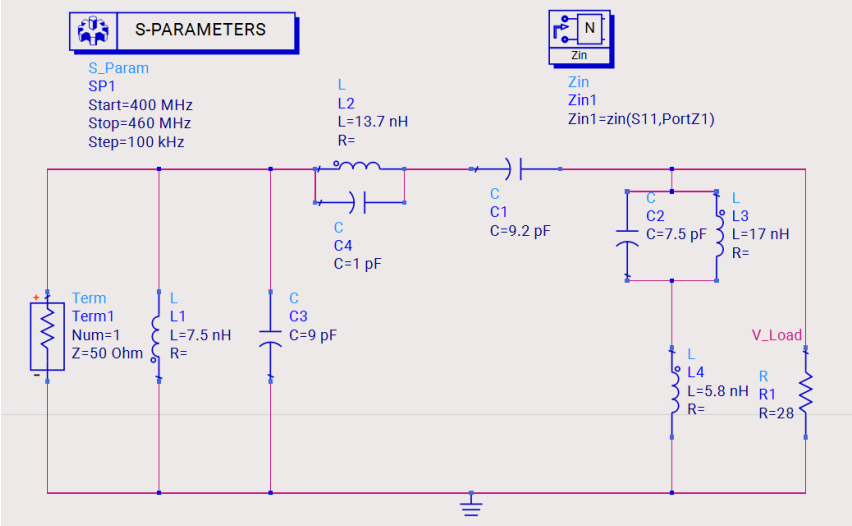


*Figure 5. Proposed load network*

According to what author indicated in Figure 6(a), the proposed load network has an impedance magnitude of approximately $23\Omega$ and a phase angle of about $34°$ over the frequency range of 400 MHz to 460 MHz. In contrast, simulations of mine, indicates an impedance magnitude of approximately $18\Omega$ and a phase angle of about $38°$ over this frequency range as shown in Figure 6(b).

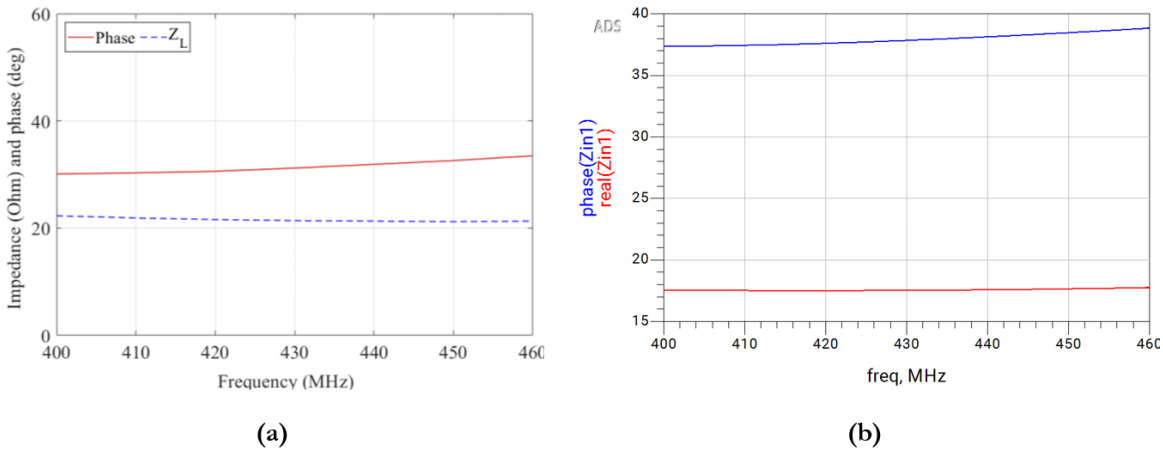


*Figure 6. Load network impedance magnitude and phase versus frequency* ***(a)*** *mentioned in the original paper* ***(b)*** *resulted from my simulations*

## proposed amplifier with real components

The actual circuit of the proposed amplifier was simulated using real component models, and the schematic is shown in the figure below. The components used in simulation and final implementation include ATC600S series capacitors, Coilcraft inductors, and the AFT09MS007N LDMOS transistor from NXP, which is suitable for wideband applications in the 136–941 MHz range with 7 W output power. All design and simulation steps were based on a Rogers RO4003C substrate with a dielectric constant of 3.55 and thickness of 0.508 mm. This substrate was selected due to its favorable electrical characteristics, such as low signal loss and better impedance and thermal control. To match the RF input to the transistor's input impedance (typically $50\Omega$), an RLC input matching network was added. This includes a 69.8 Ω resistor and a 30-pF shunt capacitor at the transistor gate, which improves stability.

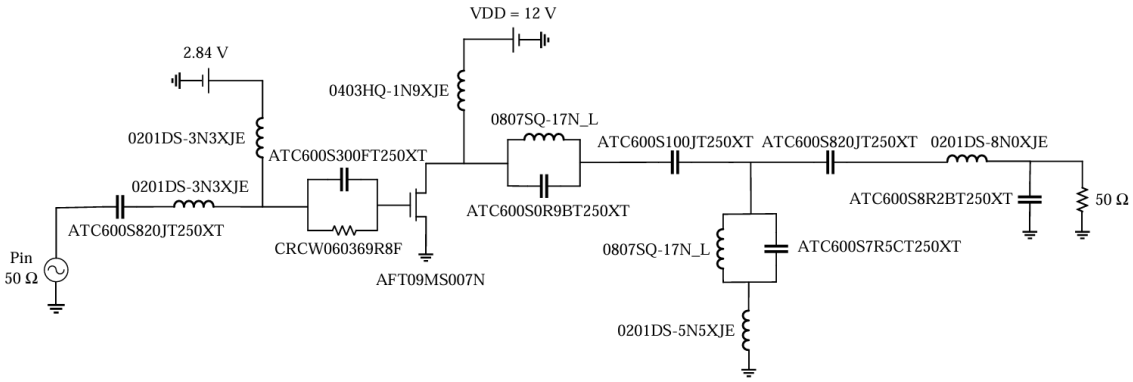


*Figure 7. Schematic of the proposed amplifier with real components*

Since the remaining simulations require specific component libraries, and with the approval of the Chief TA (Mr. Kazazi), those simulations were not performed.