UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Systems I, ECE 894, Spring 1403
Computer Assignment 3
Combinational RTL Design, Simulation, and Synthesis
Week 11-12

Name:
Date:

A 16-bit ALU is to be designed. Table below lists functions that the ALU can perform and their corresponding opcodes. Inputs are 16-bit signed integers. The ALU inputs are data *inM[15:0]*, *inN[15:0]*, carry input *inC*, and the 3-bit opcode *opc[2:0]*. The ALU signed outputs are *outF[15:0]*, and flag outputs zero (*zer*), and negative (*neg*). The output, *outF*, is defined as shown in the table below, *zer* becomes 1 when the ALU output is 16'b0, and *neg* becomes 1 when the ALU result is negative.

In this computer assignment, you are to generate a behavioral description of the ALU, perform pre-synthesis simulation, synthesize, perform post-synthesis simulation, compare simulation results, and report hardware used by Yosys synthesis tool. You will then do the hardware design of the ALU and share hardware components for the implementation of several ALU operations. You will come up with a SystemVerilog description that corresponds to your hardware-oriented design, perform pre-synthesis simulation, synthesize, perform post-synthesis simulation, compare simulation results, and report hardware used by Yosys synthesis tool. At the end, you will compare the timing and gate utilization of behavioral and the hardware-oriented descriptions of the ALU.

1. Write a behavioral description of the ALU given below in SystemVerilog. Use an **always** statement that encloses a **case** statement. Use a **case-choice** for each of the opcodes of the ALU given in the table below.
    a. Simulate the ALU and verify its operations. Use **$random** and **repeat** statements in the testbench where possible.
    b. Synthesize the description of the ALU using Yosys and using the provided target library. Manually verify the netlist. Report gates used in the netlist.
    c. Perform post-synthesis simulation on the netlist obtained from Yosys.
    d. Compare simulation results of Part a and Part c. Start with the testbench you used in Part a. Evaluate simulation speed of the two descriptions (Bonus).

2. Design the ALU manually at the structural level. Use packages discussed in class and share hardware components for the implementation of several ALU operations. You will come up with a SystemVerilog description that corresponds to your hardware-oriented design.
    a. Simulate the above hardware-oriented ALU description and verify its operations. Use **$random** and **repeat** statements in the testbench where possible.
    b. Synthesize the description of the ALU using Yosys and using the provided target library. Manually verify the netlist. Report gates used in the netlist.

c. Perform post-synthesis simulation on the netlist obtained from Yosys.
d. Compare simulation results of Part a and Part c in terms of hardware used. Start with the testbench you used in Part a. Evaluate simulation speed of the two descriptions (Bonus).

3. Write a one paragraph report, along with related diagrams, discussing and comparing simulation and synthesis results of the above two problems in terms of pre-synthesis and post-synthesis.

Opcode	**Function**
000	outF = inM + inN + inC
001	outF = inM + inN÷2.0
010	outF = MAX (inM, inN)
011	outF = inM × 3
100	outF = inM & inN (Bitwise)
101	outF = inM | inN (Bitwise)
110	outF = ~inM (Bitwise)
111	No operation

Deliverables:

Generate a report that includes all the items below:

A. For all the above problems hand-drawn schematic diagrams and partial timing diagrams are required. Your SystemVerilog descriptions must correspond to the circuit diagrams. Your simulation run and the project built for this purpose must be demonstrated to the TA. Show Yosys reports to the TA and be able to justify the hardware used.
B. For Problem 3, your report should include images of the Yosys synthesis report, simulation screen-shots and partial waveforms. Be prepared to answer questions asked about the timing and gate counts of the various circuits in these problems.

Make a PDF file of your report and name it with the format shown below:

FirstinitialLastnameStudentnumber-CAnn-ECEmmm

Where *nn* is a two-digit number for the Computer Assignment, *mmm* is the three-digit course number under which you are registered, and hopefully you know the rest. For the *Firstinitial* use only one character. For *Lastname* and for the multi-part last names use the part you are most identified with. Use the last five digits of your student id (exclude 8101) for the *Studentnumber* field of the report file name.