UNIVERSITY OF TEHRAN
Electrical and Computer Engineering Department
Digital Logic Design, ECE 367 / Digital Systems I, ECE 894
Spring 1402-03
Computer Assignment 5
State Machines and Basic RTL
Quartus Pre- and Post-Layout Simulation

Name:	**Date:**
Username:	

In this assignment, you will design a sequential divider. The algorithm used is very similar to the sequential shift-and-add multiplier that was done in class.

Datapath and Controller of an RTL Design. Restoring Division Algorithm for Unsigned Integer. One of the slow division algorithms is the restoring division algorithm for unsigned integers. The term "restoring" refers to the fact that the value of register A is restored after each iteration. In this algorithm, register Q contains the quotient, and register A contains the remainder. The n-bit dividend is loaded into register Q, and the divisor is loaded into register M. The value of register A is initially set to 0, and this is the register whose value is restored during each iteration, hence the name "restoring". The circuit has a start input and a ready output. A complete pulse on start starts the division operation.

The algorithm procedure is as follows:

Step-1: First the registers are initialized with corresponding values (Q = Dividend, M = Divisor,
A = 0, n = number of bits in dividend).
Step-2: The contents of register A and Q are shifted left as if they are a single unit.
Step-3: The content of register M is subtracted from A and result is stored in A. (A=A-M)
Step-4: The most significant bit of the A is checked and if it is 0, the least significant bit of Q is set to 1 otherwise if it is 1 the least significant bit of Q is set to 0 and value of register A is restored i.e., the value of A before the subtraction with M.
Step-5: The value of counter n is incremented.
Step-6: If the value of n becomes 7, we get of the loop otherwise we repeat from step 2.
Step-7: Finally, the register Q contains the quotient and A contains remainder.

In this problem you are to design an 8-bit Restoring Divider at the RT level.

a. Show the RTL schematic of the datapath for the divider.
b. Show the controller for the divider.
c. Write VHDL description for the datapath.
d. Write VHDL description for the Huffman controller.
e. Simulate circuit datapath in ModelSim.
f. Simulate the circuit Control Unit in ModelSim.
g. Perform synthesis of the circuit in Quartus.

h. Perform pre-and post-synthesis simulation.
i. Using a testbench examine the pre-synthesis RTL description of the divider along side with its post-synthesis netlist.

Simulation:

a. Using state machines, counters, shift-registers and other RTL components discussed in class show the design of the divider circuit.
b. In a SystemVerilog module describe the datapath of this circuit and simulate it and test it independently.
c. In a SystemVerilog module describe the control unit of this circuit and simulate it and test it independently.
d. Wire the datapath and control unit together and test you design of the divider.

Netlist Synthesis (basic gates target):

a. Take the entire divider circuit module into Quartus and synthesize it to Cyclone IV E FPGA.
b. Run Verilog simulation to verify the operation of the pre-synthesis and post-synthesis descriptions.

Synthesis and post-synthesis simulation (FPGA target):

c. Take the entire divider module into Quartus, synthesize it and generate a symbol for it.
d. Instantiate the divider within a top-level Quartus Block Diagram, and connect the input output pins.
e. Synthesize the circuit you generated in Quartus to generate .vo and .sdo files.
f. Add the post-synthesis output of the previous part to the testbench you generated for the simulation part and run the same simulations to compare the results.
g. Verify timing and operation of the post-synthesis output.

Deliverables:

A complete report containing answers to all parts of each question. Your report should include enough design illustration, description, actual data, and output justification. Note that your reports should be well-organized.

Attention:

Make a *PDF* file of your report and submit it to the course site. Also, compress all files and documents mentioned in the *Deliverables* section into a *zip* file and upload the generated file. The name of the zip file must be in this format "***YourFirstName-YourLastName-HW45***". In addition, use exactly this phrase "***Submitting HW#45***" as the subject of your email.