

REVISION HISTORY

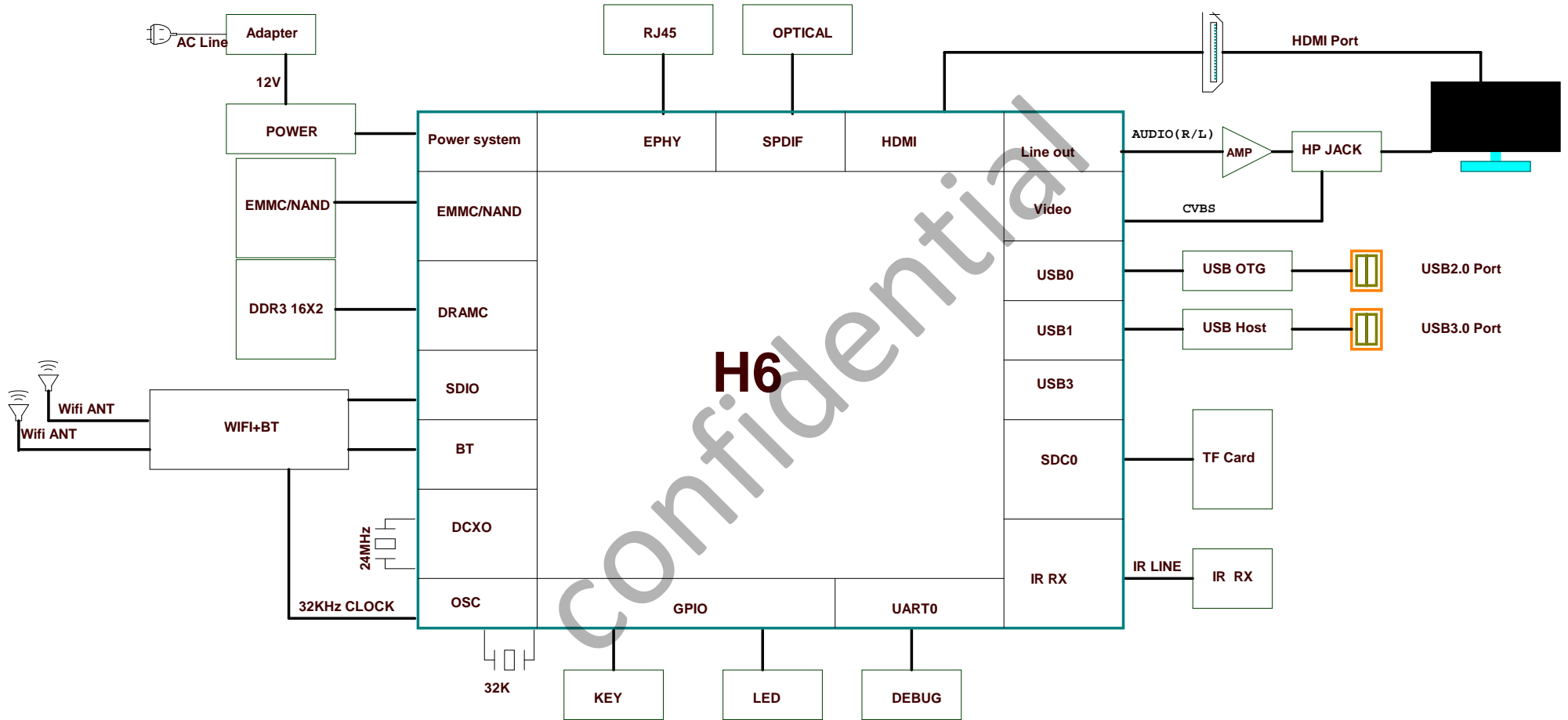
Schematics Index:

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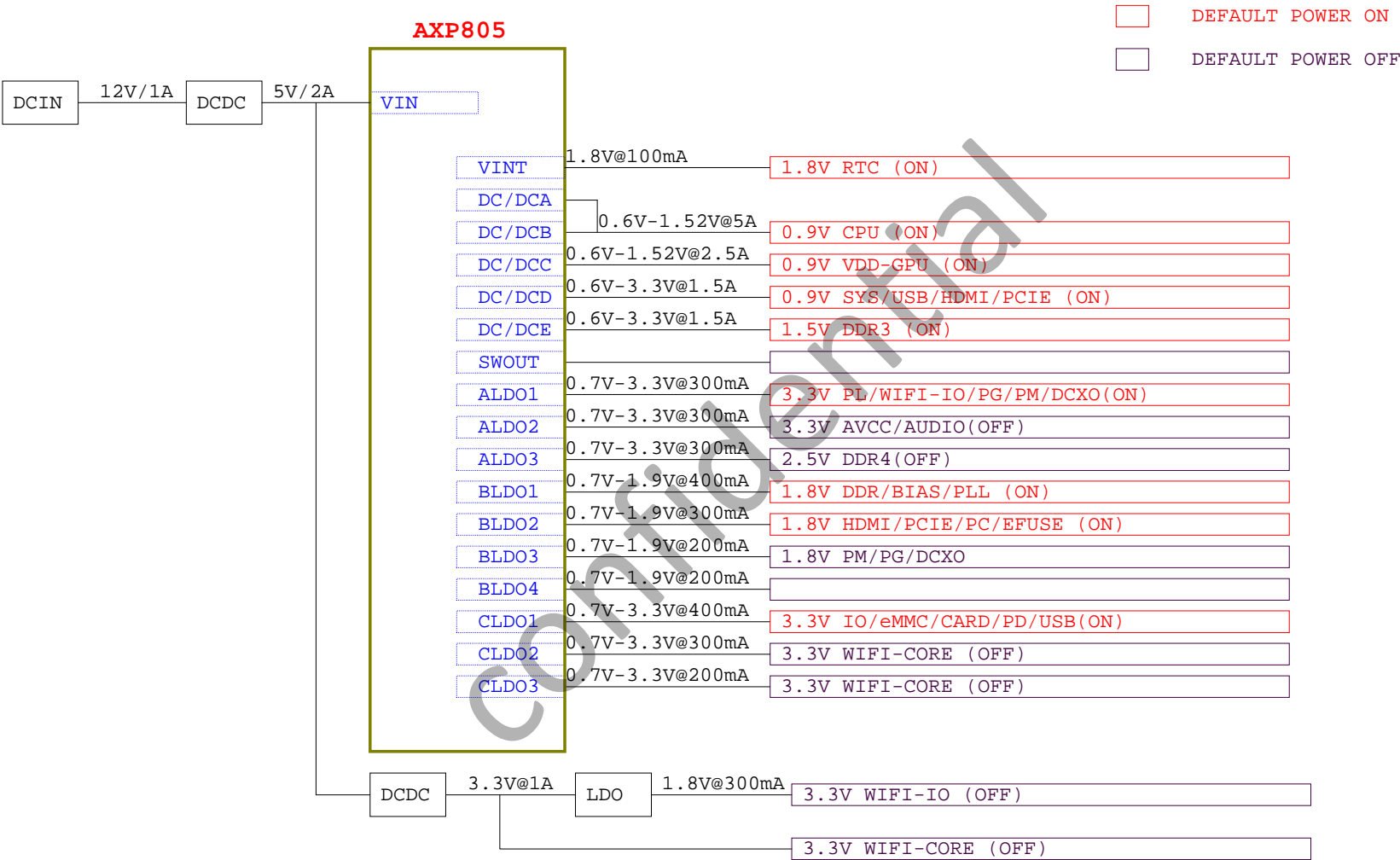
- OPTION:
- P07: DDR3 16X4
 - P07: DDR4 16X2
 - P07: LPDDR3

Revision	Description	Date	Drawn	Checked
Ver 0.5	Initial Version	2016-12-26	HJ	
Ver 0.9		2017-04-10	HJ	
Ver 1.0		2017-07-06	HJ	

Confidential



POWER TREE



GPIO ASSIGNMENT

PIN	Define	CFG	Function
PC0	NAND_WE	2	NAND/eMMC
PC1	NAND_ALE/SDC2_DS	2/3	
PC2	NAND_CLE	2	
PC3	NAND_CE0	2	
PC4	NAND_RE/SDC2_CLK	2/3	
PC5	NAND_RB0/SDC2_CMD	2/3	
PC6	NAND_DQ0/SDC2_D0	2/3	
PC7	NAND_DQ1/SDC2_D1	2/3	
PC8	NAND_DQ2/SDC2_D2	2/3	
PC9	NAND_DQ3/SDC2_D3	2/3	
PC10	NAND_DQ4/SDC2_D4	2/3	
PC11	NAND_DQ5/SDC2_D5	2/3	
PC12	NAND_DQ6/SDC2_D6	2/3	
PC13	NAND_DQ7/SDC2_D7	2/3	
PC14	NAND_DQS/SDC2_RST	2/3	
PC15	NAND_CE1	2	
PC16	NAND_RB1	2	

PIN	Define	CFG	Function
PD0	RGMII-RXD3	5	
PD1	RGMII-RXD2	5	
PD2	RGMII-RXD1	5	
PD3	RGMII-RXD0	5	
PD4	RGMII-RXCK	5	
PD5	RGMII-RXCTL	5	
PD6			
PD7	RGMII-TXD3	5	
PD8	RGMII-TXD2	5	
PD9	RGMII-TXD1	5	
PD10	RGMII-TXD0	5	
PD11	RGMII-TXCK	5	
PD12	RGMII-TXCTL	5	
PD13	RGMII-CLKIN	5	
PD14			

PIN	Define	CFG	Function
PD15			
PD16			
PD17			
PD18			
PD19	MDC	5	
PD20	MDIO	5	
PD21	RGMII-RESET	1	
PD22			
PD23			
PD24			
PD25			
PD26			

PIN	Define	CFG	Function
PG0	SDC1_CLK	2	WIFI+BT
PG1	SDC1_CMD	2	
PG2	SDC1_D0	2	
PG3	SDC1_D1	2	
PG4	SDC1_D2	2	
PG5	SDC1_D3	2	
PG6	UART1_TX	2	
PG7	UART1_RX	2	
PG8	UART1_RTS	2	
PG9	UART1_CTS	2	
PG10	PCM2_SYNC	2	
PG11	PCM2_CLK	2	
PG12	PCM2_DOUT	2	
PG13	PCM2_DIN	2	
PG14			

PIN	Define	CFG	Function
PF0	SDC0_D1	2	CARD0
PF1	SDC0_D0	2	
PF2	SDC0_CLK/UART0_TX	2/3	
PF3	SDC0_CMD	2	
PF4	SDC0_D3/UART0_RX	2/3	
PF5	SDC0_D2	2	
PF6	SDC0_DET	2	

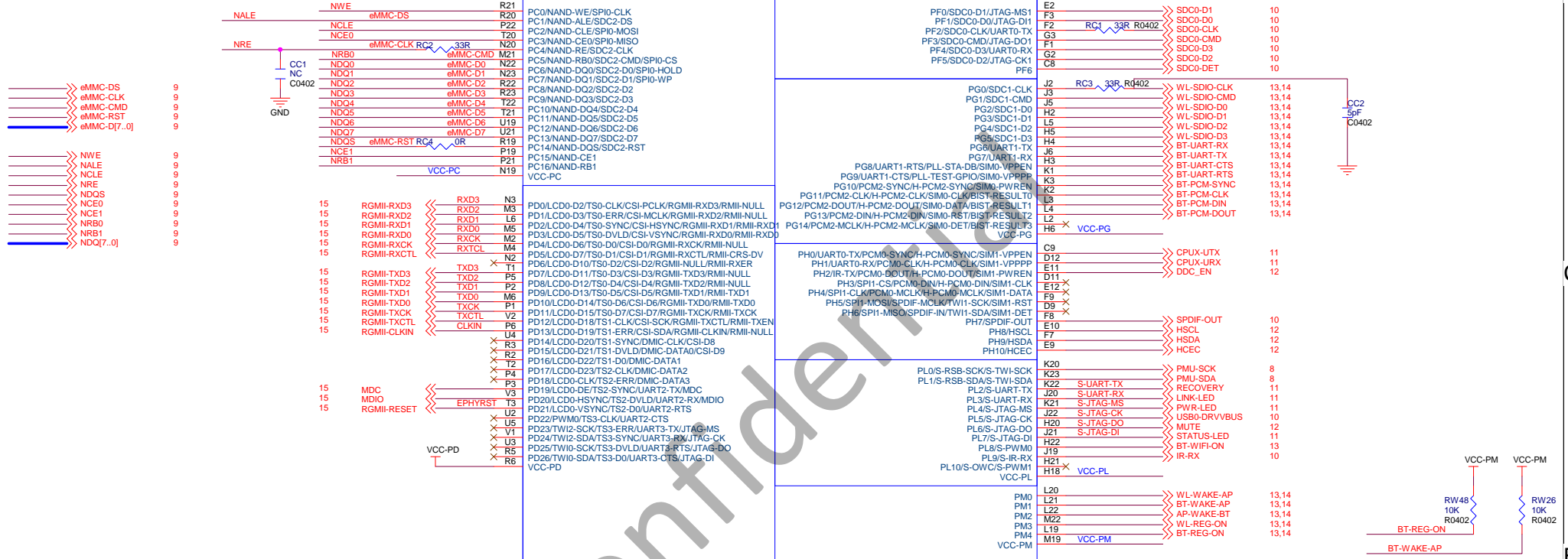
PIN	Define	CFG	Function
PH0	CPUX-UTX	2	
PH1	CPUX-URX	2	
PH2	DDC_CEC_EN	6	
PH3			
PH4			
PH5			
PH6			
PH7	SPDIF_OUT	3	
PH8	HSCL	2	
PH9	HSDA	2	
PH10	HCEC	2	

PIN	Define	CFG	Function
PL0	PMU-SCK	3	WIFI+BT
PL1	PMU-SDA	3	
PL2	RECOVERY	6	
PL3	LINK-LED	1	
PL4	PWR-LED	1	
PL5	USB0-DRVVBUS	1	
PL6	MUTE	1	
PL7	STATUS-LED	1	
PL8	BT-WIFI-ON	1	
PL9	IR-RX	2	
PL10			
PM0	WL-WAKE-AP	6	
PM1	BT-WAKE-AP	6	
PM2	AP-WAKE-BT	1	
PM3	WL-REG-ON	1	
PM4	BT-REG-ON	1	

PC, PD, 部分IO口不具备中断功能
PF, PG, PH, PL, PM, 部分IO口有中断功能

D

D



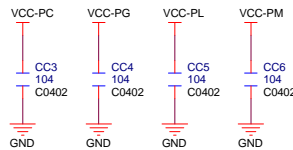
B

B

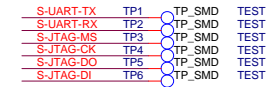
A

A

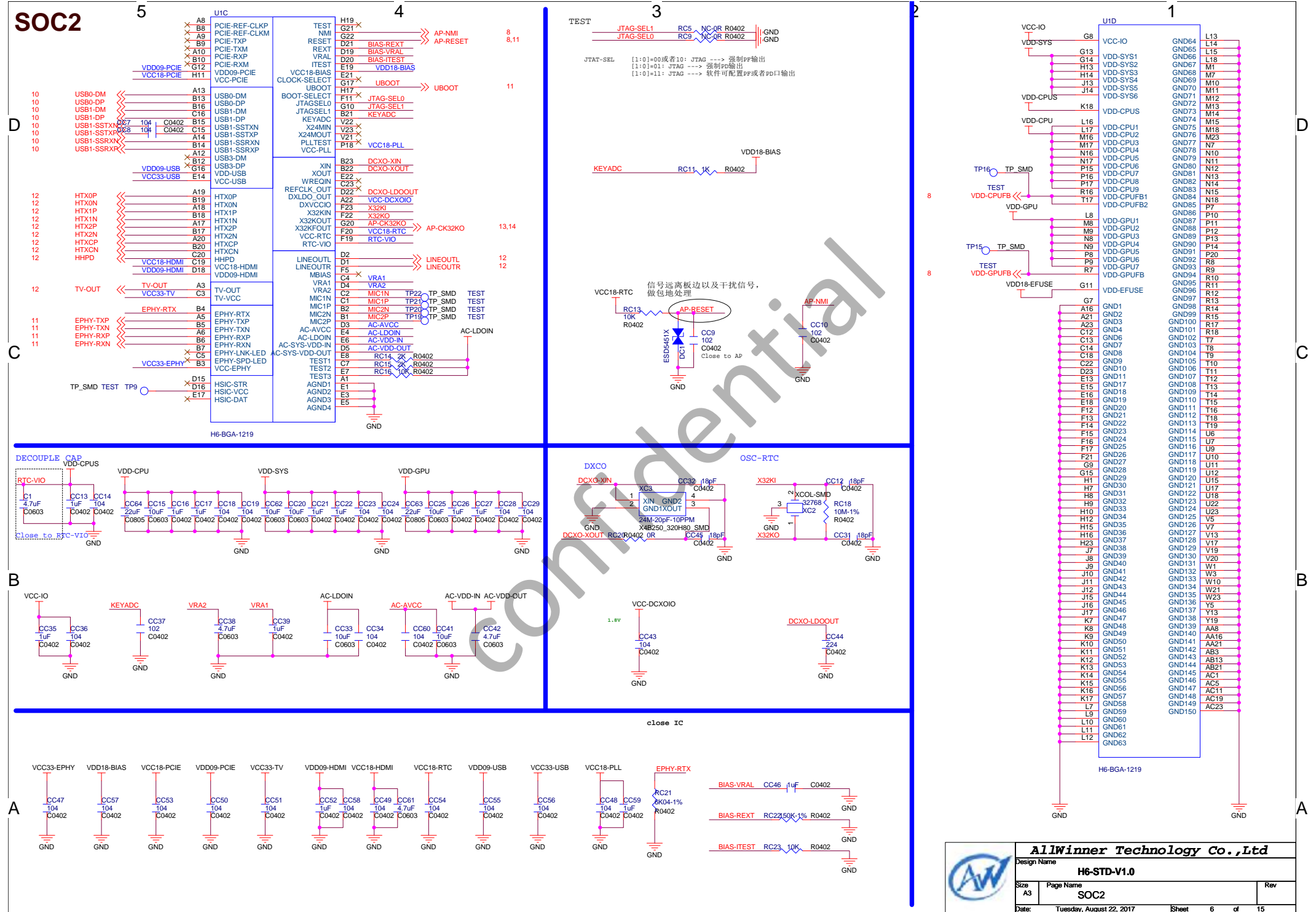
H6-BGA-1219



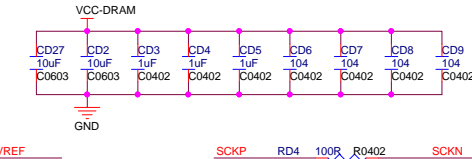
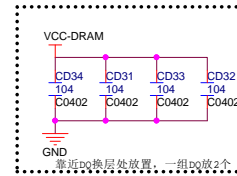
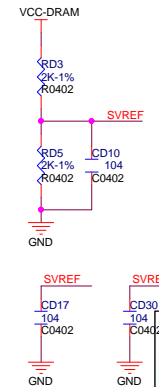
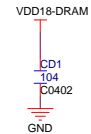
close to IC



SOC2



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PCB底层预留电容位置
默认不贴

VCC-DRAM

CD22 NC-10uF C0603

CD23 NC-1uF C0402

CD24 NC-104 C0402

CD25 NC-10 C0402

GND

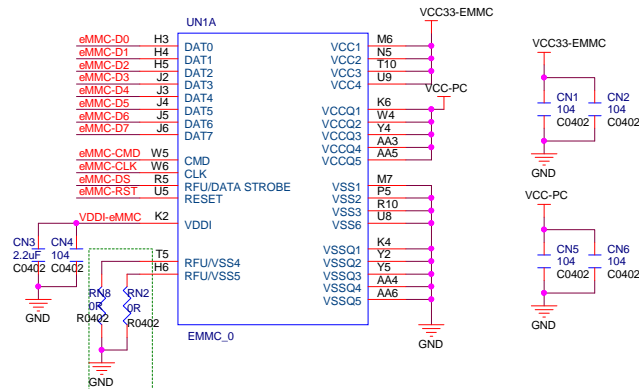
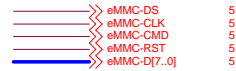
close to SoC

close to UD2

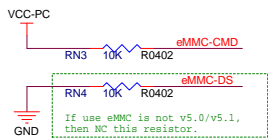
close to UD1

close to UD2

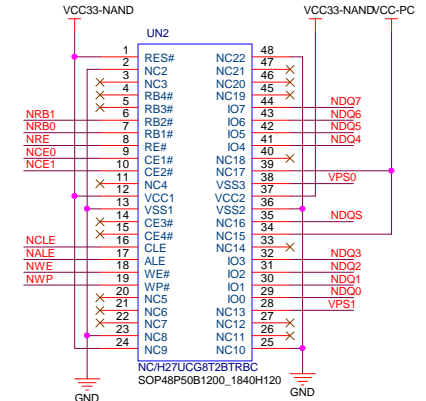
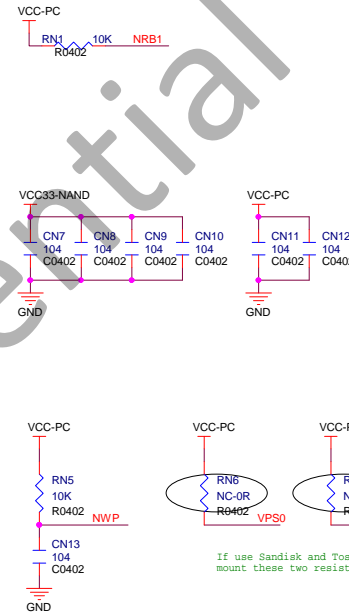
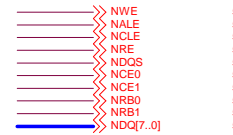
eMMC



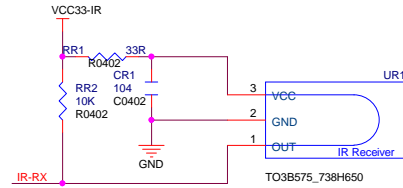
If eMMC is not v5.0/v5.1, then NC this two resistors.



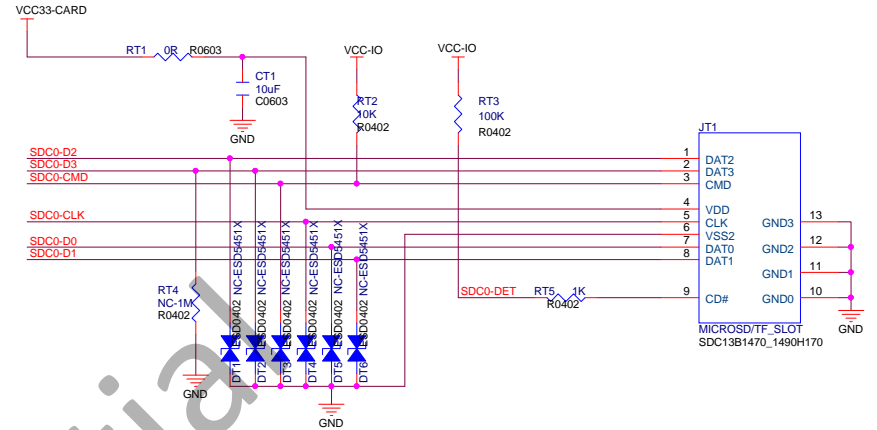
NAND



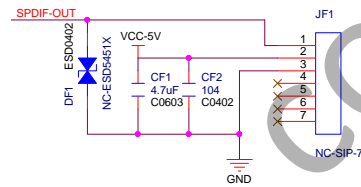
IR



CARD

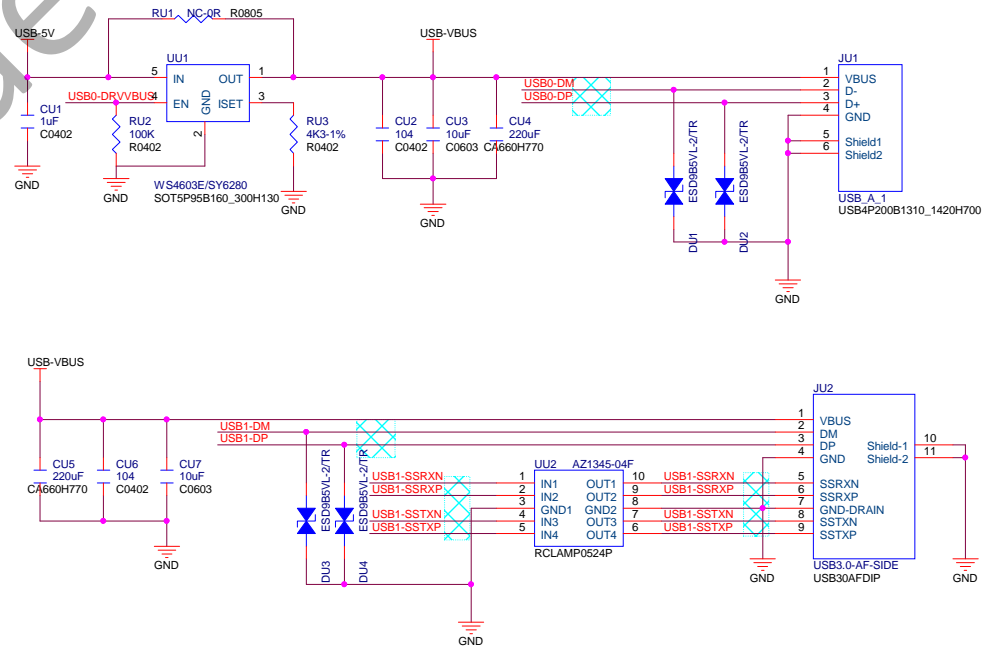


SPDIF



USB

Differential pairs
Z0= 90 ohm



6 EPHY-RXP
6 EPHY-RXN
6 EPHY-TXP
6 EPHY-TXN

5 CPUX-UTX
5 CPUX-URX
5 PWR-LED
5 STATUS-LED
5 LINK-LED

6,8	AP-RESET	⚡	_____
6	UBOOT	⚡	_____
5	RECOVERY	⚡	_____
8	PWRON	⚡	_____

The schematic diagram illustrates the EPHY-FE circuit, which interfaces the PHY layer with the Ethernet PHY. The circuit includes several key components and connections:

- PHY Layer:** The PHY layer is represented by a block with pins 1 through 16. The connections are as follows:
 - Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16 are connected to the PHY layer.
 - Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16 are connected to the PHY layer.
- Resistors:**
 - R0402: 10kΩ resistors used for termination and matching.
 - R0805: 75R-1% resistors used for termination and matching.
- Capacitors:**
 - C0402: 10pF capacitors used for decoupling and matching.
 - C1206: 1000pF/2KV capacitor used for decoupling.
- Diodes:**
 - DE1, DE2, DE3, DE4: Diodes used for signal conditioning and protection.
- Transformer:**
 - UE1: A transformer used for signal isolation and impedance matching.
- Connectors:**
 - RJ45: A standard RJ45 connector used for network connectivity.
 - 5V: A 5V regulator used for power supply.

CPUX-UTX RC24

UR

R0402

VCC-UART

RC25

10K

R0402

CPUX-URX

QC1

2

3

VCC-UART

RC25_NC

R0402

5

4

3

2

1

GND

JC1

CON2

hdr1_5p250b570_1500h700

BSN20

SOT3P95B130_290H103

The schematic diagram illustrates the LED driver circuit for the WNT2F04/MMBT3904 module. The circuit is powered by VCC33-LED and includes three LEDs (RED, BLUE, YELLOW) and three status LEDs (PWR-LED, STATUS-LED, LINK-LED). The LEDs are connected to the module's output pins (DL1, DL2, DL3) through current-limiting resistors (RL1, RL2, RL4). The status LEDs are connected to the module's status pins (PWR-LED, STATUS-LED, LINK-LED) through current-limiting resistors (RL6, RL10, RL14). The circuit uses three NPN transistors (QL1, QL2, QL3) to drive the LEDs. The base of QL1 is connected to VCC33-LED through RL3 and RL5, and to the PWR-LED pin through RL6. The emitter of QL1 is connected to GND through RL7. The base of QL2 is connected to VCC33-LED through RL8 and RL11, and to the STATUS-LED pin through RL10. The emitter of QL2 is connected to GND through RL12. The base of QL3 is connected to VCC33-LED through RL13 and RL15, and to the LINK-LED pin through RL14. The emitter of QL3 is connected to GND through RL16. The module's output pins (DL1, DL2, DL3) are connected to the LEDs through current-limiting resistors (RL1, RL2, RL4). The module's status pins (PWR-LED, STATUS-LED, LINK-LED) are connected to the status LEDs through current-limiting resistors (RL6, RL10, RL14). The module's power supply pin (VCC33-LED) is connected to the power supply through RL3 and RL5. The module's ground pin (GND) is connected to the ground through RL7, RL12, and RL16.

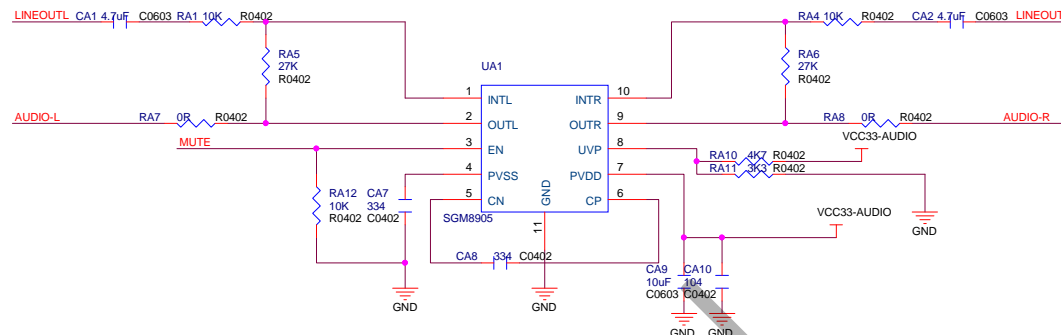
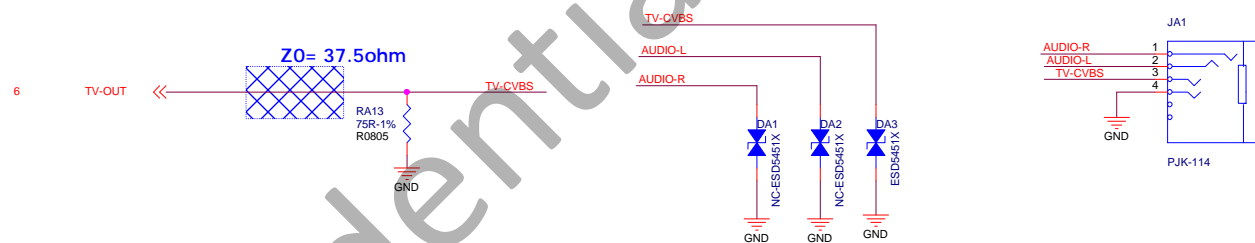


Design Name	H6-STD-V1.0
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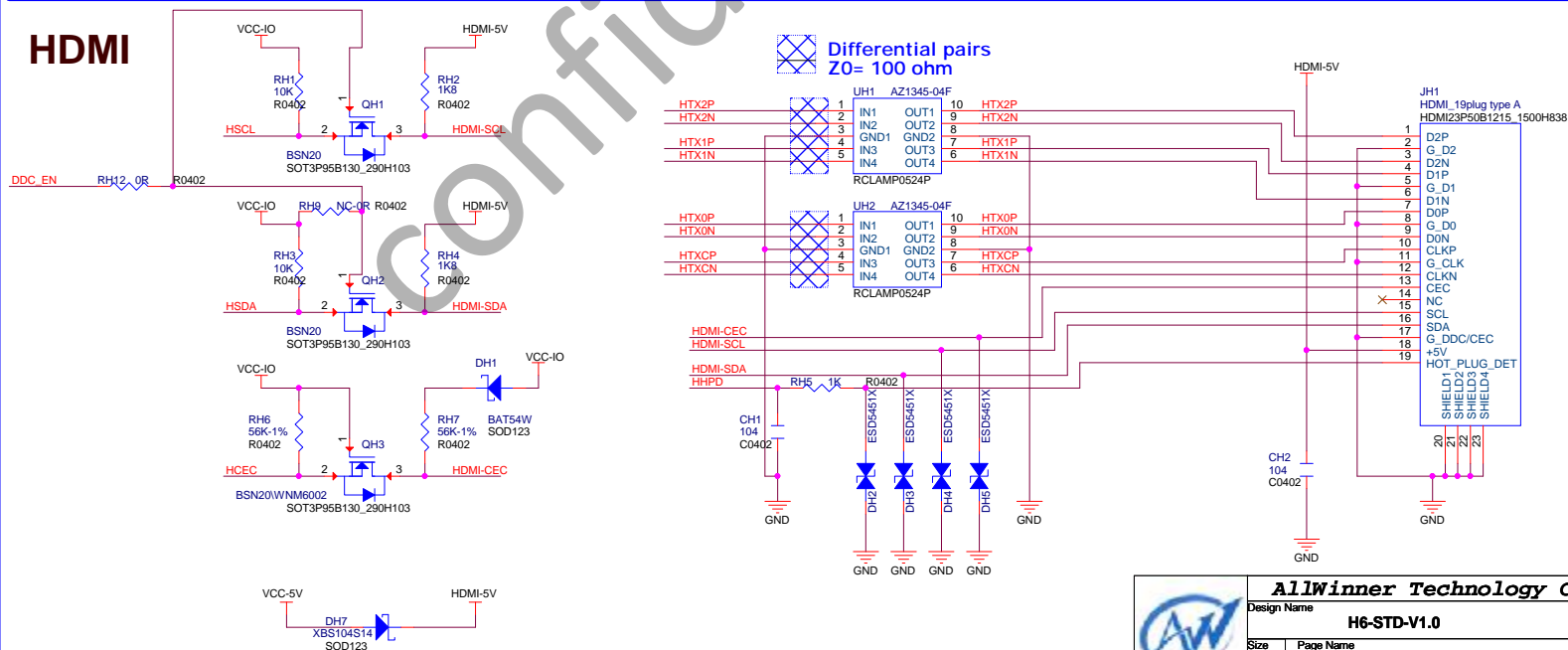
Size A3	Page Name KEY-LED-ETH-DEBUG
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输出 $2V_{rms}$


$$Z_0 = 37.5 \Omega$$


Differential pairs
Z0= 100 ohm



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Page Name	AV-HDMI
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	Rev
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WIFI+BT 2T2R

5,14 WL-SDIO-CMD
5,14 WL-SDIO-D0
5,14 WL-SDIO-D1
5,14 WL-SDIO-D2
5,14 WL-SDIO-D3
5,14 WL-SDIO-CLK

5,14 BT-UART-TX
5,14 BT-UART-RX
5,14 BT-UART-RTS
5,14 BT-UART-CTS
5,14 BT-PCM-SYNC
5,14 BT-PCM-CLK
5,14 BT-PCM-DIN
5,14 BT-PCM-DOUT

5,14 BT-REG-ON
5,14 WL-WAKE-AP
5,14 BT-WAKE-AP
5,14 AP-WAKE-BT
5,14 WL-REG-ON
6,14 AP-CK32KO

5 BT-WIFI-ON

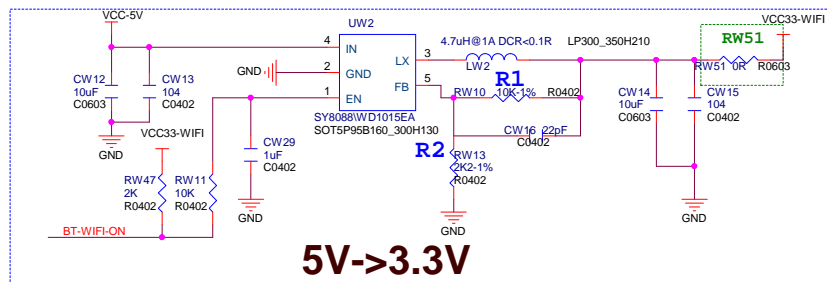
NOTE FOR crystal:

AP6356s	37.4M
WCT6RA2001S	48M

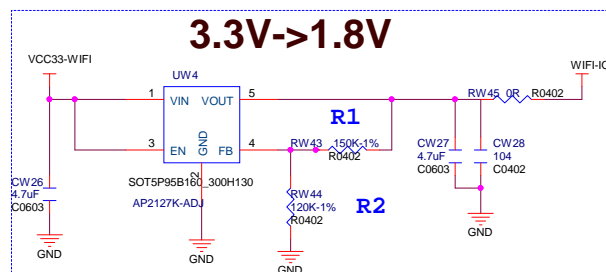
NOTE FOR:	L	C
AP6356s	4.7uH	4.7uF
WCT6RA2001S	1.5uH	22uF

NOTE:
L1, rated current 1A
expectation specification.

5V->3.3V (WIFI)和 3.3V->1.8V(WIFI+IO)电路仅用于需要时延控制的产品。
不存在时延控制唤醒的产品, 可以使用CLDO2+CLDO3来供给WIFI, ALDO1或者BLDO3来供给WIFI+IO

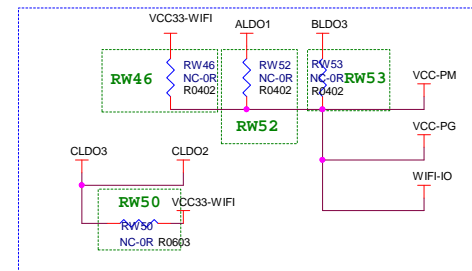


5V->3.3V



3.3V->1.8V

50 Ohm RF trace

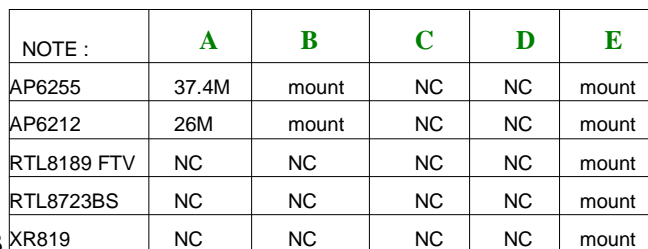


NOTE FOR:	RW51	RW45	RW46	RW50	RW52	RW53
不带蓝牙遥控	IO为1.8V	NC	NC	NC	0R	NC
	IO为3.3V	NC	NC	NC	0R	NC
带蓝牙遥控	IO为1.8V	0R	0R	NC	NC	NC
	IO为3.3V	0R	NC	0R	NC	NC

1

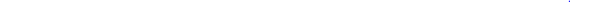
E

50 Ohm RF trace



I

XR819	NC	NC	NC	NC	mount
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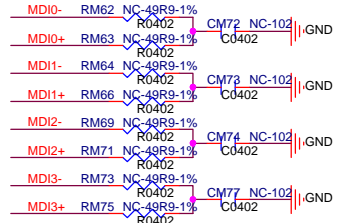
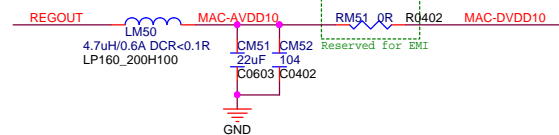
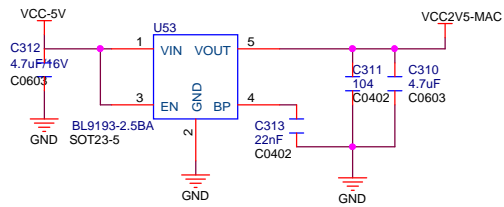
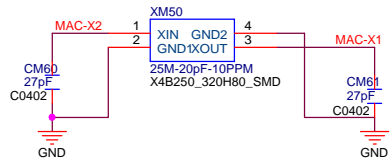
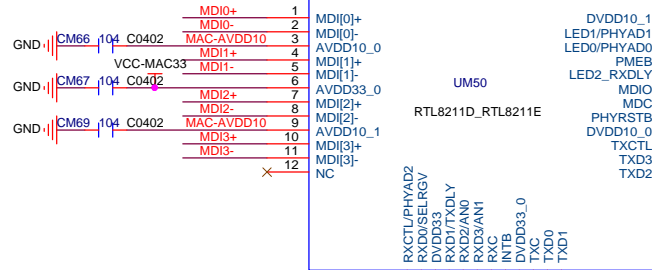
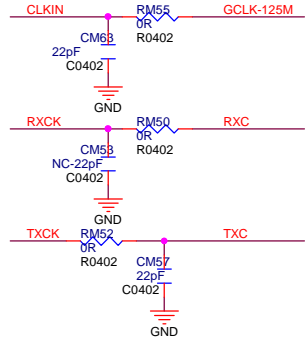


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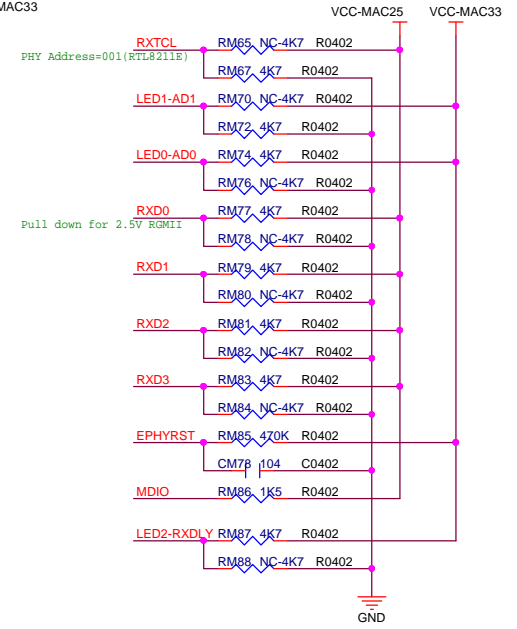
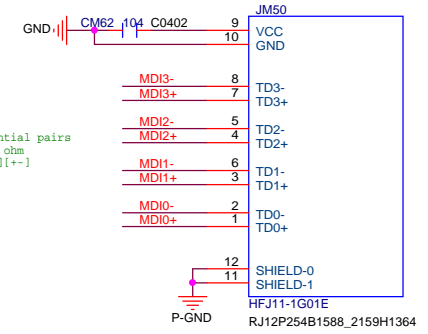
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GMAC

5 RGMII-RXD3 RXD3
5 RGMII-RXD2 RXD2
5 RGMII-RXD1 RXD1
5 RGMII-RXD0 RXD0
5 RGMII-RXCK RXCK
5 RGMII-RXCTL RXCTL
5 RGMII-TXD3 TXD3
5 RGMII-TXD2 TXD2
5 RGMII-TXD1 TXD1
5 RGMII-TXD0 TXD0
5 RGMII-TXCK TXCK
5 RGMII-TXCTL TXCTL
5 RGMII-CLKIN CLKIN
5 MDIO MDIO
5 RGMII-RESET EPHYRST

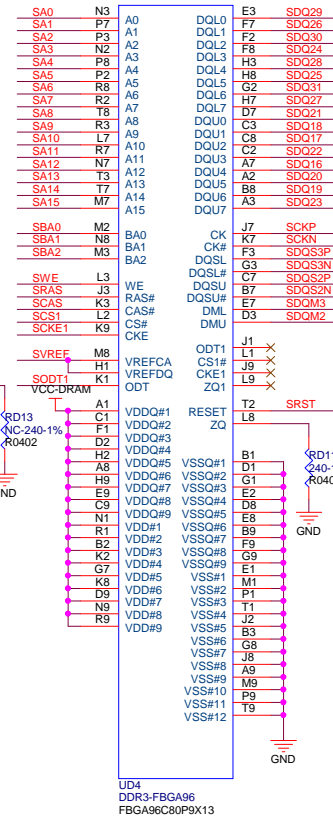
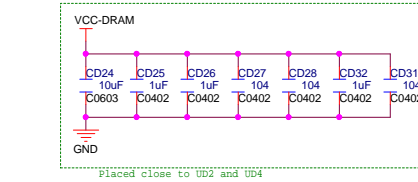
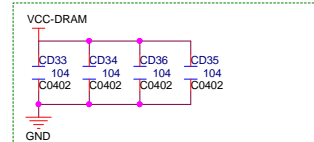
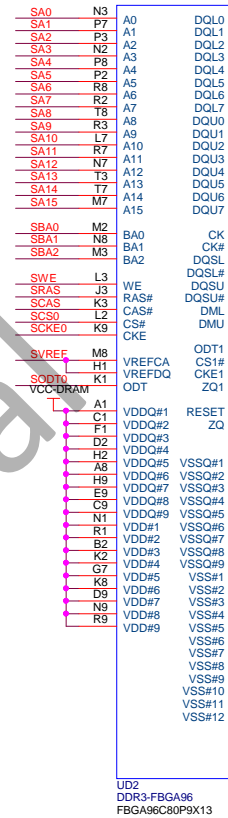
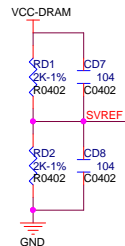
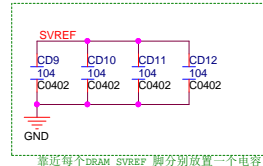
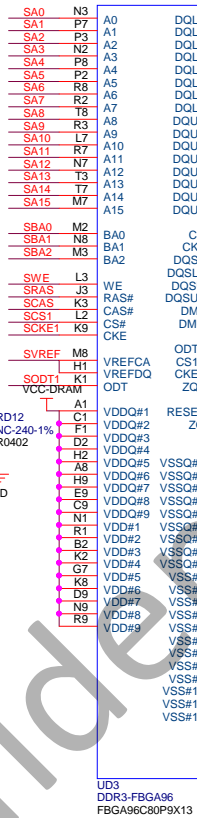
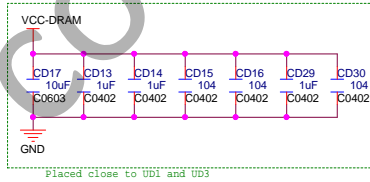
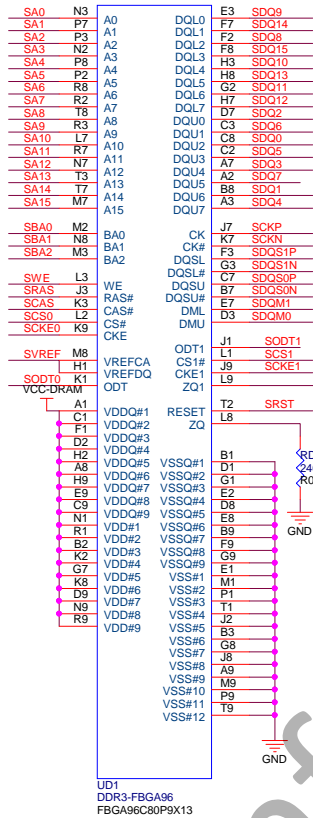
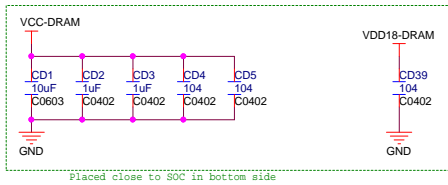
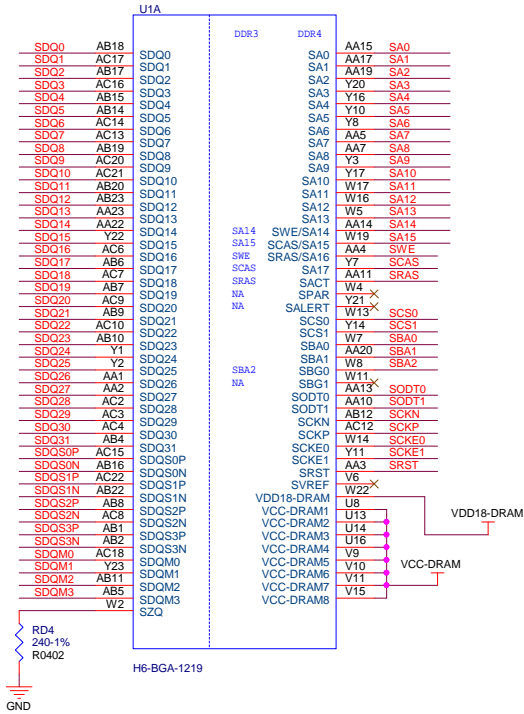


Differential pairs
Z0= 100 ohm
MDI[0-3][+/-]

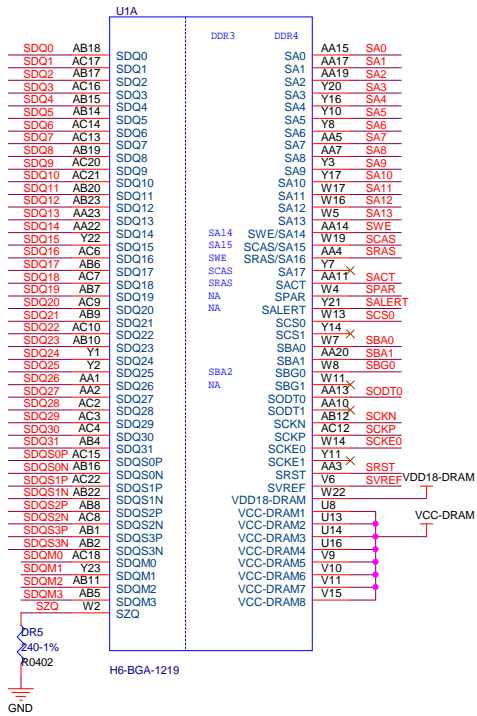


Allwinner Technology Co., Ltd			
Design Name			
H6-STD-V1.0			
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DDR3_16X4D



DDR4 16X2



LPDDR3

