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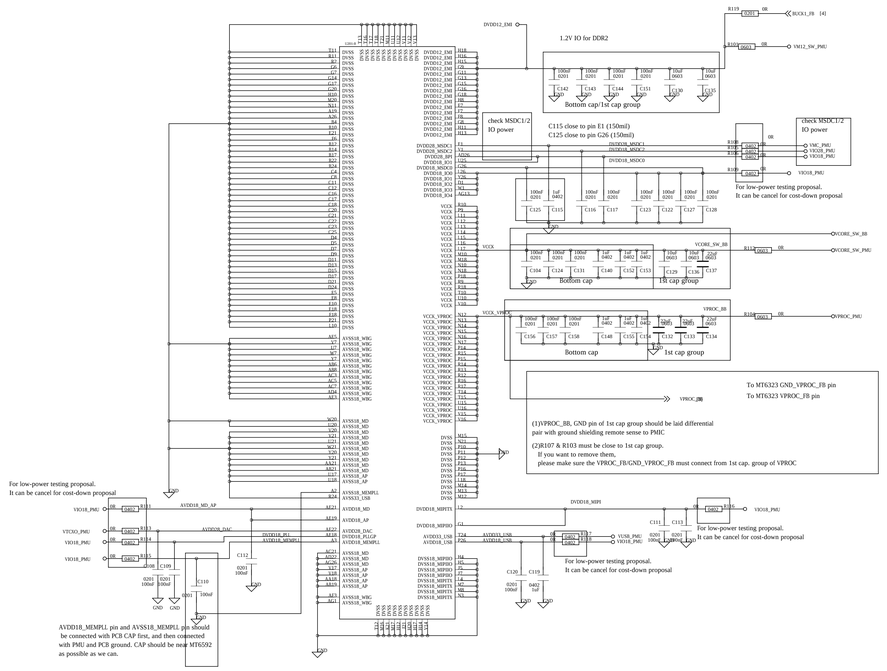

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SH201
GND
SH-T8850-88

Pin	DVDD18_EFUSE	FSOURCE_P	Description
Voltage	VGPx (2V0)		w/i EFUSE program
	GND		w/o EFUSE program

EFUSE Notice

Please reserve UART0/1 test point
UART0 for AP log
UART1 for MD log

C213 Close to MT6582
AF19 should connect to C213.2 first, than connect to GND by via

Please reserve bypass cap for AUX_ADC decoupling (from Antenna) proposal.
It can be cancel for cost-down proposal.

MT6333 switching charger function de-feature
(Need to add external SWCHR)
Change notice:
Page 2
1. Add GPIO_CHG_EN/GPIO93_DRVVBUS trace

MT6605 OSC_EN (SRCLKENAI) need to default low for MT6605 TESTMODE boot-strap

C208 are for ESD ehshace proposal.
It can be cancel for cost-down proposal

For earpohne & MSDC hotplug EINT, plase choose EINT0~15 with HW de-bounce function.

Close to MT6592

Close to MT6592

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Symbol	LPDDR2/1.2V	PCDDR3U/1.35V	PCDDR3/1.5V	LPDDR1/1.8V	Default
SPI_CSN	H	L (20K)	H	L (20K)	PU
XUD_MOSI	L	H (20K)	H (20K)	L	PO

MT6333 switching charger function de-feature (Need to add external SWCHR)
Change notice:
Page 3
1. Add R335, MT6322 pin N13 (CHRLDO) connect to R335, then connect to VBUS_1
2. R330.1 connect to VUBS_1

Plasse reservr R331/NTC301 & R339/NTC302
for thermal protection option

Close to battery connector

SOD123
500mW

VF : 4.85V~5.36V

Refer to MT6323 design
notice for Zener selection

What should connect to C341 first,
then star-connesion to MT6323

Star-connection

MT6166 side	MT6322 side	
C159	C321	
NC	0.1uF	
1uF	0.1uF	
0.1uF	0.1uF	

No GPS / w/ GPS: GPS co-clock / GPS non co-clock

Reserved C321 for no GPS application.

For low-power testing proposal.
It can be cancel for cost-down proposal

C322 must to be close
to MT6323 pin B1

GND_AUXADC

Connect 3600 pin2
GND to MT6323 pin
B2 first then
connect
to main GND (near pin B2)

Close to MT6322 AUXADC_VREF18 PIN,
and the path need shielding with GND

BATTERY CONNECTOR

Please refer to MT6322 design notice for
Buck GND layout rule

(1)MT6322 Buck GND(GND_VPROC/GND_VPA/GND_VSYS) is connected together first,
and then single trace connect to GND layer

(2)Use single trace >40mil or GND plan to connect buck input bypass cap
and MT6322 GND pins of buck in the same layer,
and then isolate this GND plan

if you use digital MIC,
please change cap (C241)
to 1.0uF

Connect to MT6166 XO4 pin directly

Reserved for desense tuning proposal.
It can be cancel for cost-down proposal

C333 are for VPROC_FB decoupling proposal.
It can be cancel for cost-down proposal

From 1st cap. group of VPROC on MT6582 side
VPROC_FB, GND_VPROC_FB should be laid differential
pair with ground shielding remote sense to PMIC

L303 / L302 / L303
Please use inductor recommand by MTK
Refer to MT6323 design notice

PMU side

Backup Batt.

For 32k-less, please change GB301(battery) to 22uF cap.
Recommend implementing 1~100uF for VRTC,
DONOT implement the backup battery. (Because of the Time precision: +-1.5 sec every 30 sec)

For longer RTC time sustain after battery remove,
please refer to RTC design notice.

I2C Address
FAN53555 : 0xC0
NCP6335D: 0x1C

U302 placement, please be close to MT6322
L307 placement, please be close to L301

C327 must to be close
to U202

AUADC_REF should be laid L307 as close as possible to L301,
then connect to VPROC_PMU

VPROC_FB should be ground shielding.

Close to MT6322

RTC 32K :
(1) X301 / C324 / C319 = mount
(2) R333 / R350 = NC

RTC 32K-less (NOT MP yet)
(1) X301 / C324 / C319 = NC
(2) R333 / R350 = 0R

Regulator	Output Voltage(V)	Output Current(mA)	Input Decoupling	Output Decoupling	Notes
VPROC	0.7~1.4	2800	>10uF	L=0.68uH,C=10uF*4	Total outptu cap>40uF
VSYS	2.2	1200	>10uF	L=0.68uH,C=10uF*2	Total outptu cap>20uF
VPA	0.5~3.4	600	>4.7uF	L=2.2uH,C=2.2uF+2.2uF	Output cap range 4.4uF +/-20%

LDO	Output Voltage(V)	Output Current(mA)	Input Decoupling	Output Decoupling	Notes
VM	1.24 /1.39/1.54/1.84	700	10uF	-20%~+20%	Far-end bypass cap
VRF18	1.825	200	1uF	-20%~+200%	Far-end bypass cap
VIO18	1.8	300	4.7uF	-20%~+200%	Far-end bypass cap
VCN_1V8	1.8	120	1uF	-20%~+20%	Far-end bypass cap
VCAMD	1.2 /1.3/1.5/1.8	150	1uF	-20%~+20%	Far-end bypass cap
VCAM_IO	1.8	100	1uF	-20%~+20%	Far-end bypass cap
VGP3	1.2 /1.3/1.5/1.8	200	1uF	-20%~+20%	Far-end bypass cap
VA	2.8	150	1uF	-20%~+20%	Far-end bypass cap
VTCXO	2.8	40	1uF	-20%~+20%	Far-end bypass cap
VCN28	2.8	30	1uF	-20%~+20%	Far-end bypass cap
VCAMA	2.8	150	3.2uF	-20%~+20%	1uF near-end ,2.2uF Far-end bypass cap
VCN33	3.3/3.4/3.5/3.6	350	4.7uF	-20%~+20%	Far-end bypass cap
VIO28	2.8	200	2.2uF	-20%~+200%	Far-end bypass cap
VUSB	3.3	20	1uF	-20%~+20%	Far-end bypass cap
VMC	1.8 /3.3	100	1uF	-20%~+20%	Far-end bypass cap
VMCH	3.0 /3.3	400	2.2uF	-20%~+20%	Far-end bypass cap
VEMC_3V3	3.0 /3.3	400	4.7uF	-20%~+20%	Far-end bypass cap
VCAM_AF	1.2/1.3/1.5/1.8 /2.0 2.8/3.0/3.3	100	1uF	-20%~+20%	Far-end bypass cap
VSIM1	1.8 /3.0	50	1uF	-20%~+20%	Far-end bypass cap
VSIM2	1.8 /3.0	50	1uF	-20%~+20%	Far-end bypass cap
VGP1	1.2/1.3/1.5/1.8/2.0 2.8 /3.0/3.3	100	1uF	-20%~+20%	Far-end bypass cap
VGP2	1.2/1.3/1.5/1.8/2.0 2.5 /3.0/3.3	100	1uF	-20%~+20%	Far-end bypass cap
VIBR	1.2 /1.3/1.5/1.8/2.0 2.8/3.0/3.3	100	1uF	-20%~+20%	Far-end bypass cap
VDIG18	1.8	20	1uF	-20%~+20%	Far-end bypass cap
VRTC	2.8	2	0.1uF to 1000uF	-20%~+20%	Far-end bypass cap

PJD	03 MT6592 - Power & MT6322
Size / Document Number	MT6592 PHONE / V1.0
Date: Tuesday, July 30, 2013	Sheet 3 of 22

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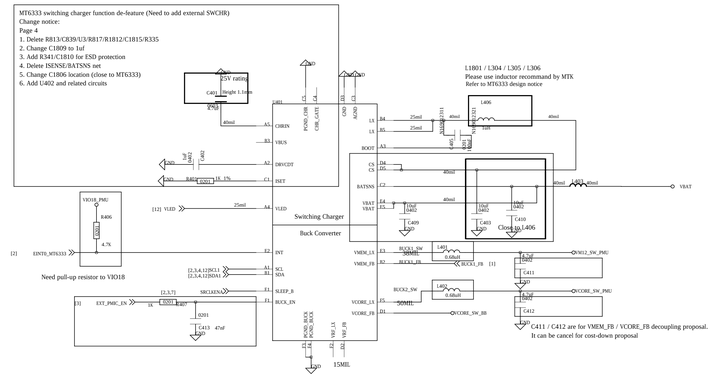

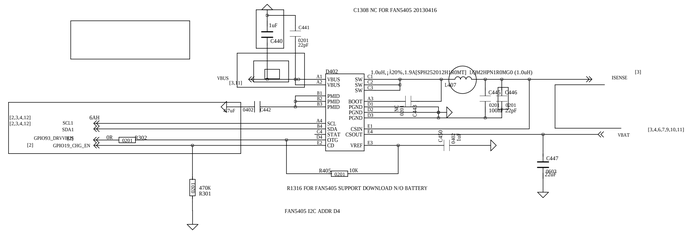

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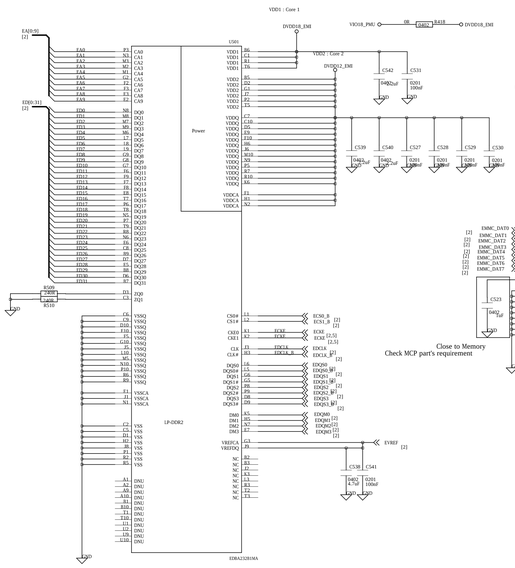
SDIN8DE1-8G

VDDI	VCC	VCCQ
>=100nF	<=100nF	<=100nF
	>=4.7uF	>=4.7uF

Discrete LPDDR2

134 ball, 0.5mm pitch

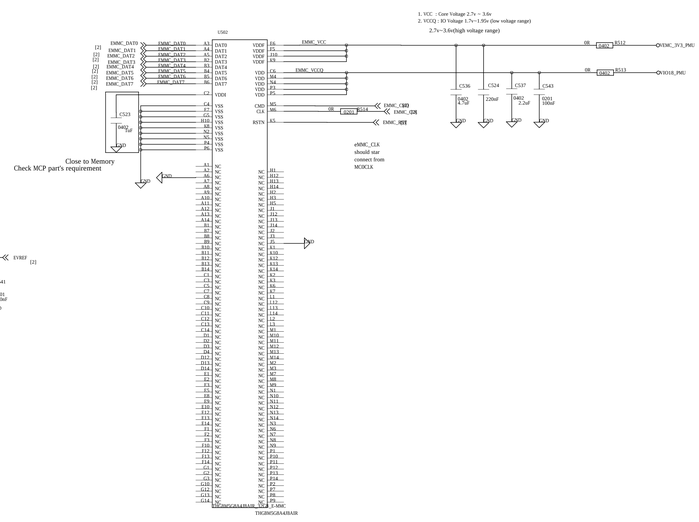
VDD1=1.8V
VDD2=1.20V
VDDCA=1.2V
VDDQ= 1.20V



VDD1=1.8V
VDDQ=1.20V
VDDCA=1.2V
VDDQ= 1.20V

Discrete eMMC (153 balls)

153 ball, 0.5mm pitch



Close to Memory
Check MCP part's requirement

6	5	4	3	2	1

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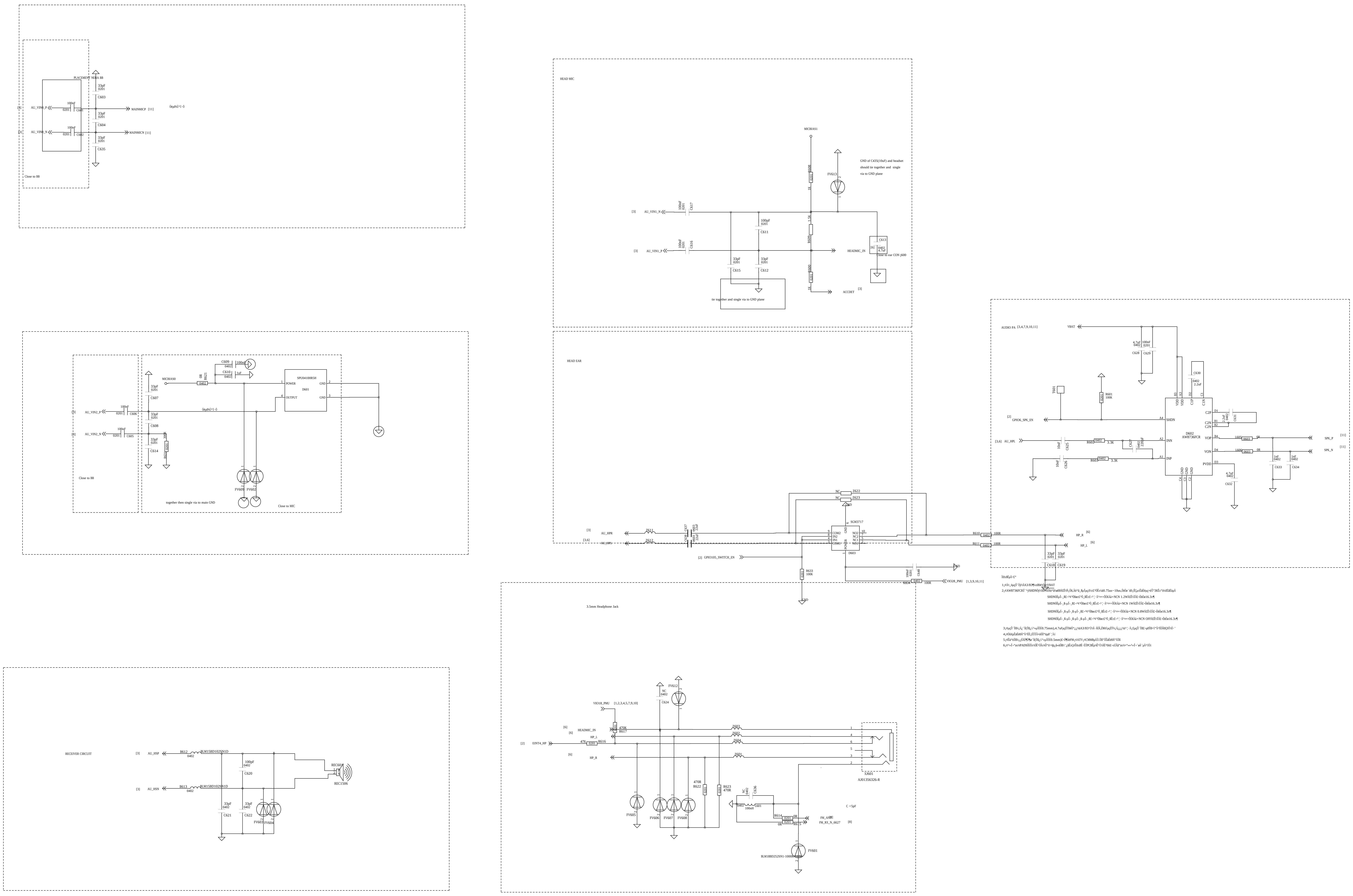

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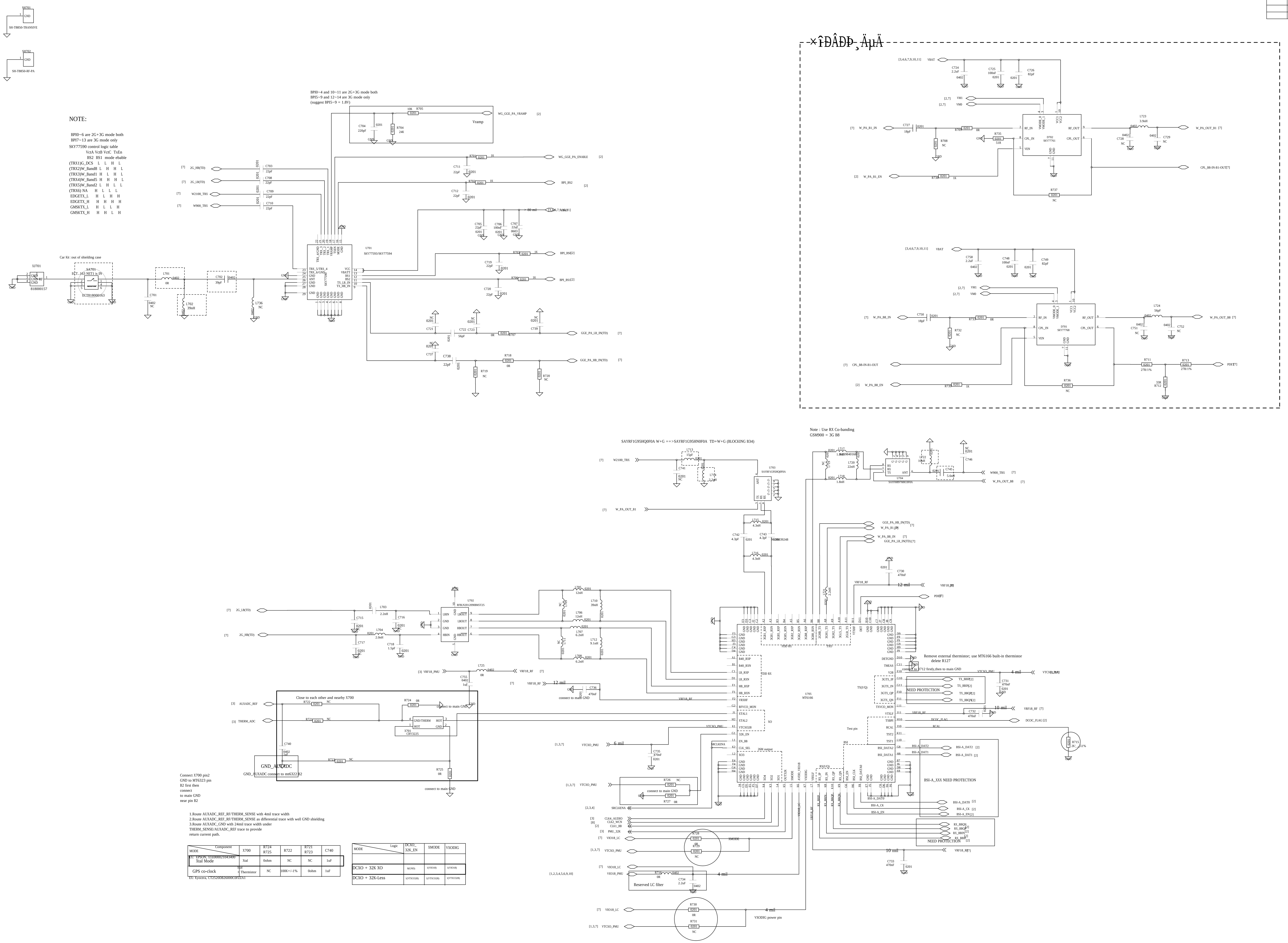

NOTE:

BPI0~6 are 2G+3G mode both
BPI7~13 are 3G mode only

SKY77590 control logic table

	VctA BS2	VctB BS1	VctC mode	TxEn ebable
(TRX1)G_DCS	L	L	H	L
(TRX2)W_Band8	L	H	H	L
(TRX3)W_Band1	H	L	H	L
(TRX4)W_Band5	H	H	H	L
(TRX5)W_Band2	L	H	L	L
(TRX6) NA	H	L	L	L
EDGETX_L	H	L	H	H
EDGETX_H	H	H	H	H
GMSKTX_L	H	L	L	H
GMSKTX_H	H	H	L	H

Connect X700 pin2
GND to MT6323 pin
B2 first then
connect
to main GND
near pin B2

GND_AUXADC
GND_AUXADC connect to mt6322 B2

1.Route AUXADC_REF_RF/THERM_SENSE with 4mil trace width
2.Route AUXADC_REF_RF/THERM_SENSE as differential trace with well GND shielding
3.Route AUXADC_GND with 24mil trace width under THERM_SENSE/AUXADC_REF trace to provide return current path.

MODE \ Component	X700	R724 R725	R722	R721 R723	C740
Xtal Mode (EX: EPSON, X1E000021043400)	Xtal	0ohm	NC	NC	1uF
GPS co-clock	Xtal + Thermistor	NC	100K+/-1%	0ohm	1uF

EX: Kyocera, CT2520DB26000C0FZZA1

MODE \ Logic	DCXO_ 32K_EN	XMODE	VXODIG
DCXO + 32K XO	0(GND)	1(VIO18)	1(VIO18)
DCXO + 32K-Less	1(VTXCO28)	1(VTXCO28)	1(VTXCO28)

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SH-T8850-WIFI

SH-T8850-CRYSTAL

MT6628_GPS / FM

Car Kit :out of shielding case

Based on your system level design , if better WIFI performance is needed on your system, please refer to WiFi performance enhance proposal

Based on your system level design , if better GPS performance is needed on your system, please refer to GPS performance enhance proposal

FM

Bead1001 are for FM desense-free proposal.
They can be cancel for cost-down proposal

Close to MT6572

Close to MT6627

change from AVDD28_FM to VCN_2V8_PMU refer to V0.4 by sunning 0411

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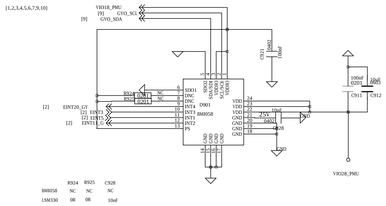
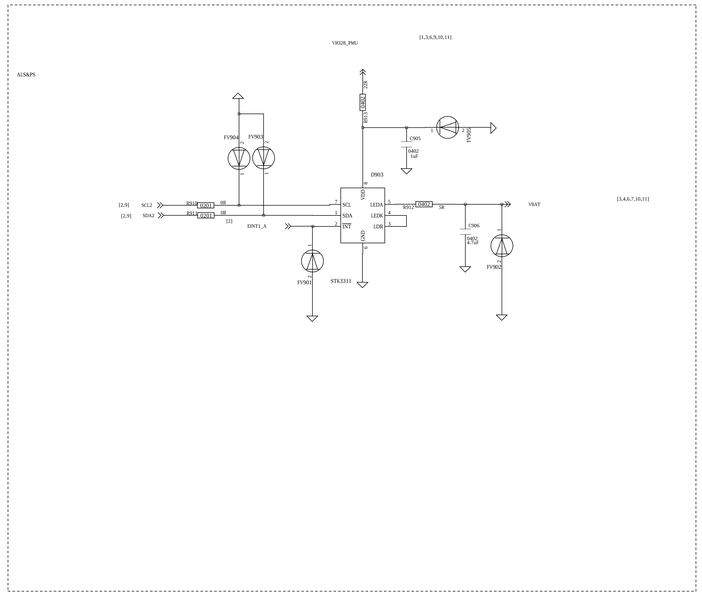
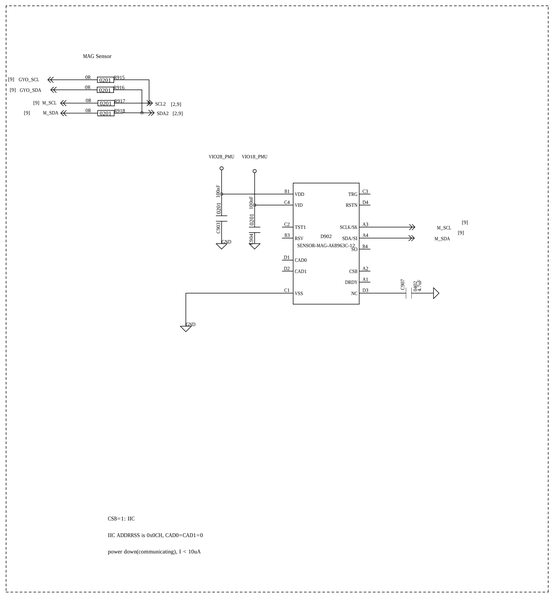
BMI058 G-SENSOR 0x18
GY 0x68

LSM330 G-SENSOR 0x1E
GY 0x6A







G-Sensor

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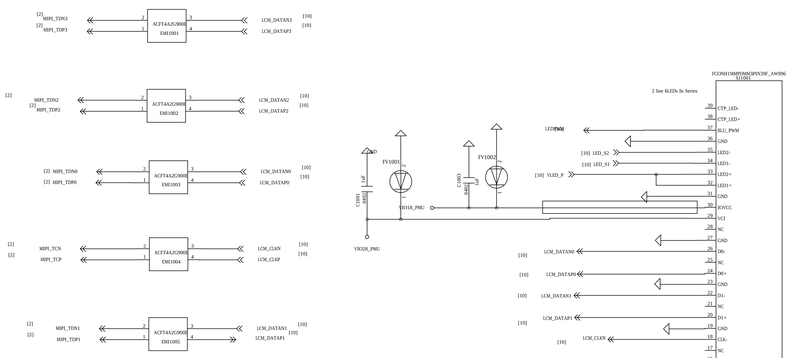
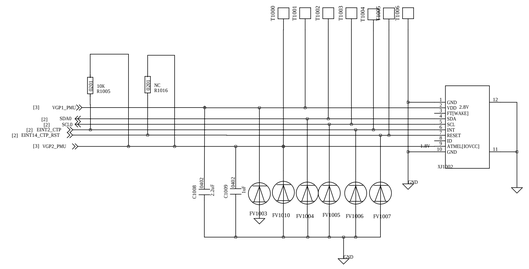
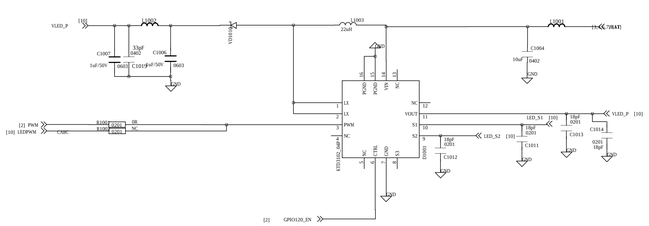
MIPI CMEF



4.3" COF CTP



Back Light Driver for 12LEDs In 2Series 6 P



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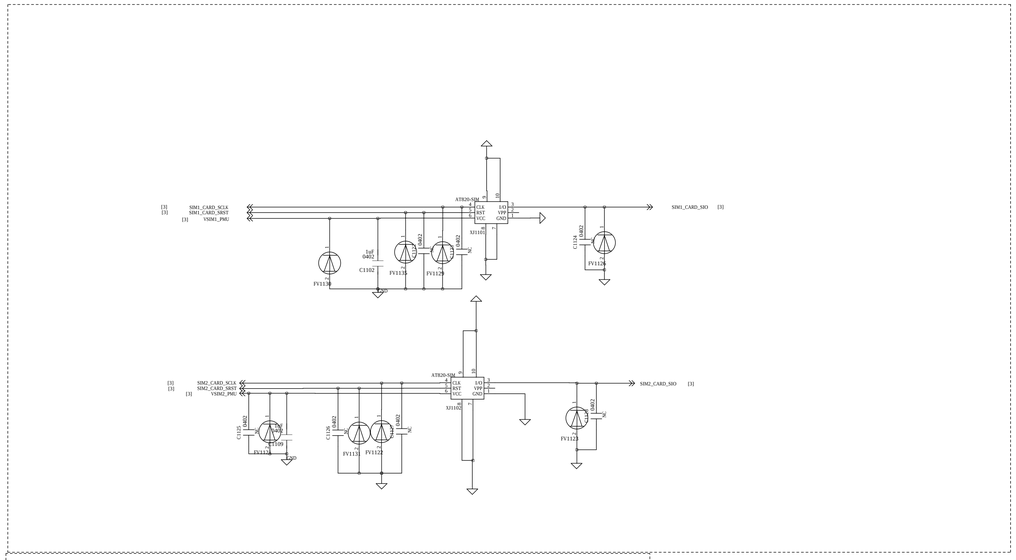

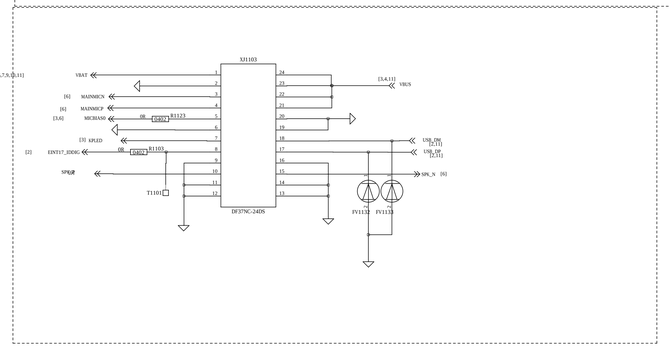

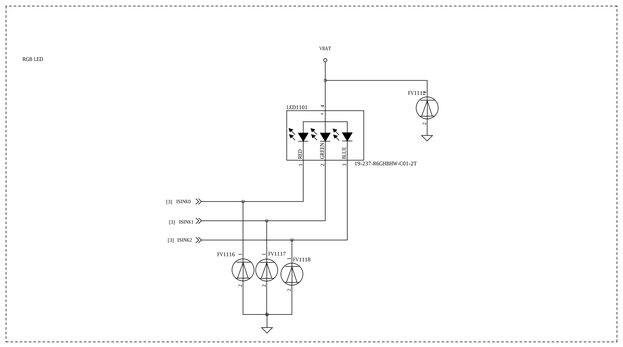

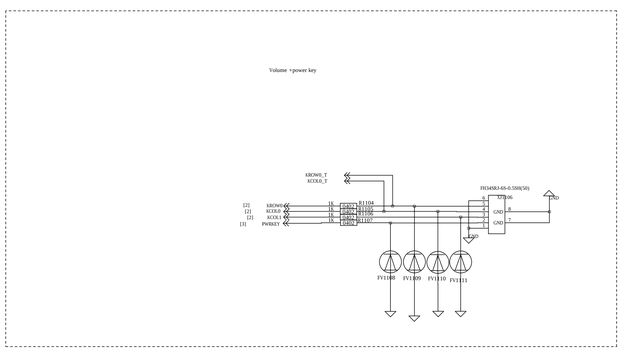

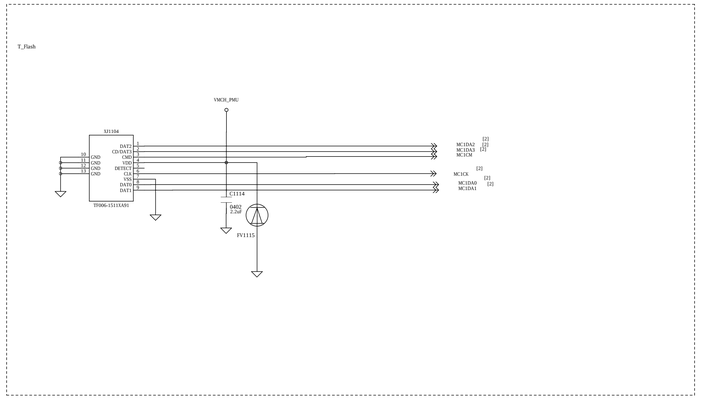

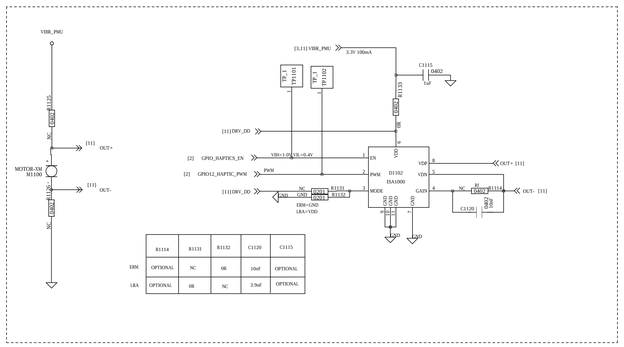

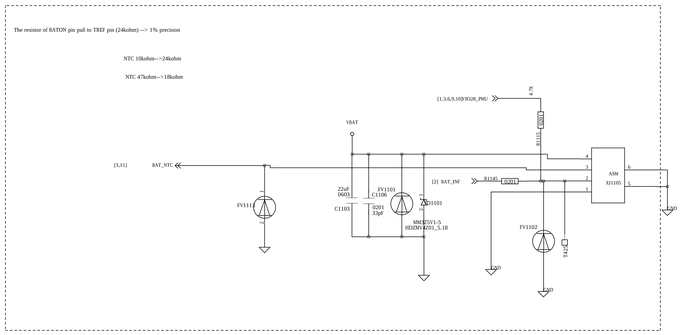

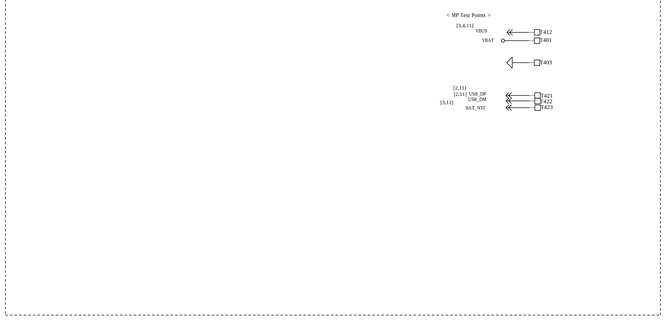

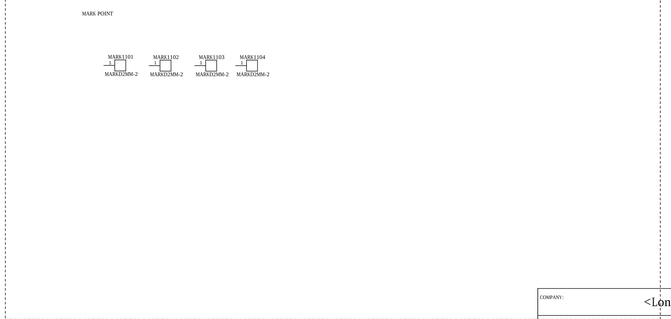

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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

300W

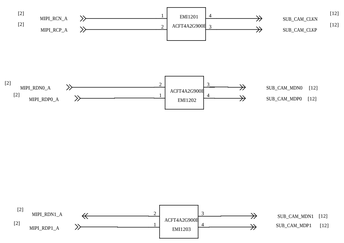
DBVR IC	SEN_DVDD	SEN_DOVDD	SEN_AVDD
	1.2V	2.8V/1.8V	2.8V

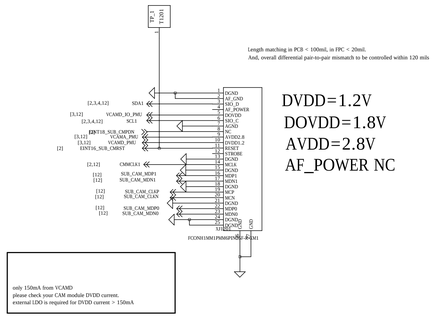
500W 1.2/1.3/1.5/1.8 1.2/1.3/1.5/1.8 1.8/2.5/2.8/3.0

DBVR IC	SEN_DVDD	SEN_DOVDD	SEN_AVDD
A80543	NC	1.8V	2.8V
	200mA	200mA	100mA

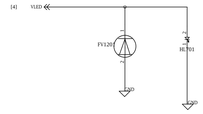
0.3M Sensor

MIPI CMEF

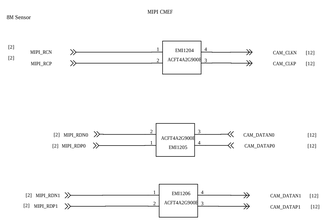


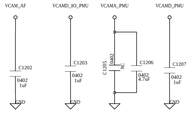


DVDD=1.2V
DOVDD=1.8V
AVDD=2.8V
AF_POWER NC



IM SensorMIPI CMEF



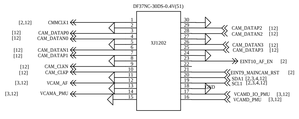


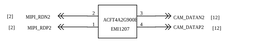
Length matching in PCB < 100mil, in FPC < 20mil.
And, overall differential pair-to-pair mismatch to be controlled within 120 mils

IMX135
AF POWER 2.7V
AVDD 2.7V
DVDD 1.2V
DOVDD 1.8V

S5K3L2
AF POWER 2.8V
AVDD 2.8V
DVDD 1.2V
DOVDD=1.8V

VRF18_2 1.05~1.25 (50mV/step)





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