|  |  |
| --- | --- |
| Name: \_\_\_\_Syed Muhammad Adil  \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ | EE-272L Digital Systems Design |
| Reg. No.: \_\_\_\_\_\_\_\_\_\_\_2022-EE-139  \_\_\_\_\_\_\_\_\_\_\_\_\_ | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

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**Lab Manual**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **DSD Lab Manual Evaluation Rubrics** | | | | | |
|  |  |  |  |  |  |
| **Assessment** | **Total Marks** | **Marks Obtained** | **0-30%** | **30-60%** | **70-100%** |
| Code Organization | 3 |  | No Proper Indentation and descriptive naming, no code organization.  Zero to Some understanding but not working | Proper Indentation or descriptive naming or code organization.  Mild to Complete understanding but not working | Proper Indentation and descriptive naming, code organization.  Complete understanding, and proper working |
| Simulation | 5 |  | Simulation not done or incorrect, without any understanding of waveforms | Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms | Working simulation without any errors, etc and complete understanding of waveforms |
| FPGA | 2 |  | Not implemented on FPGA and questions related to synthesis and implementation not answered. | Correctly Implemented on FPGA or questions related to synthesis and implementation answered. | Correctly Implemented on FPGA and questions related to synthesis and implementation answered. |

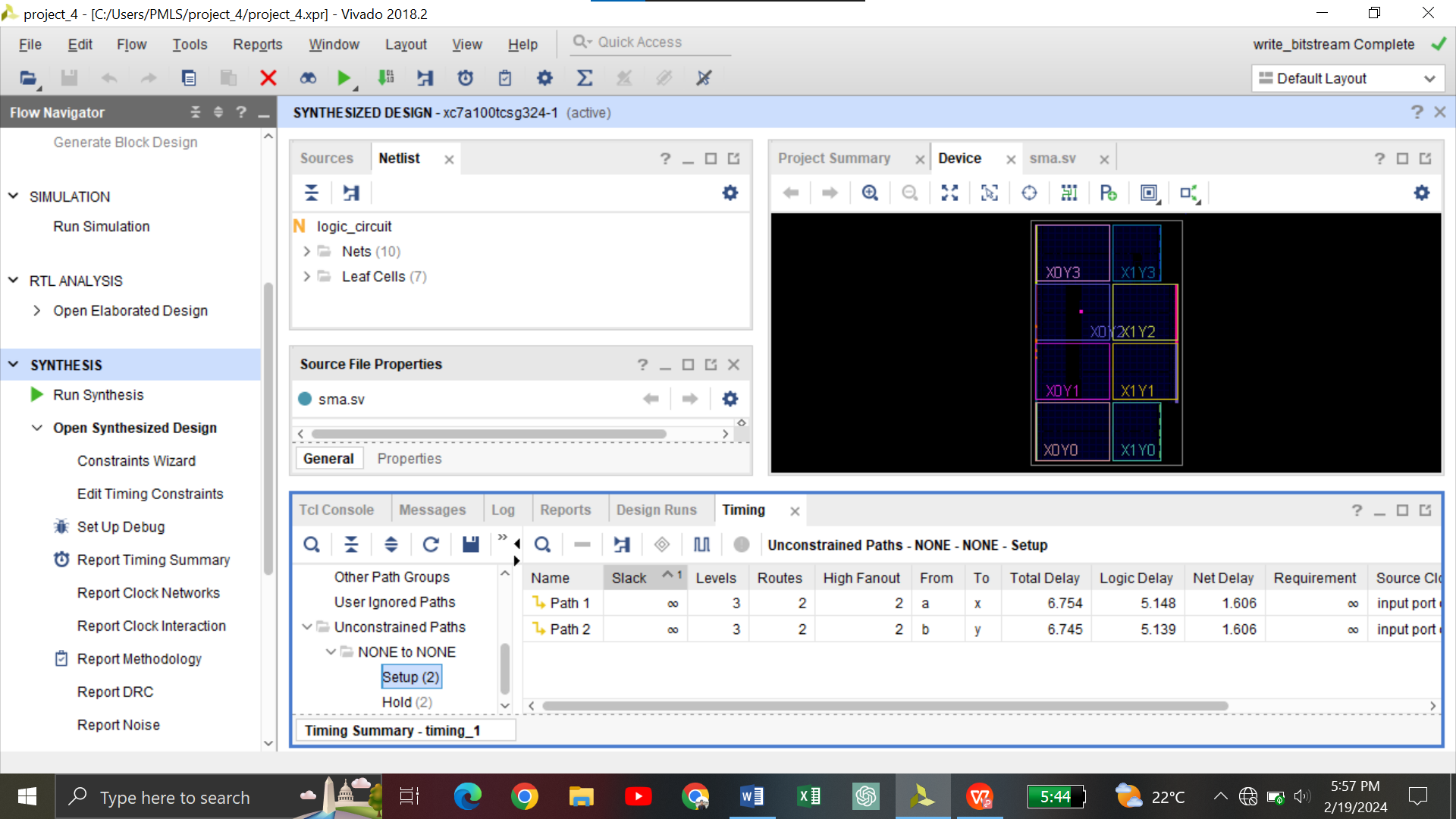
**TASK-1:**

**(a)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | X | Y |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**(b)**

**The path from input ‘a’ to output ‘x’ has the maximum combination delay due to logic delay .**

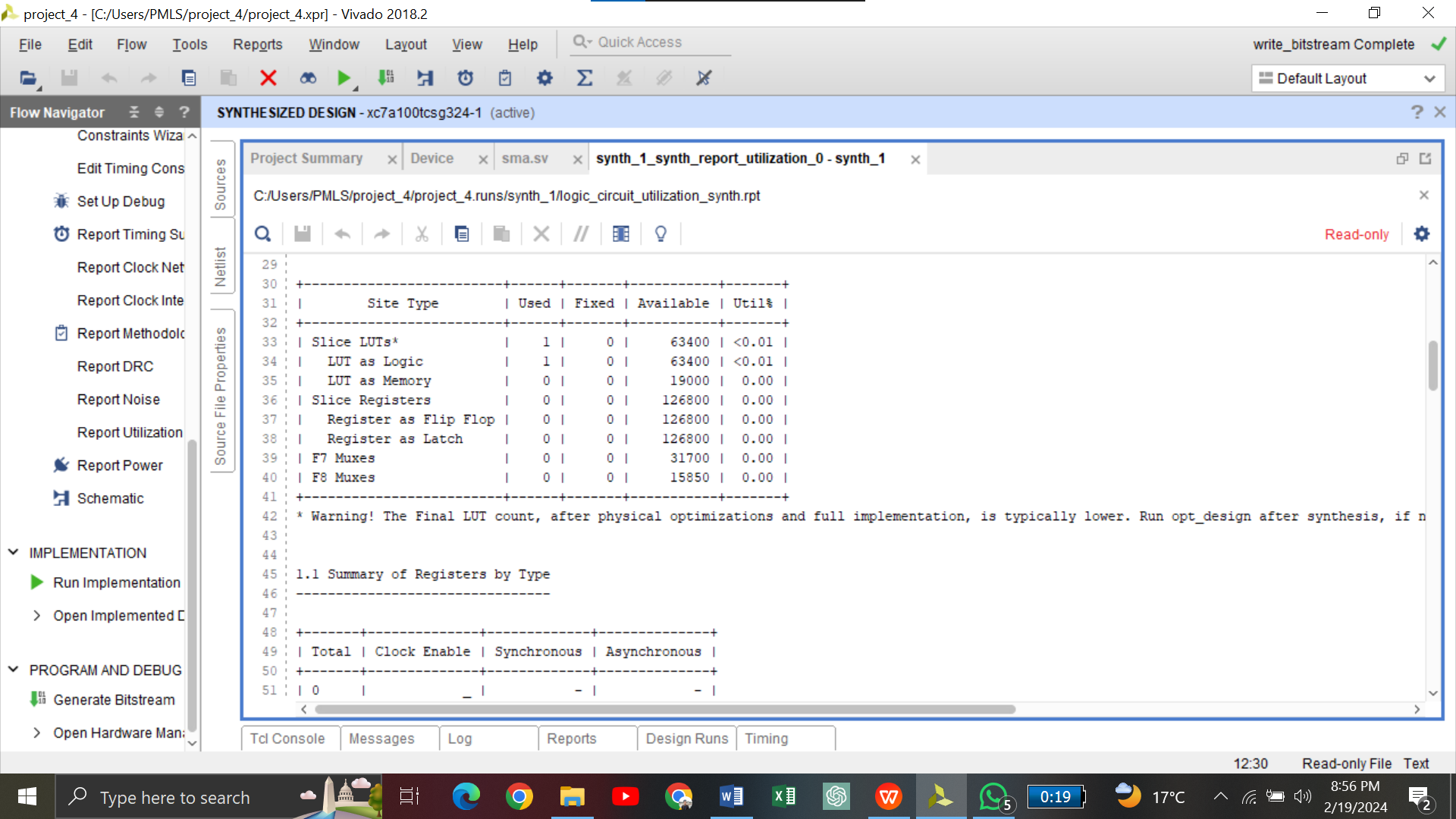
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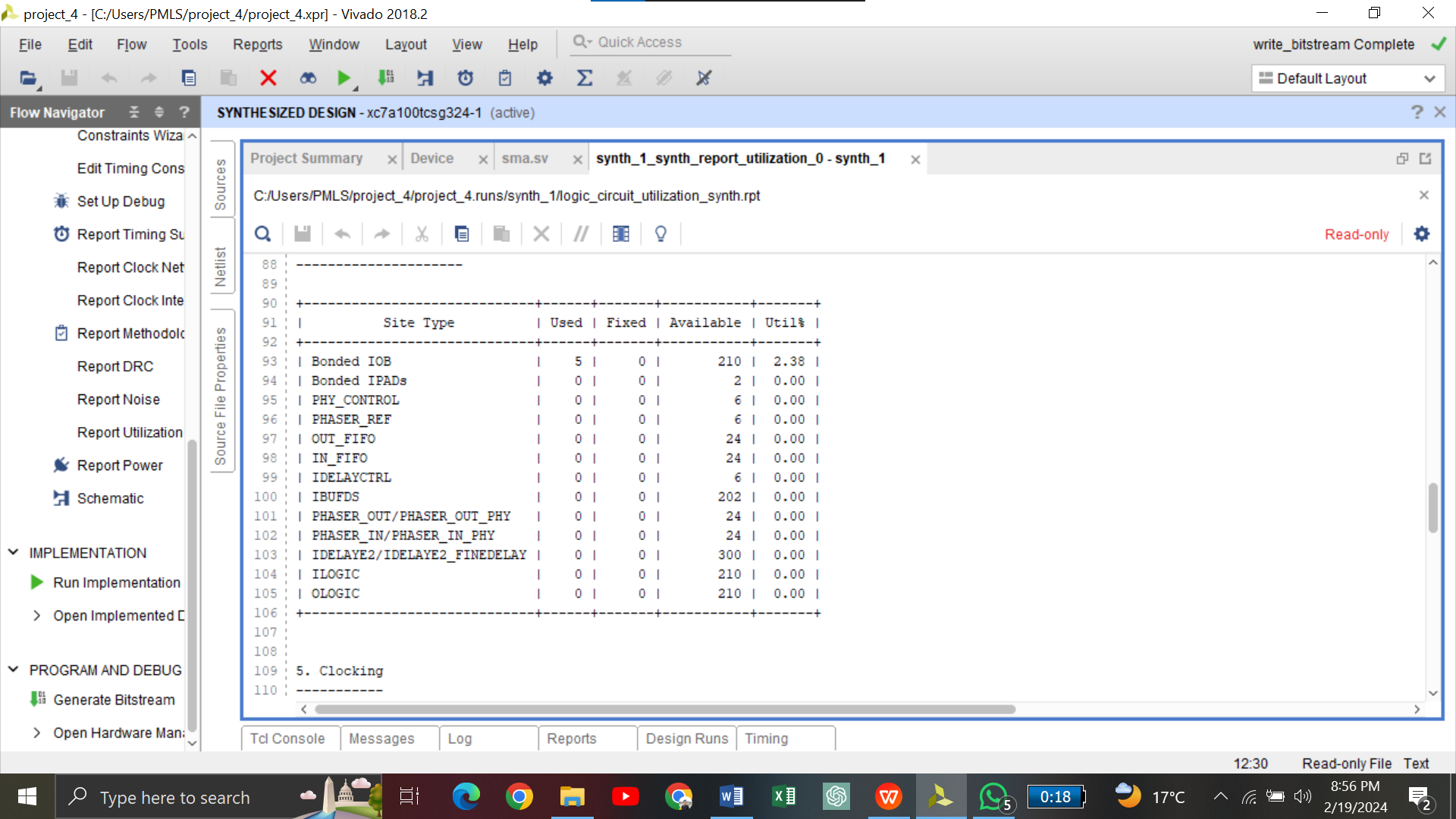
**( c )**

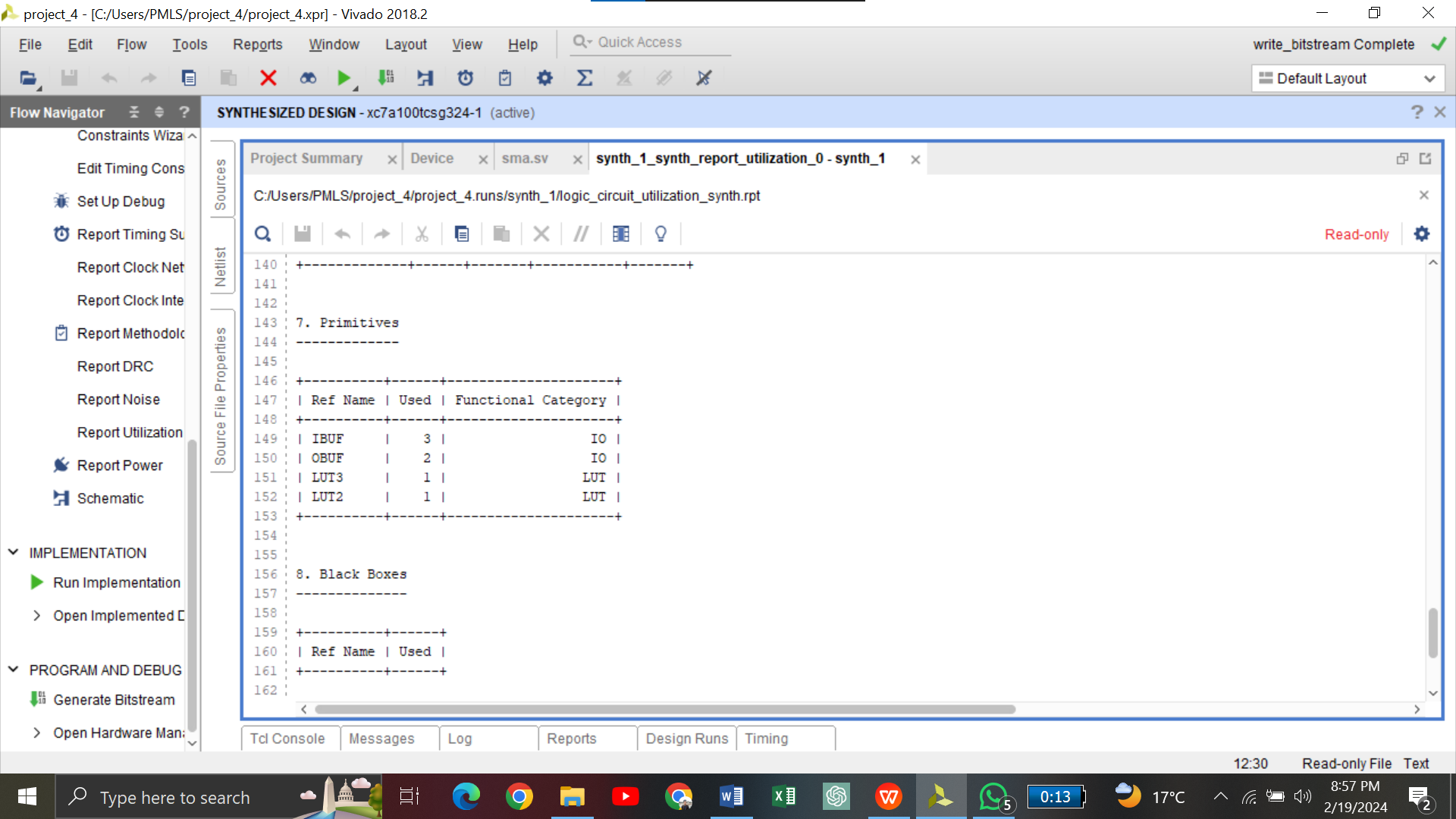
Total resources in the FPGA utilized are listed below.

1. Slice logic : 1 slice LUT used as a logic total available =63400
2. 5 Bonded IOB used , total available = 210
3. Premitives:

* 3 IBUF IO used
* 3 OBUF IO used
* 1 LUT3 used
* 1 LUT2 used

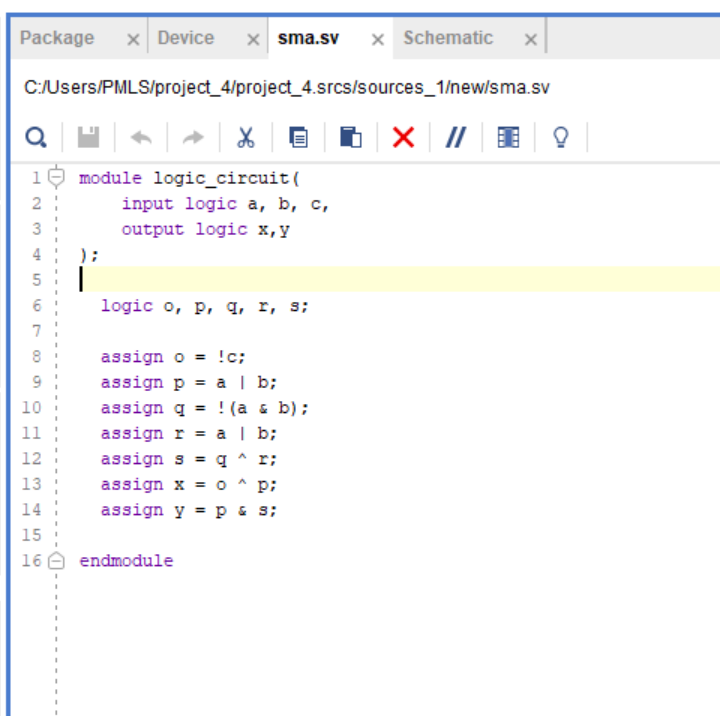


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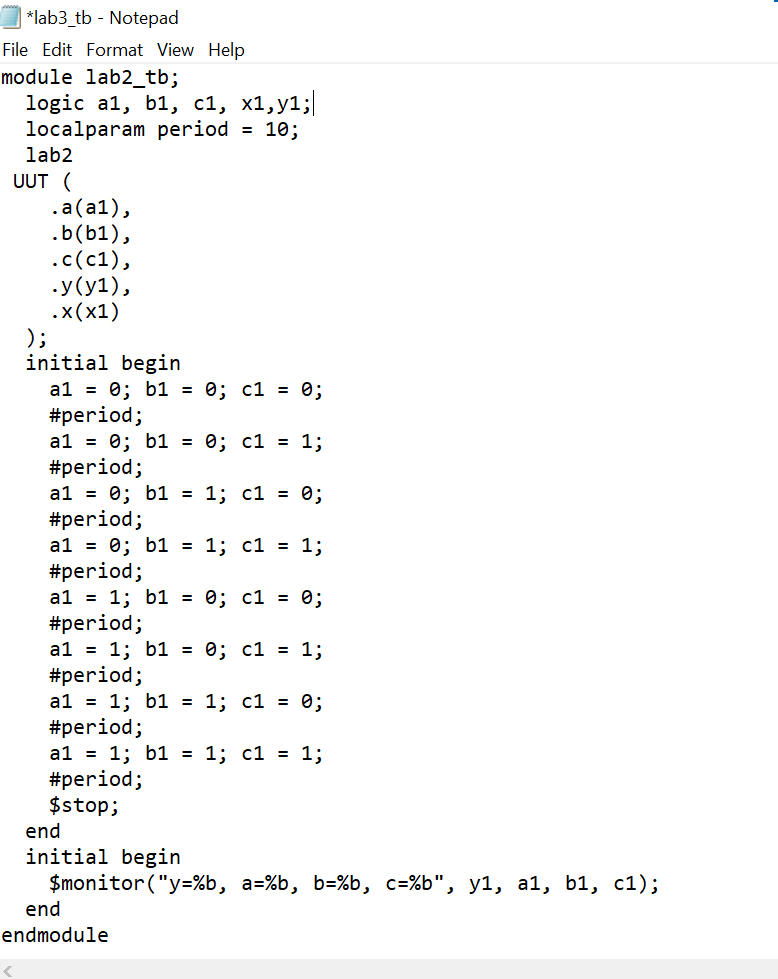
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**TASK\_2:**

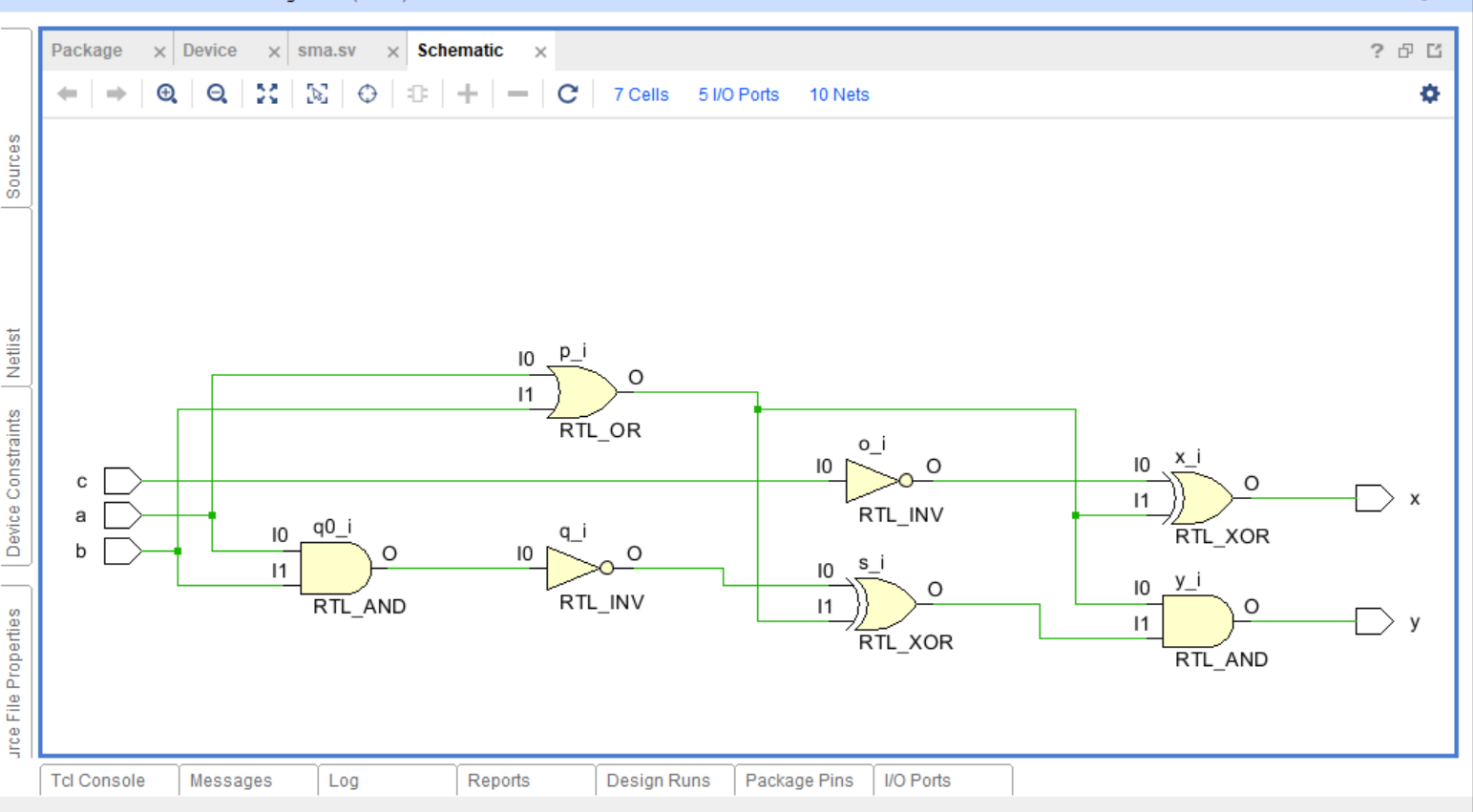
**Code1:**

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**TESTBENCH CODE:**

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**SCHEMATIC VERIFICATION:**

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