Code Genation

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- MIPS has 32 registers:
 - t0, ..., t9
 - a0, a1, a3, a4
 - v0, v1
 - sp, fp
 - ra
 - •
- We will work with MIPS32
 - 32-bit registers

- Arithmetic instructions operate on registers and constants:
 - add, sub, and, mul, div, or, xor, nor, ...

```
li $t0, 3
li $t1, 4
add $t2, $t0, $t1
mul $t3, t1, 7
```

Read from memory:

```
lw $t0,4($t1)
lw $t0,label
lw $t0,label+4
lw $t0,label+8($t1)
```

• Write to memory:

```
sw $t0,2($t1)
sw $t0,label
sw $t0,label+4
sw $t0,label+8($t1)
```

Branches and Jumps:

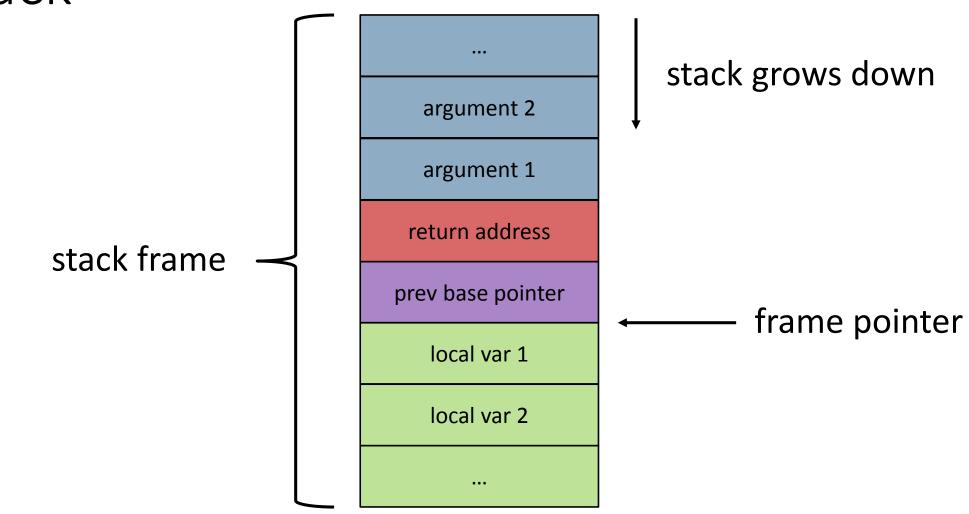
```
beq $t1, $t2, label
bne $t1, 7, label
j label
...
label:
```

- System calls:
 - Syscall number passed via v0
 - Arguments are passed via a0, a1, a2, a3
- For example, calling PrintInt(17):

```
li $v0, 1
li $a0, 17
syscall
```

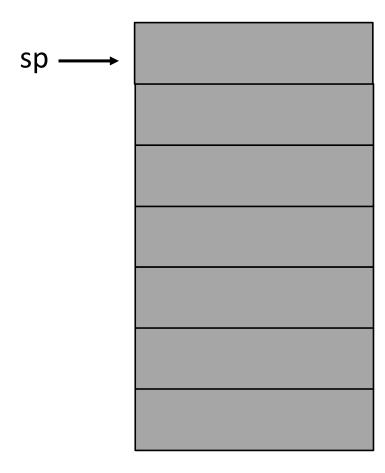
Stack Frames

- The stack consists of stack frame
- Each called function creates it's stack frame

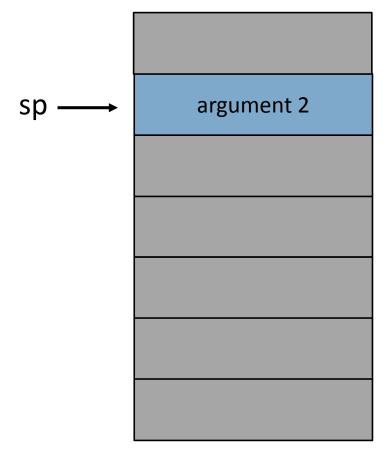


```
int f(int x, int y) {
   int z = x + y;
   return z;
}
int g() {
   int x = f(10, 20)
}
```

f: subu \$sp, \$sp, 4 sw \$ra, 0(\$sp) subu \$sp, \$sp, 4 sw \$fp, 0(\$sp) move \$fp, \$sp sub \$sp, \$sp, 16 lw \$t0, 8(\$fp) lw \$t1, 12(\$fp) add \$t2, \$t0, \$t1 sw \$t2, -4(\$fp)1w \$v0, -4 (\$fp)move \$sp, \$fp lw \$fp, 0(\$sp) lw \$ra, 4(\$sp) addu \$sp, \$sp, 8 jr \$ra



f: subu \$sp, \$sp, 4 sw \$ra, 0(\$sp) subu \$sp, \$sp, 4 sw \$fp, 0(\$sp) move \$fp, \$sp sub \$sp, \$sp, 16 lw \$t0, 8(\$fp) lw \$t1, 12(\$fp) sw \$t2, -4(\$fp)1w \$v0, -4(\$fp)move \$sp, \$fp lw \$fp, 0(\$sp) lw \$ra, 4(\$sp) addu \$sp, \$sp, 8 jr \$ra



f: subu \$sp, \$sp, 4 sw \$ra, 0(\$sp) subu \$sp, \$sp, 4 sw \$fp, 0(\$sp) move \$fp, \$sp sub \$sp, \$sp, 16 lw \$t0, 8(\$fp) lw \$t1, 12(\$fp) add \$t2, \$t0, \$t1 addu \$sp, \$sp, 8 sw \$t2, -4(\$fp)1w \$v0, -4(\$fp)move \$sp, \$fp lw \$fp, 0(\$sp) lw \$ra, 4(\$sp) addu \$sp, \$sp, 8 jr \$ra



f: subu \$sp, \$sp, 4 sw \$ra, 0(\$sp) subu \$sp, \$sp, 4 sw \$fp, 0(\$sp) move \$fp, \$sp sub \$sp, \$sp, 16 lw \$t0, 8(\$fp) lw \$t1, 12(\$fp) add \$t2, \$t0, \$t1 sw \$t2, -4(\$fp)1w \$v0, -4(\$fp)move \$sp, \$fp lw \$fp, 0(\$sp) lw \$ra, 4(\$sp) addu \$sp, \$sp, 8 jr \$ra



f: subu \$sp, \$sp, 4 sw \$ra, 0(\$sp) subu \$sp, \$sp, 4 sw \$fp, 0(\$sp) move \$fp, \$sp sub \$sp, \$sp, 16 lw \$t0, 8(\$fp) lw \$t1, 12(\$fp) add \$t2, \$t0, \$t1 sw \$t2, -4 (\$fp)1w \$v0, -4(\$fp)move \$sp, \$fp lw \$fp, 0(\$sp) lw \$ra, 4(\$sp) addu \$sp, \$sp, 8 jr \$ra

argument 2 argument 1 return address sp

f: subu \$sp, \$sp, 4 sw \$ra, 0(\$sp) subu \$sp, \$sp, 4 sw \$fp, 0(\$sp) move \$fp, \$sp sub \$sp, \$sp, 16 lw \$t0, 8(\$fp) lw \$t1, 12(\$fp) add \$t2, \$t0, \$t1 sw \$t2, -4(\$fp)1w \$v0, -4(\$fp)move \$sp, \$fp lw \$fp, 0(\$sp) lw \$ra, 4(\$sp) addu \$sp, \$sp, 8 jr \$ra

argument 2 argument 1 return address sp previous fp

f: subu \$sp, \$sp, 4 sw \$ra, 0(\$sp) subu \$sp, \$sp, 4 sw \$fp, 0(\$sp) move \$fp, \$sp sub \$sp, \$sp, 16 lw \$t0, 8(\$fp) lw \$t1, 12(\$fp) add \$t2, \$t0, \$t1 sw \$t2, -4 (\$fp)1w \$v0, -4 (\$fp)move \$sp, \$fp lw \$fp, 0(\$sp) lw \$ra, 4(\$sp) addu \$sp, \$sp, 8 jr \$ra

argument 2 argument 1 return address sp previous fp fp

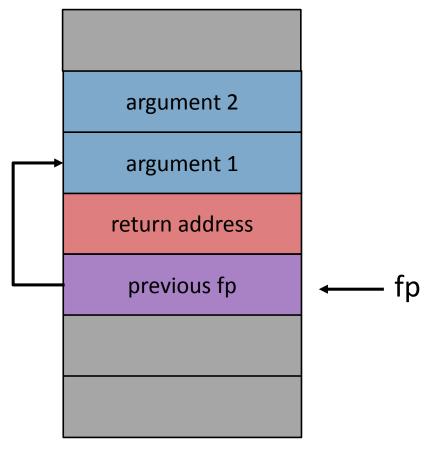
f: subu \$sp, \$sp, 4 sw \$ra, 0(\$sp) subu \$sp, \$sp, 4 sw \$fp, 0(\$sp) move \$fp, \$sp sub \$sp, \$sp, 16 lw \$t0, 8(\$fp) lw \$t1, 12(\$fp) add \$t2, \$t0, \$t1 sw \$t2, -4(\$fp)1w \$v0, -4 (\$fp)move \$sp, \$fp lw \$fp, 0(\$sp) lw \$ra, 4(\$sp) addu \$sp, \$sp, 8 jr \$ra

argument 2 argument 1 return address previous fp

f: subu \$sp, \$sp, 4 sw \$ra, 0(\$sp) subu \$sp, \$sp, 4 sw \$fp, 0(\$sp) move \$fp, \$sp sub \$sp, \$sp, 16 lw \$t0, 8(\$fp) lw \$t1, 12(\$fp) add \$t2, \$t0, \$t1 sw \$t2, -4 (\$fp)1w \$v0, -4 (\$fp)move \$sp, \$fp lw \$fp, 0(\$sp) lw \$ra, 4(\$sp) addu \$sp, \$sp, 8 jr \$ra

g: argument 2 argument 1 sw \$t0, 0(\$sp) lw \$t0, 8(\$fp) lw \$t1, 12(\$fp) jal f return address add \$t2, \$t0, \$t1 addu \$sp, \$sp, 8 sw \$t2, -4(\$fp)move \$t0, \$v0 previous fp lw \$v0, -4 (\$fp)move \$sp, \$fp lw \$fp, 0(\$sp) lw \$ra, 4(\$sp) addu \$sp, \$sp, 8 jr \$ra

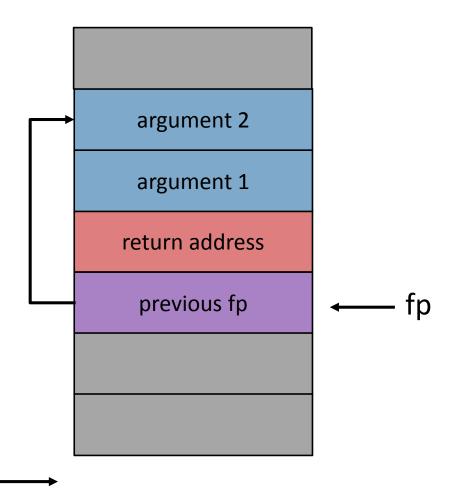
sp —



```
f:
subu $sp, $sp, 4
sw $ra, 0($sp)
subu $sp, $sp, 4
sw $fp, 0($sp)
move $fp, $sp
sub $sp, $sp, 16
lw $t0, 8($fp)
lw $t1, 12($fp)
add $t2, $t0, $t1
sw $t2, -4($fp)
1w $v0, -4 ($fp)
move $sp, $fp
lw $fp, 0($sp)
lw $ra, 4($sp)
addu $sp, $sp, 8
jr $ra
```

```
g:
li $t0, 20
subu $sp, $sp, 4
sw $t0, 0($sp)
li $t0, 10
subu $sp, $sp, 4
sw $t0, 0($sp)
jal f
addu $sp, $sp, 8
move $t0, $v0
```

sp



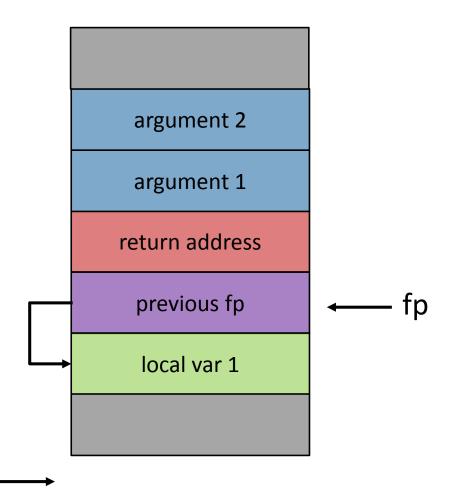
f: subu \$sp, \$sp, 4 sw \$ra, 0(\$sp) subu \$sp, \$sp, 4 sw \$fp, 0(\$sp) move \$fp, \$sp sub \$sp, \$sp, 16 lw \$t0, 8(\$fp) lw \$t1, 12(\$fp) add \$t2, \$t0, \$t1 sw \$t2, -4(\$fp)1w \$v0, -4 (\$fp)move \$sp, \$fp lw \$fp, 0(\$sp) lw \$ra, 4(\$sp) addu \$sp, \$sp, 8 jr \$ra

sp

argument 2 argument 1 return address previous fp fp local var 1

f: subu \$sp, \$sp, 4 sw \$ra, 0(\$sp) subu \$sp, \$sp, 4 sw \$fp, 0(\$sp) move \$fp, \$sp sub \$sp, \$sp, 16 lw \$t0, 8(\$fp) lw \$t1, 12(\$fp) add \$t2, \$t0, \$t1 sw \$t2, -4(\$fp) 1w \$v0, -4 (\$fp)move \$sp, \$fp lw \$fp, 0(\$sp) lw \$ra, 4(\$sp) addu \$sp, \$sp, 8 jr \$ra

sp



f: subu \$sp, \$sp, 4 sw \$ra, 0(\$sp) subu \$sp, \$sp, 4 sw \$fp, 0(\$sp) move \$fp, \$sp sub \$sp, \$sp, 16 lw \$t0, 8(\$fp) lw \$t1, 12(\$fp) add \$t2, \$t0, \$t1 sw \$t2, -4(\$fp)lw \$v0, -4(\$fp)move \$sp, \$fp lw \$fp, 0(\$sp) lw \$ra, 4(\$sp) addu \$sp, \$sp, 8 jr \$ra

argument 2 argument 1 return address previous fp sp local var 1

f: subu \$sp, \$sp, 4 sw \$ra, 0(\$sp) subu \$sp, \$sp, 4 sw \$fp, 0(\$sp) move \$fp, \$sp sub \$sp, \$sp, 16 lw \$t0, 8(\$fp) lw \$t1, 12(\$fp) add \$t2, \$t0, \$t1 sw \$t2, -4(\$fp)1w \$v0, -4 (\$fp)move \$sp, \$fp lw \$fp, 0(\$sp) lw \$ra, 4(\$sp) addu \$sp, \$sp, 8 jr \$ra

argument 2 argument 1 return address previous fp sp local var 1

f: subu \$sp, \$sp, 4 sw \$ra, 0(\$sp) subu \$sp, \$sp, 4 sw \$fp, 0(\$sp) move \$fp, \$sp sub \$sp, \$sp, 16 lw \$t0, 8(\$fp) lw \$t1, 12(\$fp) add \$t2, \$t0, \$t1 sw \$t2, -4 (\$fp)1w \$v0, -4 (\$fp)move \$sp, \$fp lw \$fp, 0(\$sp) lw \$ra, 4(\$sp) addu \$sp, \$sp, 8 jr \$ra

argument 2 argument 1 sp return address previous fp local var 1

f: subu \$sp, \$sp, 4 sw \$ra, 0(\$sp) subu \$sp, \$sp, 4 sw \$fp, 0(\$sp) move \$fp, \$sp sub \$sp, \$sp, 16 lw \$t0, 8(\$fp) lw \$t1, 12(\$fp) add \$t2, \$t0, \$t1 sw \$t2, -4 (\$fp)1w \$v0, -4 (\$fp)move \$sp, \$fp lw \$fp, 0(\$sp) lw \$ra, 4(\$sp) addu \$sp, \$sp, 8 jr \$ra

argument 2 argument 1 sp return address previous fp local var 1

f: subu \$sp, \$sp, 4 sw \$ra, 0(\$sp) subu \$sp, \$sp, 4 sw \$fp, 0(\$sp) move \$fp, \$sp sub \$sp, \$sp, 16 lw \$t0, 8(\$fp) lw \$t1, 12(\$fp) add \$t2, \$t0, \$t1 sw \$t2, -4(\$fp)1w \$v0, -4 (\$fp)move \$sp, \$fp lw \$fp, 0(\$sp) lw \$ra, 4(\$sp) addu \$sp, \$sp, 8 jr \$ra

argument 2 argument 1 sp return address previous fp local var 1

```
f:
          subu $sp, $sp, 4
          sw $ra, 0($sp)
          subu $sp, $sp, 4
          sw \$fp, 0(\$sp) sw \$t0, 0(\$sp)
          move $fp, $sp
          sub $sp, $sp, 16
          lw $t0, 8($fp)
          lw $t1, 12($fp)
          add $t2, $t0, $t1 addu $sp, $sp, 8
          sw $t2, -4($fp)
          1w $v0, -4($fp)
        move $sp, $fp
lw $fp, 0($sp)
lw $ra, 4($sp)
addu $sp, $sp, 8
```

```
g:
li $t0, 20
subu $sp, $sp, 4
li $t0, 10
subu $sp, $sp, 4
sw $t0, 0($sp)
jal f
move $t0, $v0
```

sp argument 2 argument 1 return address previous fp local var 1

f: subu \$sp, \$sp, 4 sw \$ra, 0(\$sp) subu \$sp, \$sp, 4 sw \$fp, 0(\$sp) move \$fp, \$sp sub \$sp, \$sp, 16 lw \$t0, 8(\$fp) lw \$t1, 12(\$fp) add \$t2, \$t0, \$t1 sw \$t2, -4(\$fp)1w \$v0, -4 (\$fp)move \$sp, \$fp lw \$fp, 0(\$sp) lw \$ra, 4(\$sp) addu \$sp, \$sp, 8 jr \$ra

sp argument 2 argument 1 return address previous fp local var 1

f: subu \$sp, \$sp, 4 sw \$ra, 0(\$sp) subu \$sp, \$sp, 4 sw \$fp, 0(\$sp) move \$fp, \$sp sub \$sp, \$sp, 16 lw \$t0, 8(\$fp) lw \$t1, 12(\$fp) add \$t2, \$t0, \$t1 sw \$t2, -4(\$fp)1w \$v0, -4 (\$fp)move \$sp, \$fp lw \$fp, 0(\$sp) lw \$ra, 4(\$sp) addu \$sp, \$sp, 8 jr \$ra

- Our IR is likely to use too many registers
- Assume for now, that the number of IR registers is reduced
 - Every IR register mapped to a CPU register (t0, ... t7)
- We will see later how to compute this register allocation

- Translate global variable initializations
- Translate the IR instructions for each function
 - Implement a translation function for each IR instruction
 - If the translation requires additional registers:
 - Use registers s0, s1, ...

Global initializations

Assignments (constant)

li \$t1, c

- Assignments (read from memory)
- For local variables and parameters:

- Assignments (write to memory)
- For local variables and parameters:

$$x = t1$$

$$\downarrow$$
sw \$t1, off(\$fp)

- Assignments (read from memory)
- For global variables:

```
t1 = g_var

g_var: .word 17
...
lw $t1, g_var
```

- Assignments (write to memory)
- For global variables:

```
g_var = t1

g_var: .word 17
...
sw $t1, g_var
```

• Arithmetic operation

Arithmetic operation

```
t0 = add t1, t2
add $t0, $t1, $t2
ble $t0, max, end
li $t0, max
end:
# more checks...
```

• Branch

```
branch_eq t1, t2, label
```



beq \$t1, \$t2, label

Function call

```
t0 = call f(t1, t2)
   sw $t1, 0($sp)
   subu $sp, $sp, 4
   sw $t2, 0($sp)
   subu $sp, $sp, 4
   jal f
   addu $sp, $sp, 8
   move $t0, $v0
```

- Return (in a function f)
- Store result in **v0** and jump to f's **epilogue label** (f_epilogue)

return t1

move \$v0, \$t1

j f epilogue

Another example

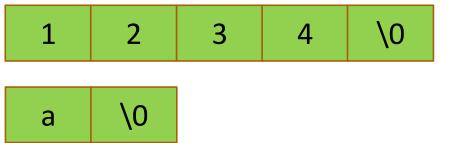
```
int g = 70;
int f(int x) {
   int z = x;
   if (z) {
      z = g
   }
   return z;
}
```

```
t1 = x
z = t1
t1 = z
beq t1, 0, end
t1 = g
z = t1
end:
return z
```

```
.data
g: .word 70
.text
f:
# prologue here
lw $t1, 8($fp)
sw $t1, -4($fp)
lw $t1, -4($fp)
beq $t1, 0, end
lw $t1, g
sw $t1, -4($fp)
end:
lw $t1, -4($fp)
move $v0s, $t1
f epilogue:
# epilogue here...
```

- We use null terminated strings
- Every character is one byte

```
string s1 = "1234";
string s2 = "a";
...
```



• Assume that s1 and s2 are strings

```
if (s1 == s2) {
}
```

```
t1 = s1;
t2 = s2;
t3 = str_eq t1, t2
compare t3, 0
...
```

Inline string comparison

```
t1 = s1;
t2 = s2;
t3 = str_eq t1, t2
compare t3, 0
...
```

```
lw $t1, -4($fp) // local var 1
lw $t2, -8($fp) // local var 2
li $t3, 1 // result
move $s0, $t1
move $s1, $t2
str eq loop:
1b $s2, 0($s0)
1b $s3, 0($s1)
bne $s2, $s3, neg label
beq $s2, 0, str eq end
addu $s0, $s0, 1
addu $s1, $s1, 1
j str eq loop
neq_label:
li $t3, 0
str eq end:
```

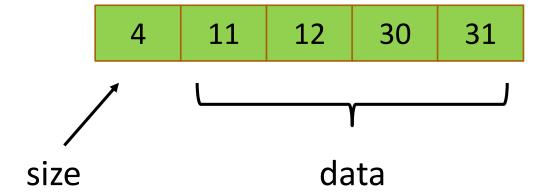
Alternatively, create a function str_eq

```
t1 = s1;
t2 = s2;
t3 = str_eq t1, t2
compare t3, 0
...
```

```
lw $t1, -4($fp) // local var 1
lw $t2, -8($fp) // local var 2
subu $sp, $sp, 4
sw $t2, 0($sp)
subu $sp, $sp, 4
sw $t1, 0($sp)
jal str_eq
addu $sp, $sp, 8
move $t3, $v0
```

Arrays

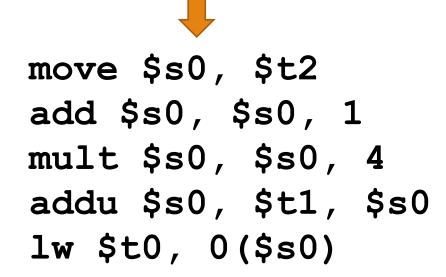
- Each cell is 4 bytes (int or pointer)
- First cell is the **size** of the array
- The rest of the cells contain data



Arrays

Array access

```
t0 = array_access t1, t2
```



Division by zero

$$t0 = div t1, t2$$

div \$t0, \$t1, \$t2

Division by zero

```
t0 = div t1, t2
```

```
beq $t2, 0, abort
div $t0, $t1, $t2
...
abort:
li $v0, 10
syscall
```

Out of bounds array access

```
t0 = array_access t1, t2
```

```
move $s0, $t2
add $s0, $s0, 1
mult $s0, $s0, 4
addu $s0, $t1, $s0
lw $t0, 0($s0)
```

Out of bounds array access

```
t0 = array_access t1, t2
```

```
bltz $t2, abort
lw $s0, 0($t1)
bge $t2, $s0, abort
move $s0, $t2
add $s0, $s0, 1
mult $s0, $s0, 4
addu $s0, $t1, $s0
lw $t0, 0($s0)
abort:
li $v0, 10
syscall
```

- Null pointer dereference
 - Arrays
 - Field access
 - Method calls

- Null pointer dereference
- For example, in arrays:

```
t0 = array_access t1, t2
```

```
beq $t1, abort
move $s0, $t2
add $s0, $s0, 1
mult $s0, $s0, 4
addu $s0, $t1, $s0
lw $t0, 0($s0)
abort:
li $v0, 10
syscall
```

- Null pointer dereference
- For example, in field accesses:

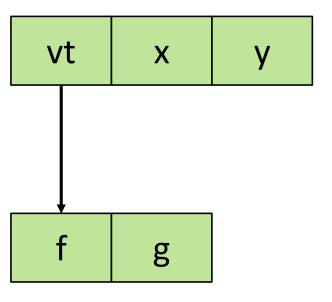
```
t0 = field_access t1, foo
```

```
beq $t1, 0, abort
move $t0, off($t1)
...
abort:
li $v0, 10
syscall
```

Classes

Class Layout

```
class A {
  int x;
  string y;
  int f() { ...
  int g() { ...
}
```

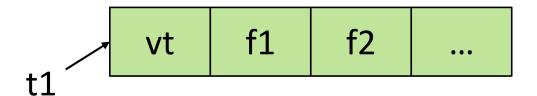


Class Layout

```
class A {
  int x;
  string y;
                                vt
                                       X
  int f() { ...
  int g() { ... -.
                                                          B's layout
class B extends A {
  int z;
  int f() { ...
  int h() {
```

Field Access

```
t0 = field_access t1, f2 move $t0, 8($t1)
```



Field Access

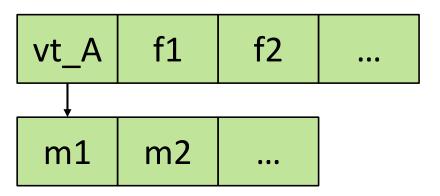
```
t0 = field_access t1, f2
```

```
vt f1 f2 ...
```

```
beq $t1, 0, abort
move $t0, 8($t1)
...
abort:
li $v0, 10
syscall
```

```
class A {
  int f1;
  ...
  int m1() { ...
  ...
}

A a = new A;
```



```
class A {
  int f1 = c;
  ...
  int m1() { ...
  ...
}

A a = new A;
```

```
t0 = alloc (size)
set_vt t0, A
t1 = c
field_set t0, f1, t
```

```
t0 = alloc (size)
set_vt t0, A
t1 = c
field_set t0, f1, t1
...
```

```
m1 m2 ...

Virtual Table
```

```
.data
vt_A: .word m1, m2, ...
```

```
t0 = alloc (size)
set_vt t0, A
t1 = c
field_set t0, f1, t1
...
```

```
m1 m2 ...

Virtual Table
```

```
.data
vt_A: .word m1, m2, ...
.text
li $v0, 9
li $a0, size
syscall
move $t0, $v0
```

```
t0 = alloc (size)
set_vt t0, A
t1 = c
field_set t0, f1, t1
...
```

```
m1 m2 ...

Virtual Table
```

```
.data
vt A: .word m1, m2, ...
.text
li $v0, 9
li $a0, size
syscall
move $t0, $v0
la $s0, vt A
sw $s0, 0($t0)
```

```
t0 = alloc (size)
set_vt t0, A
t1 = c
field_set t0, f1, t1
...
```

```
m1 m2 ...

Virtual Table
```

```
.data
vt A: .word m1, m2, ...
.text
li $v0, 9
li $a0, size
syscall
move $t0, $v0
la $s0, vt A
sw $s0, 0($t0)
li $t1, c
```

```
t0 = alloc (size)
set_vt t0, A
t1 = c
field_set t0, f1, t1
...
```

```
m1 m2 ...

Virtual Table
```

```
.data
vt A: .word m1, m2, ...
.text
li $v0, 9
li $a0, size
syscall
move $t0, $v0
la $s0, vt A
sw $s0, 0($t0)
li $t1, c
sw $t1, 4($t0)
```

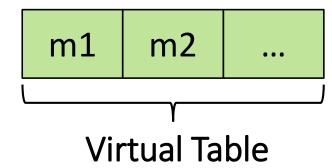
```
class A {
  int f1 = c;
  ...
  int m1(int x) { ...
  int m2(int x) { ...
}

A a = new A;
  z = a.m2(7)
```

```
t0 = a
t1 = 7
t2 = virtual_call t0, m2, t1
z = t2
```

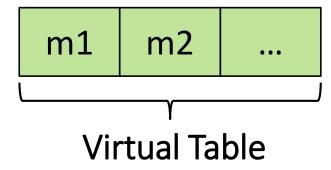
```
t0 = a
t1 = 7
t2 = virtual_call t0, m2, t1
z = t2
```

```
subu $sp, $sp, 4
sw $t1, 0($sp)
```



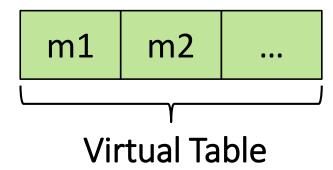
```
t0 = a
t1 = 7
t2 = virtual_call t0, m2, t1
z = t2
```

```
subu $sp, $sp, 4
sw $t1, 0($sp)
subu $sp, $sp, 4
sw $t0, 0($sp)
```



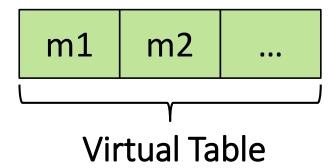
```
t0 = a
t1 = 7
t2 = virtual_call t0, m2, t1
z = t2
```

```
subu $sp, $sp, 4
sw $t1, 0($sp)
subu $sp, $sp, 4
sw $t0, 0($sp)
lw $s0, 0($t0)
```



```
t0 = a
t1 = 7
t2 = virtual_call t0, m2, t1
z = t2
```

```
subu $sp, $sp, 4
sw $t1, 0($sp)
subu $sp, $sp, 4
sw $t0, 0($sp)
lw $s0, 0($t0)
lw $s1, 4($s0)
```



```
t0 = a
t1 = 7
t2 = virtual_call t0, m2, t1
z = t2
```

```
m1 m2 ...

Virtual Table
```

```
subu $sp, $sp, 4
sw $t1, 0($sp)
subu $sp, $sp, 4
sw $t0, 0($sp)
lw $s0, 0($t0)
lw $s1, 4($s0)
jalr $s1
addu $sp, $sp, 8
```

SPIM

```
.data
                                  .text
PrintInt(17) = \begin{cases} 1i & v0, 1 \\ 1w & a0, 17 \\ syscall \end{cases} PrintStr("hello") = \begin{cases} 1i & v0, 4 \\ 1i & a0, g_str_syscall \end{cases}
```

SPIM

- Runing SPIM:
 - spim –f input_file
- Interactive debugging:
 - xspim
- Tutorials:
 - https://courses.cs.washington.edu/courses/cse410/08sp/notes/spim/SpimTu torial.pdf
 - https://web.stanford.edu/class/cs143/materials/SPIM_Manual.pdf