

# Register Allocation

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# MIPS Architecture

- MIPS has 32 registers:
  - t0, ..., t9
  - a0, a1, a3, a4
  - v0, v1
  - sp, fp
  - ra
  - ...
- We will work with MIPS32
  - 32-bit registers

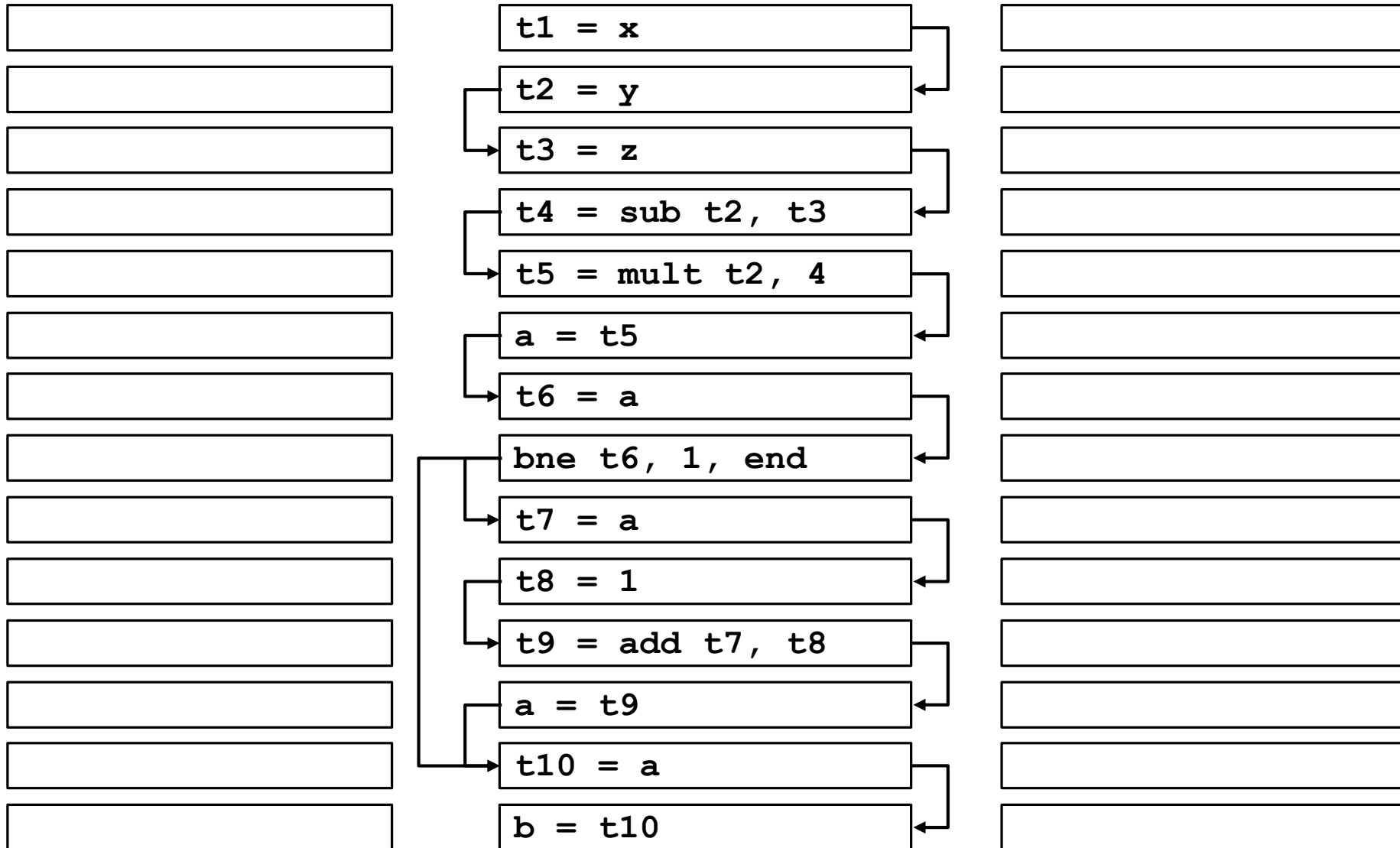
# Control Flow Graph

- TODO

# Control Flow Graph

```
a = x * (y - z)
if (a) {
    a = a + 1;
}
b = a
```

```
t1 = x
t2 = y
t3 = z
t4 = sub t2, t3
t5 = mult, t1, t4
a = t5
t6 = a
bne t6, 1, end
t7 = a
t8 = 1
t9 = add t7, t8
a = t9
end:
t10 = a
b = t10
```



```
t1 = x
t2 = y
t3 = z
t4 = sub t
t5 = mult,
a = t5
t6 = a
bne t6, 1,
t7 = a
t8 = 1
t9 = add t
a = t9
end:
t10 = a
b = t10
```

# Liveness Analysis

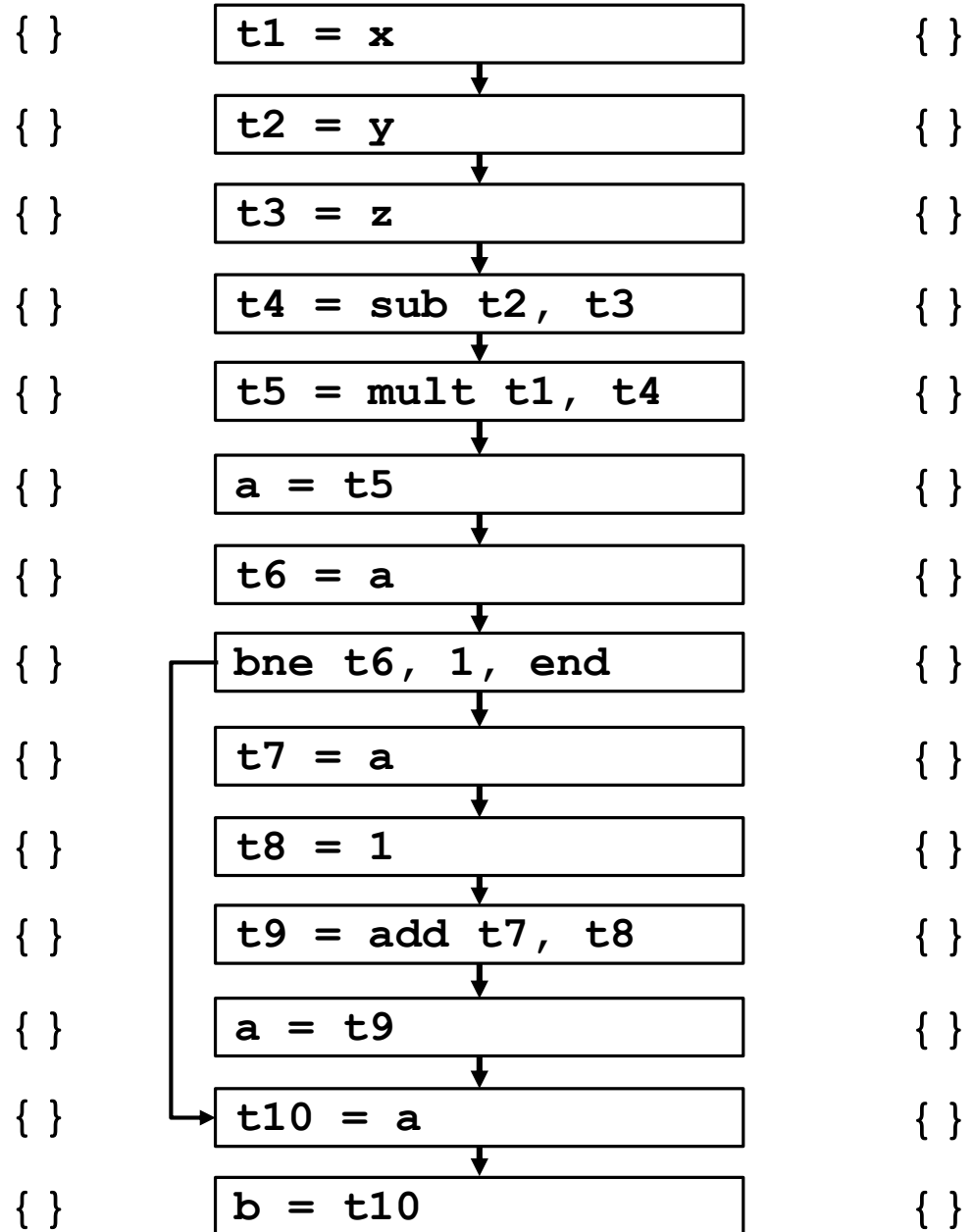
- TODO

# Liveness Analysis

- First pass

IN

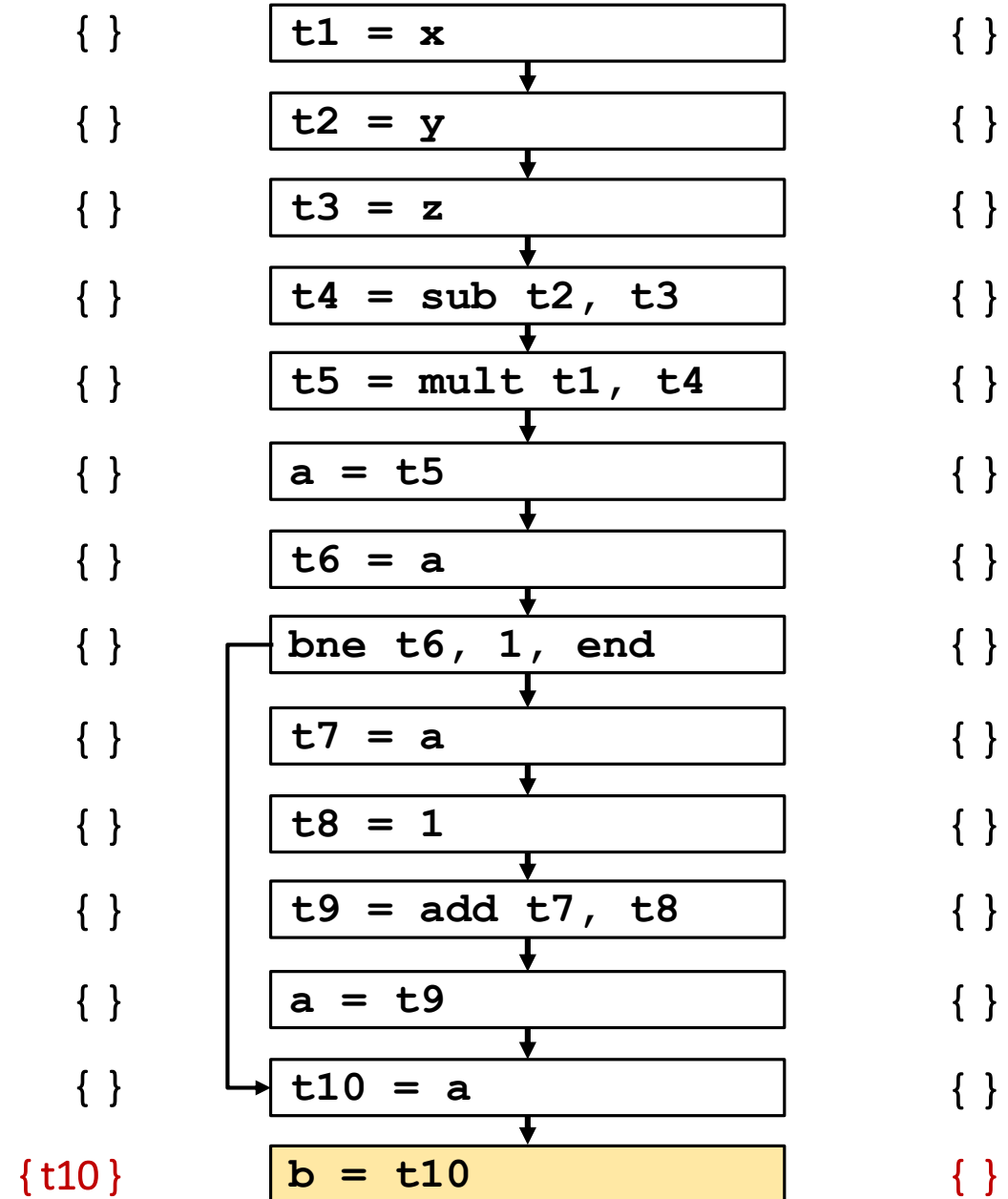
OUT

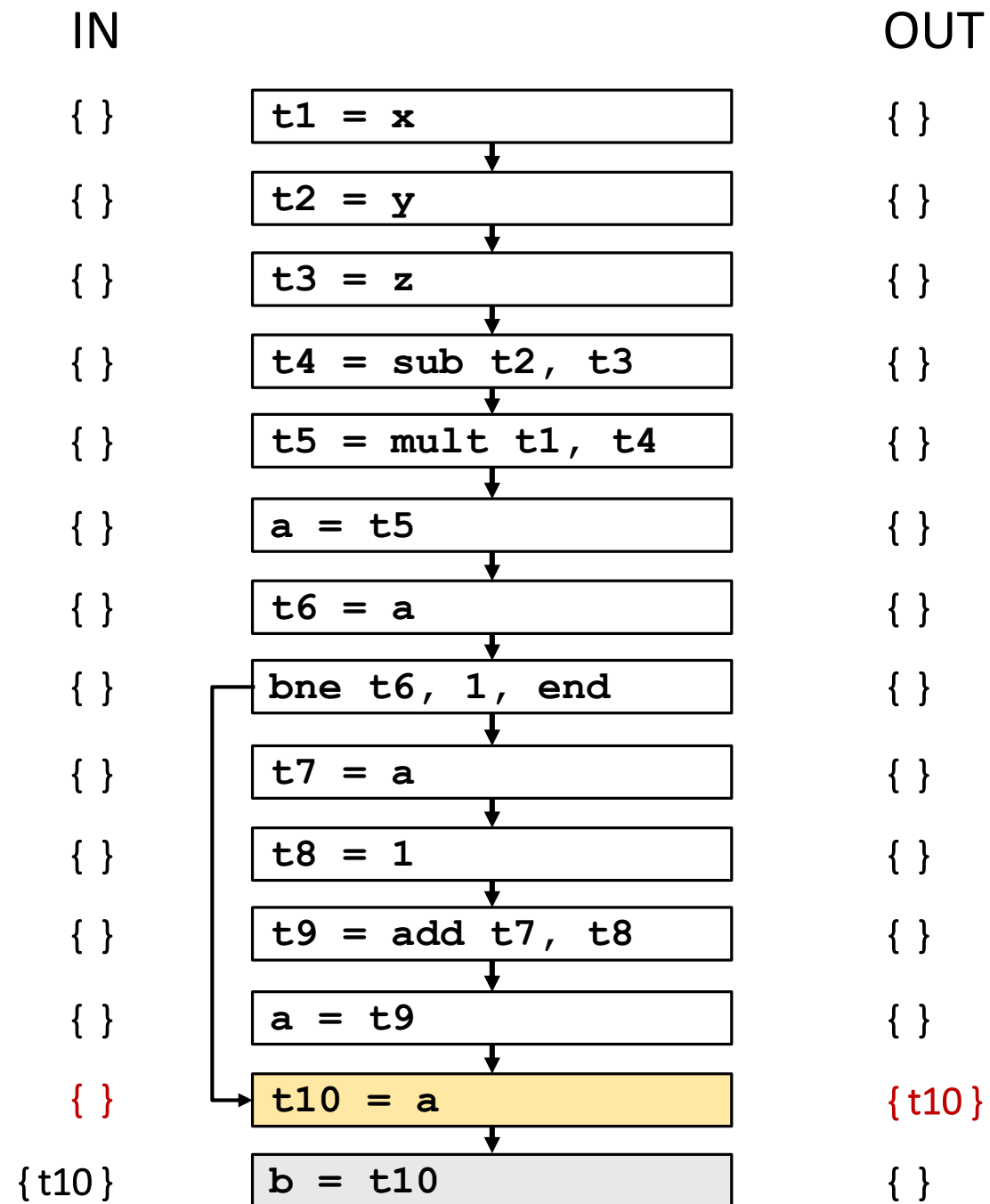


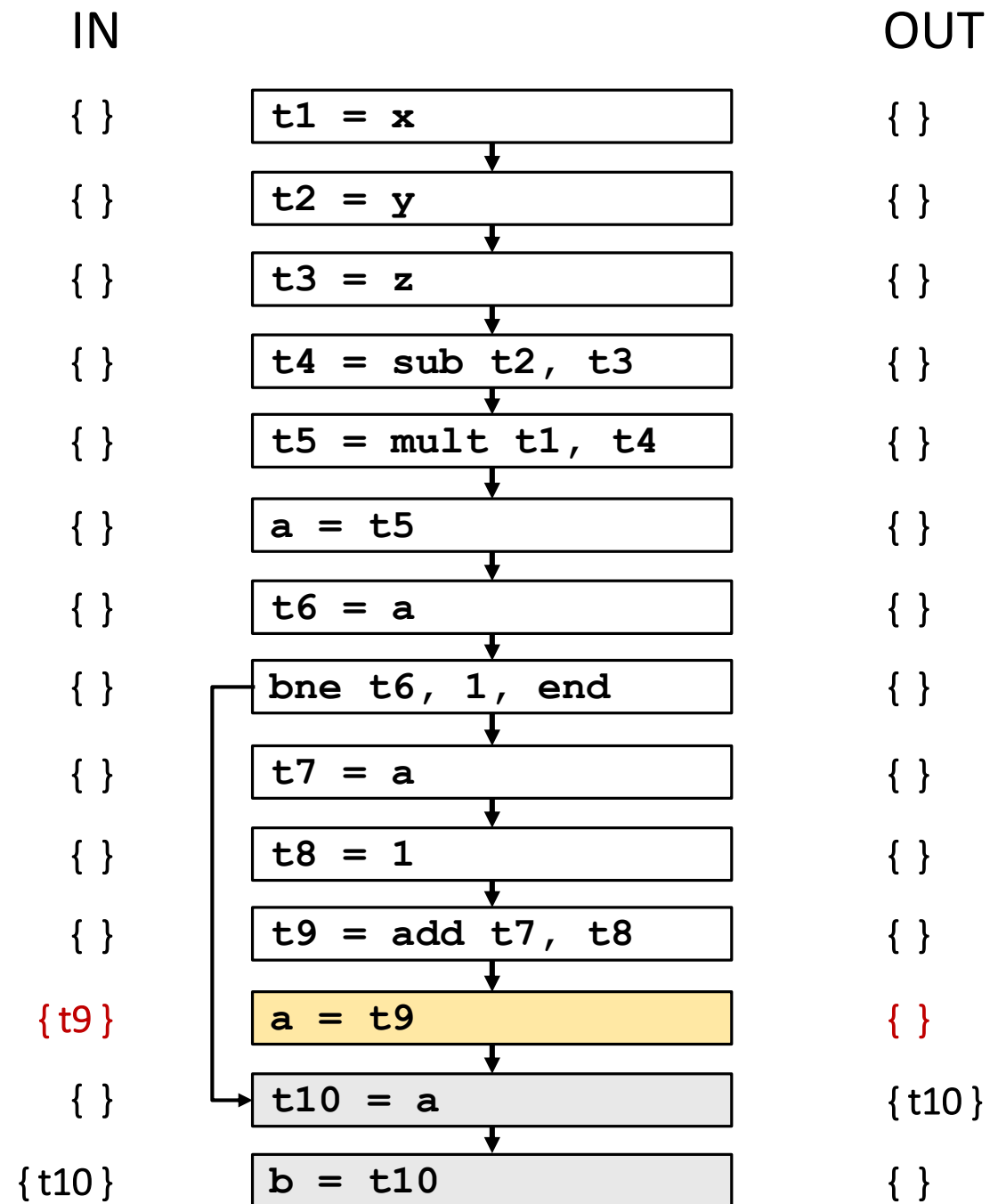


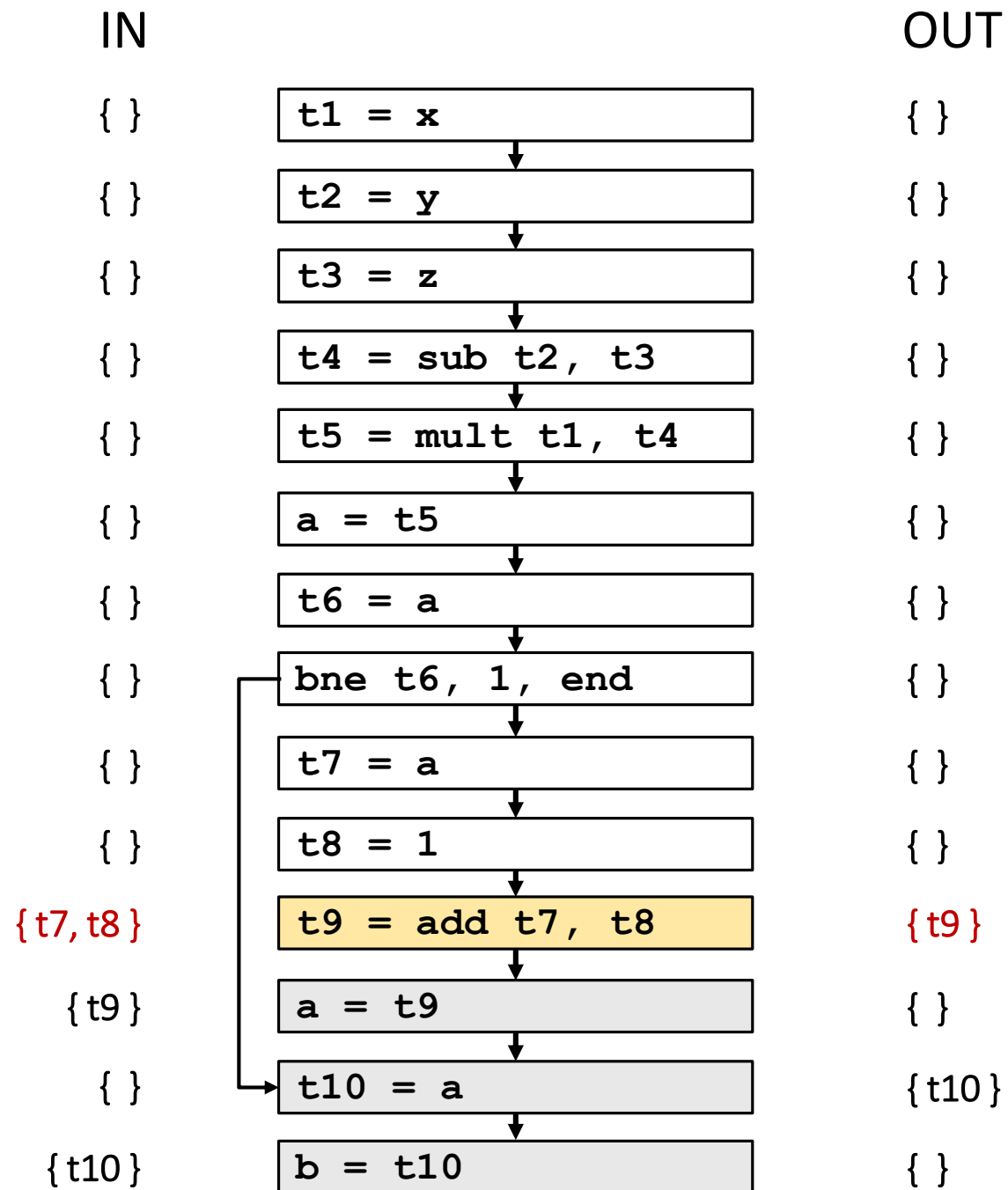
IN

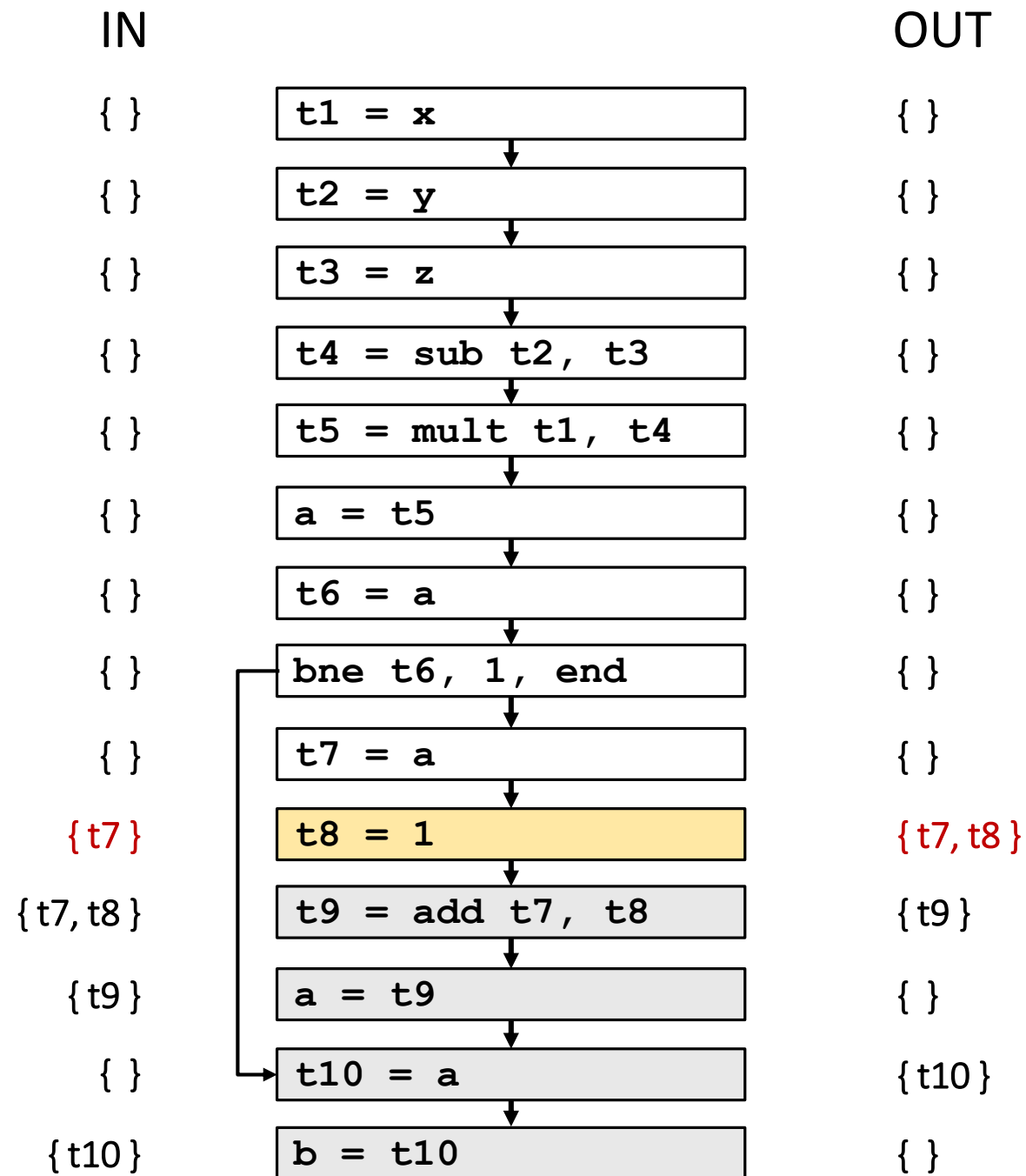
OUT

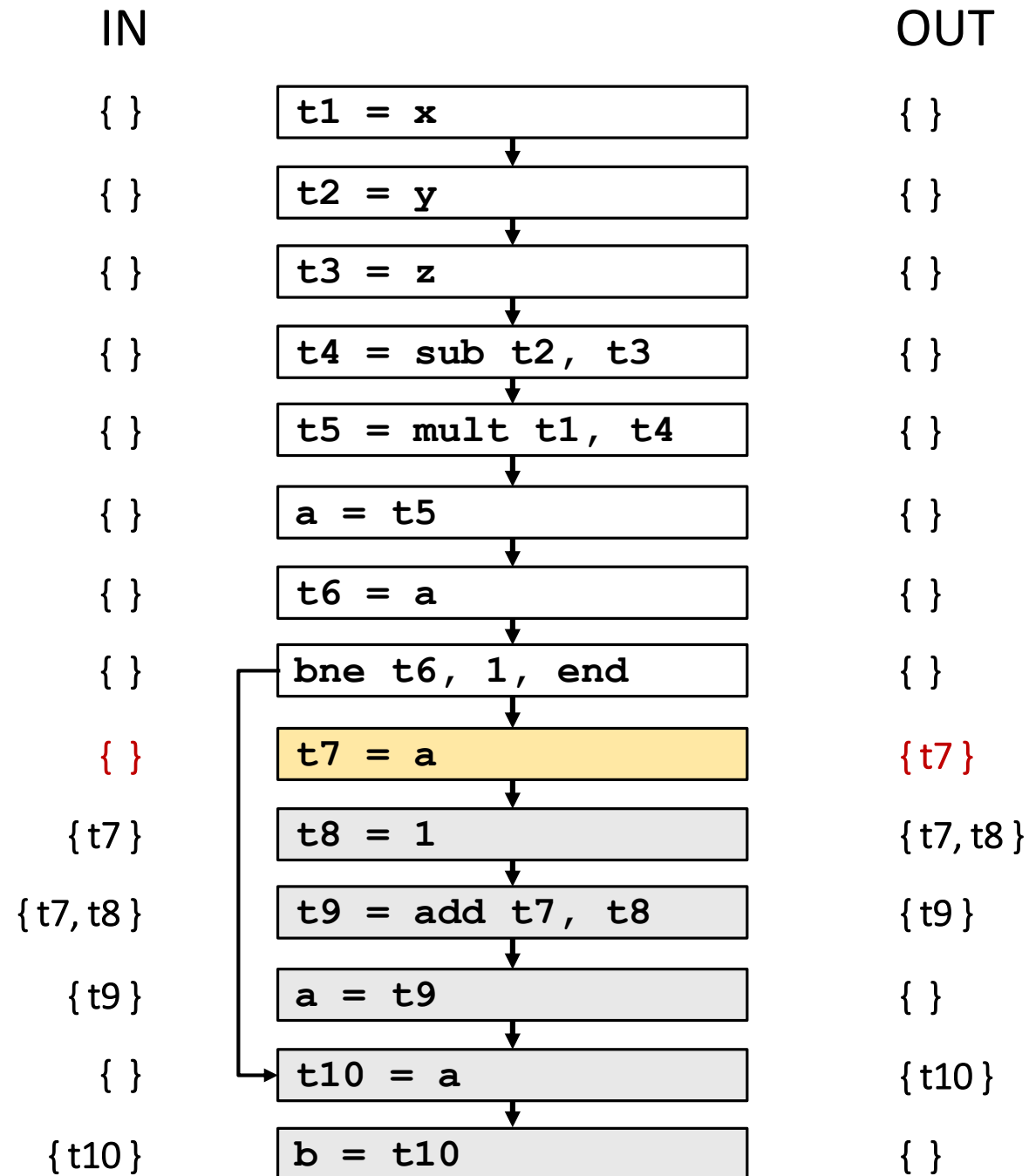


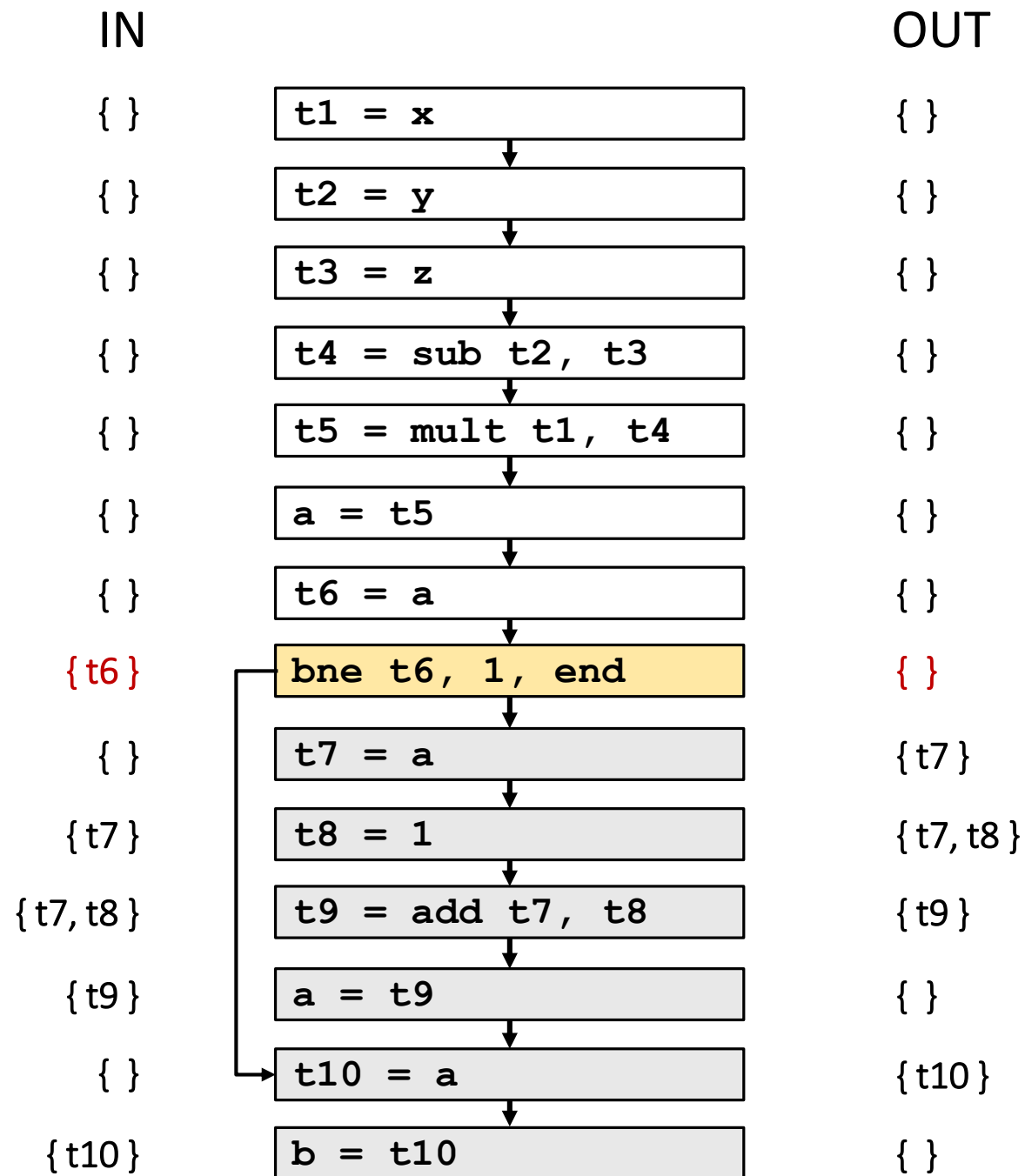


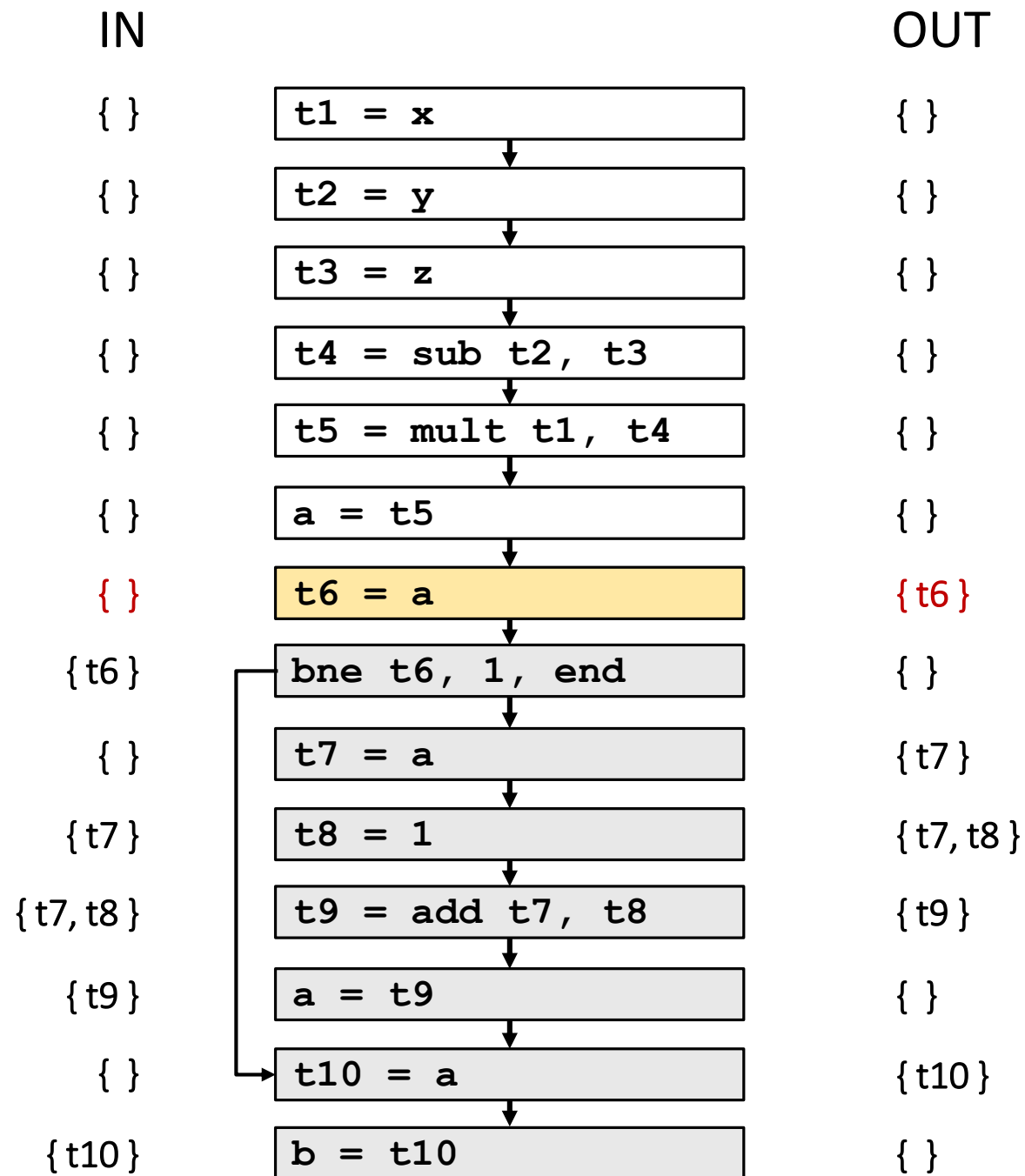




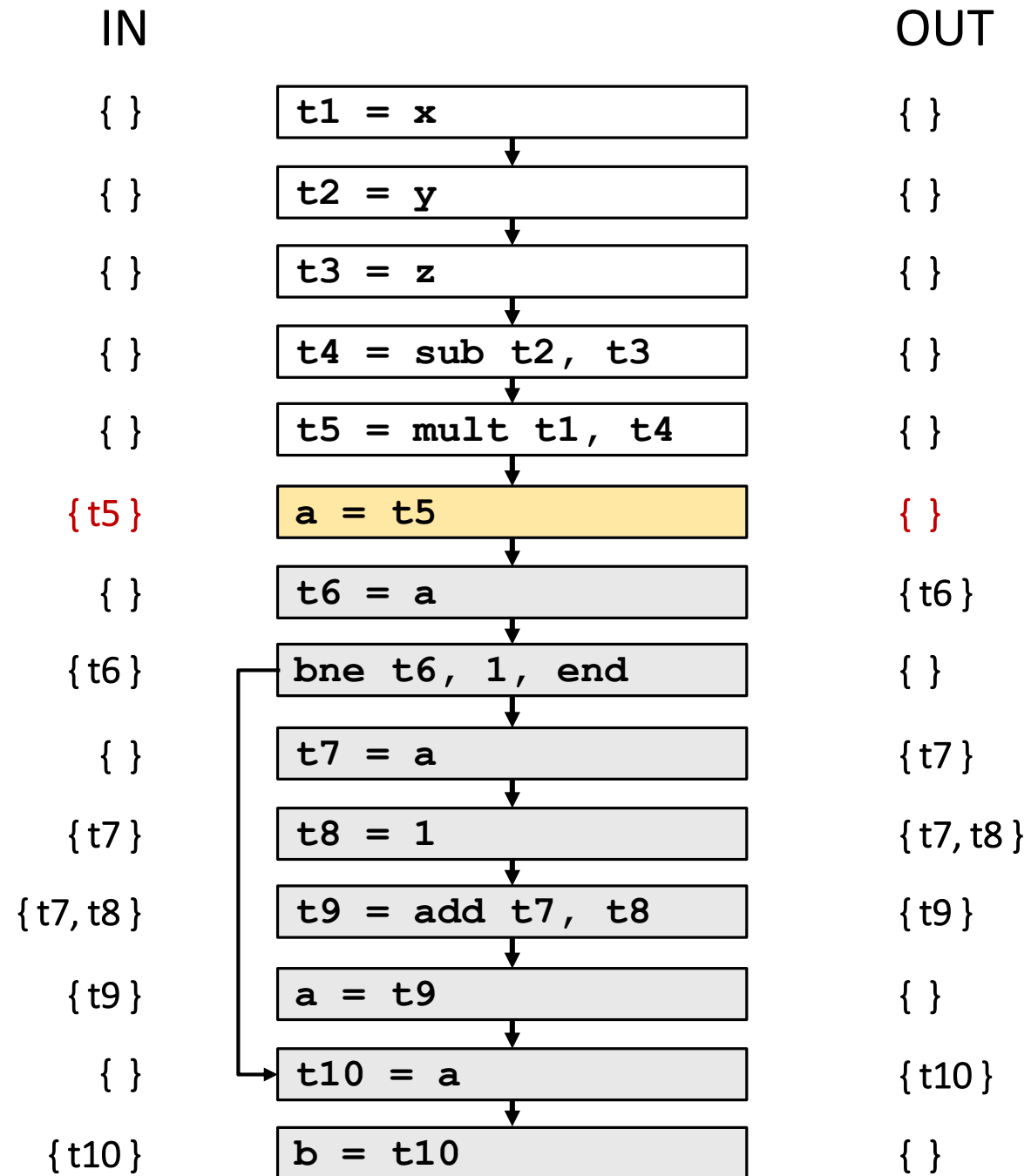


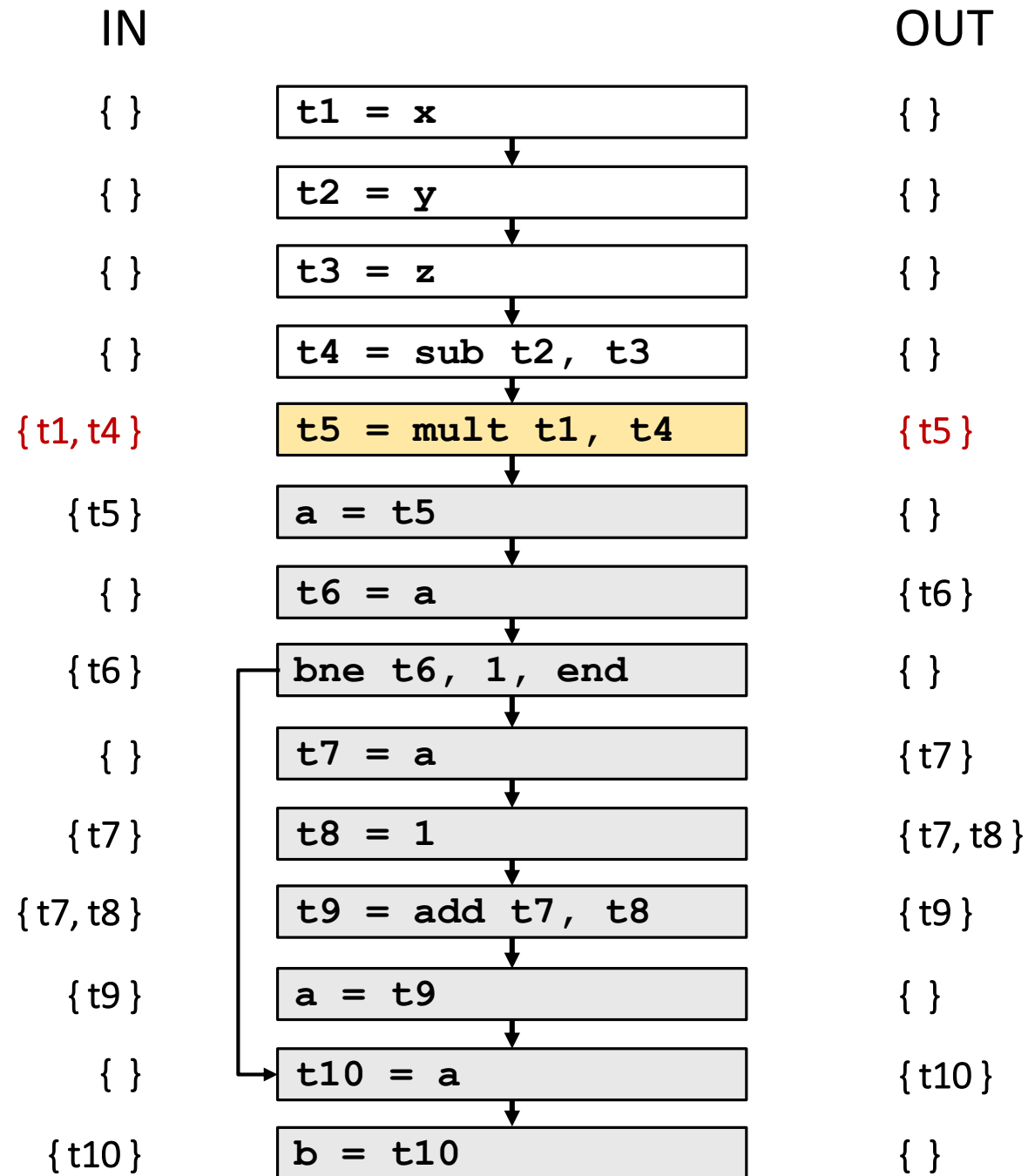


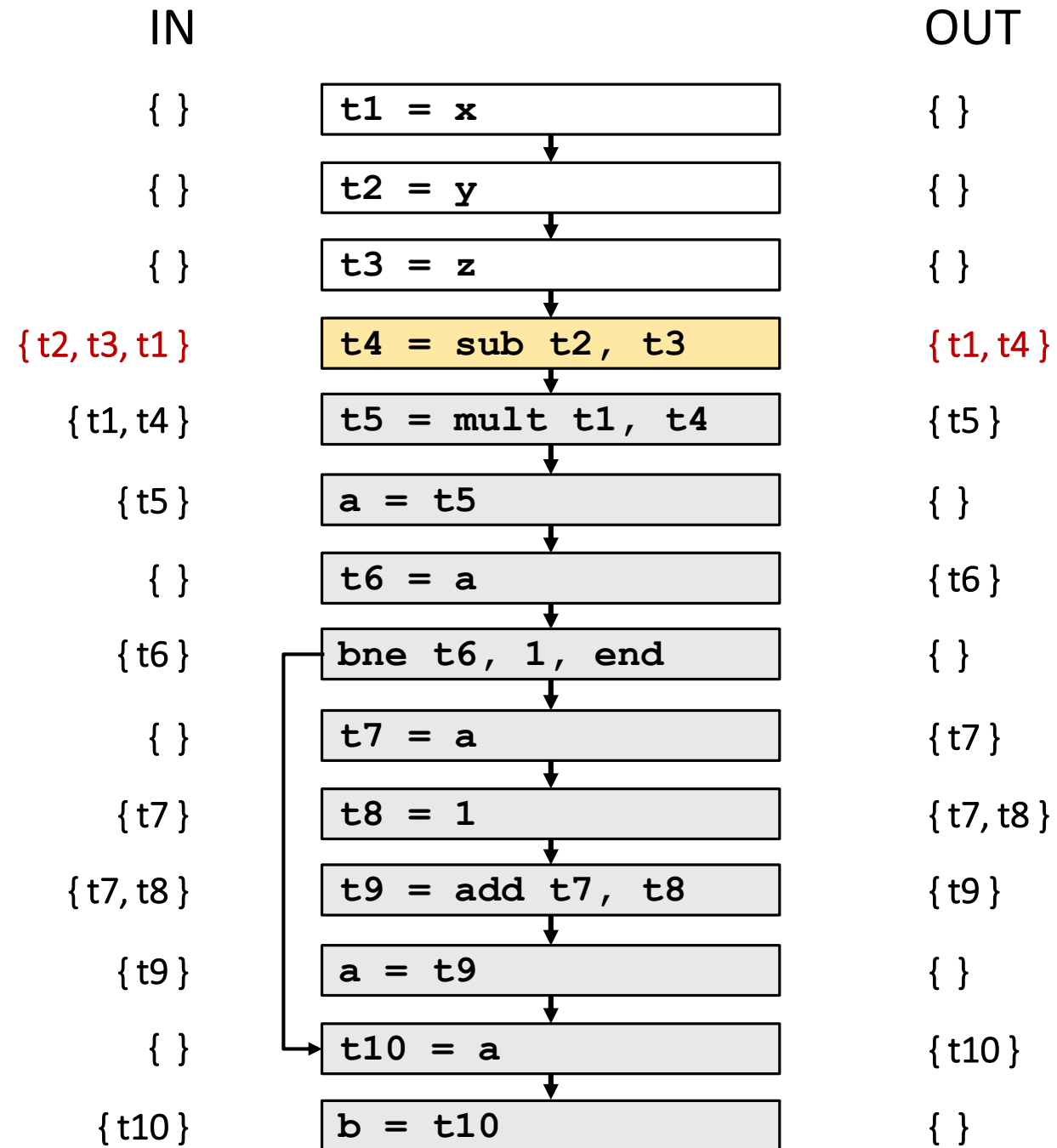


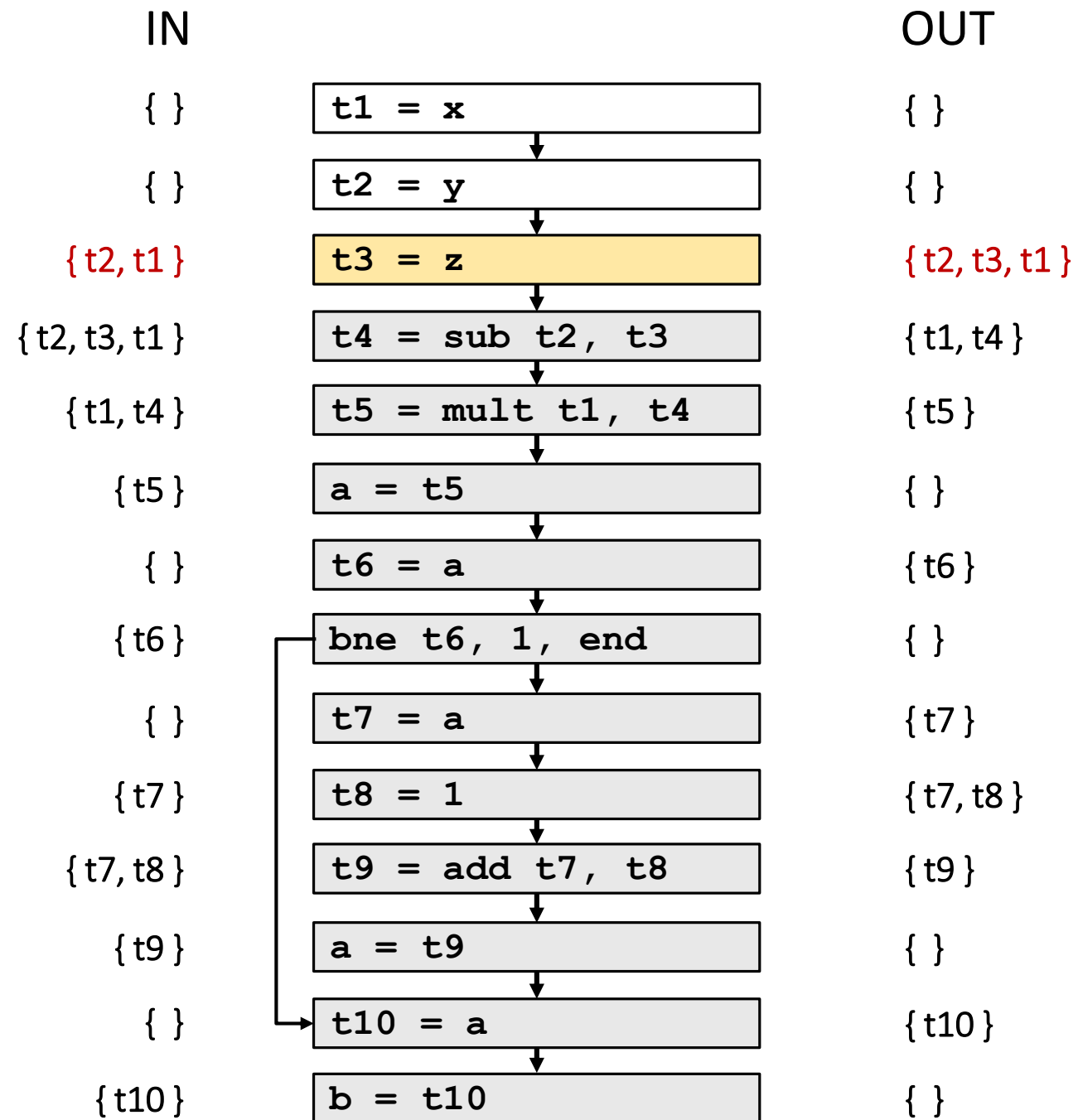


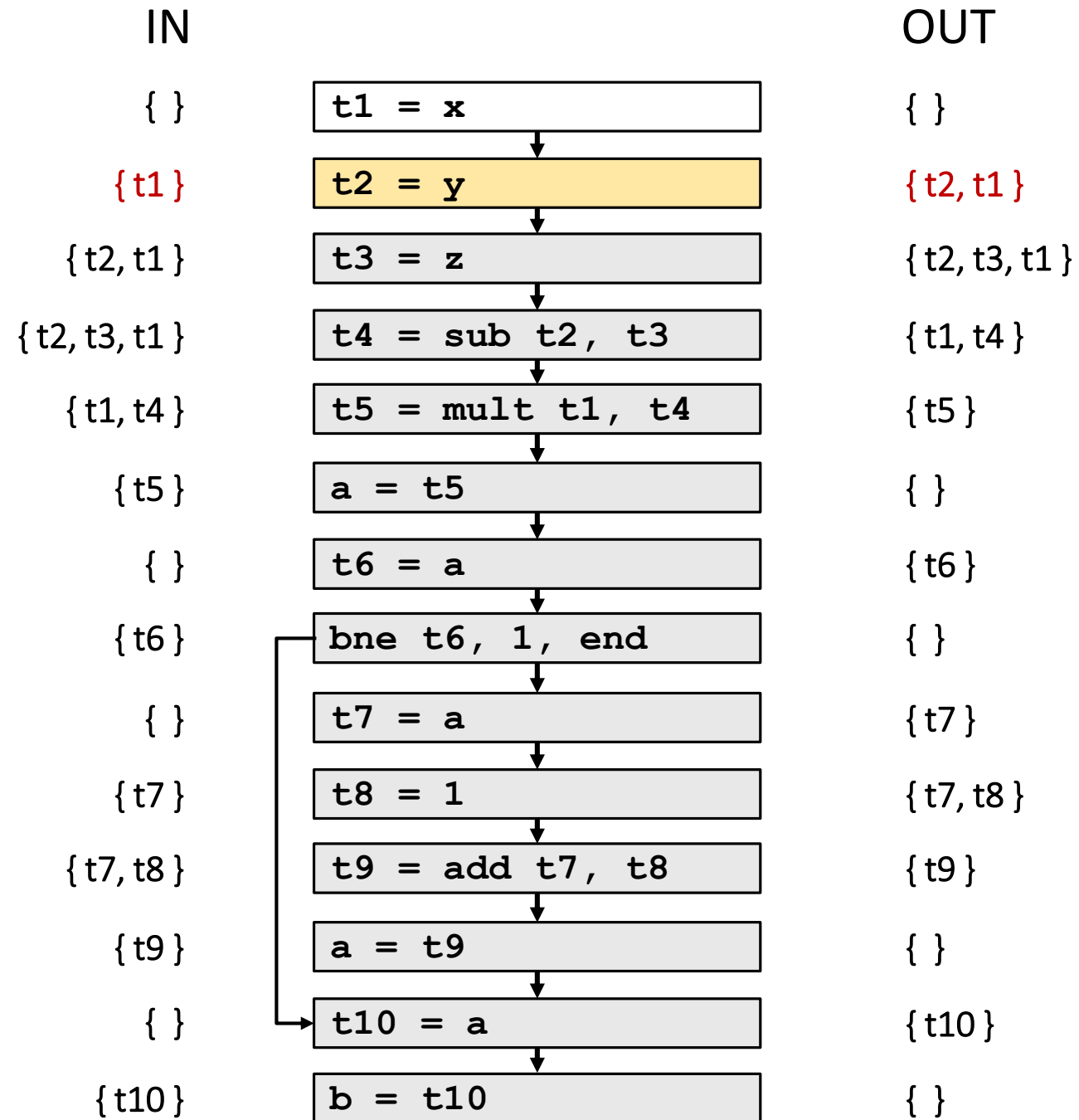






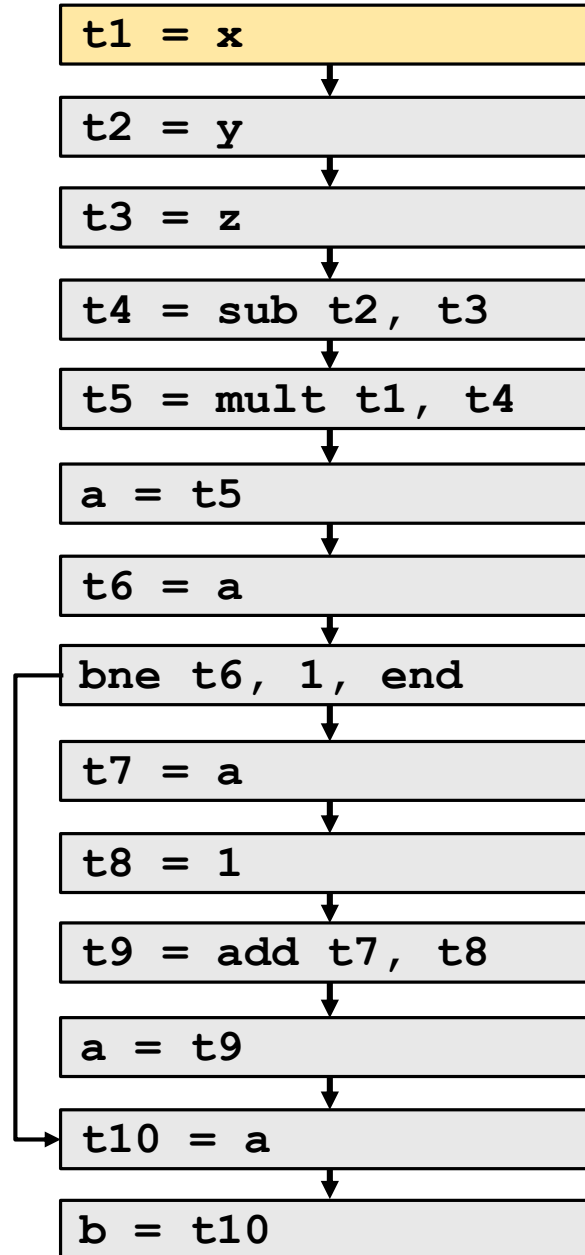






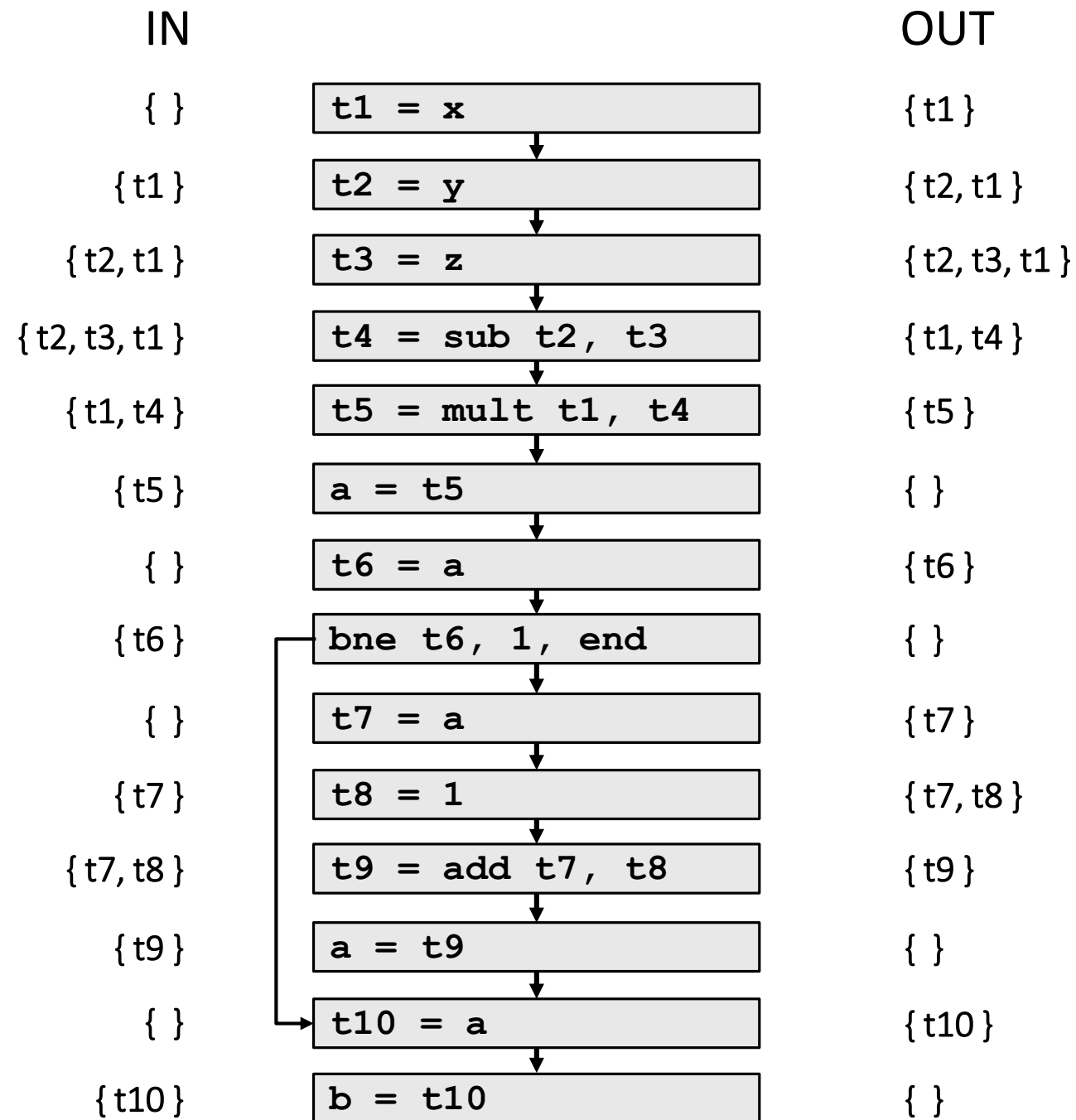
IN

{ }  
{ t1 }  
{ t2, t1 }  
{ t2, t3, t1 }  
{ t1, t4 }  
{ t5 }  
{ }  
{ t6 }  
{ }  
{ t7 }  
{ t7, t8 }  
{ t9 }  
{ }  
{ t10 }



OUT

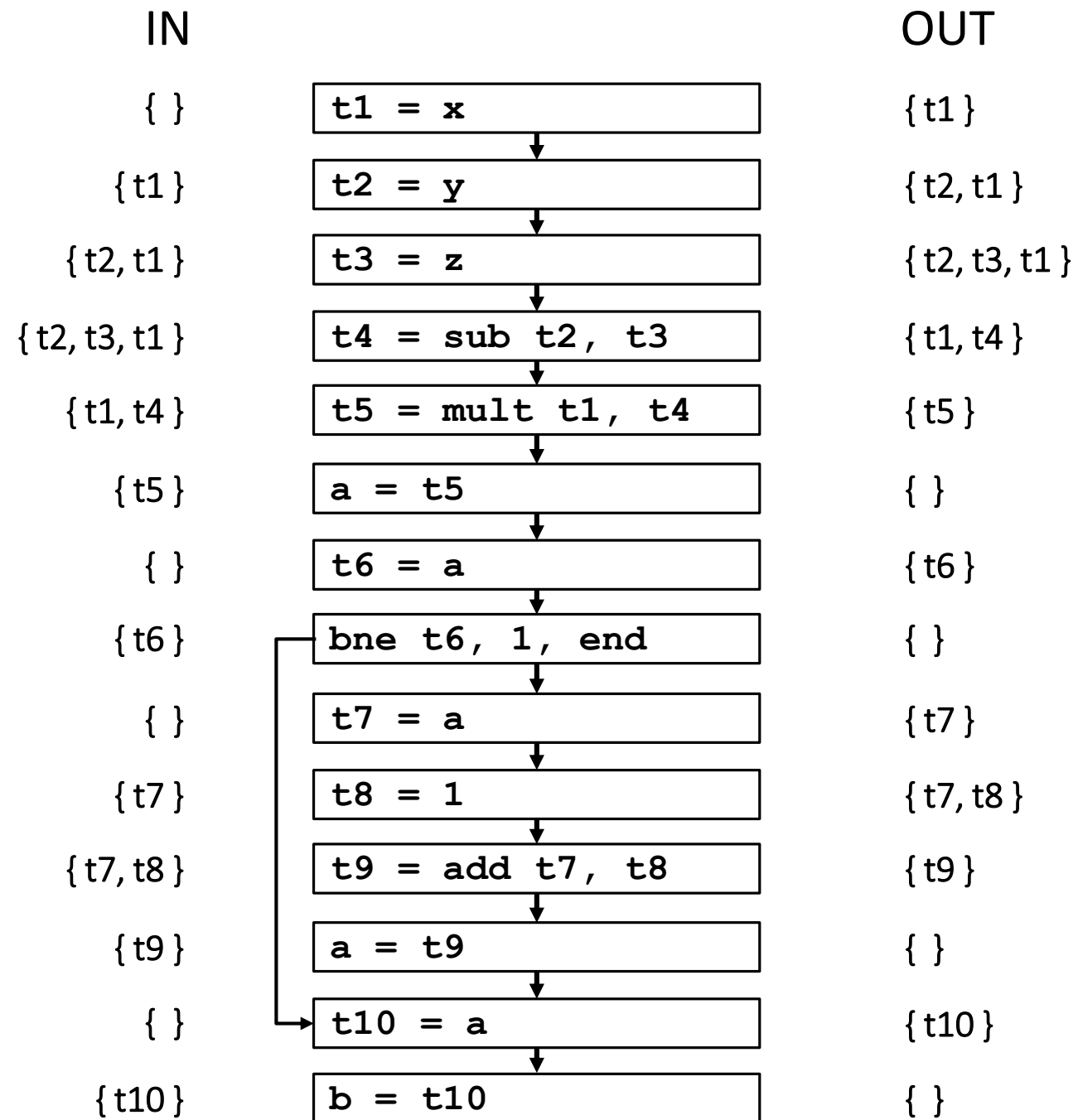
{ t1 }  
{ t2, t1 }  
{ t2, t3, t1 }  
{ t1, t4 }  
{ t5 }  
{ }  
{ t6 }  
{ }  
{ t7 }  
{ t7, t8 }  
{ t9 }  
{ }  
{ t10 }  
{ }

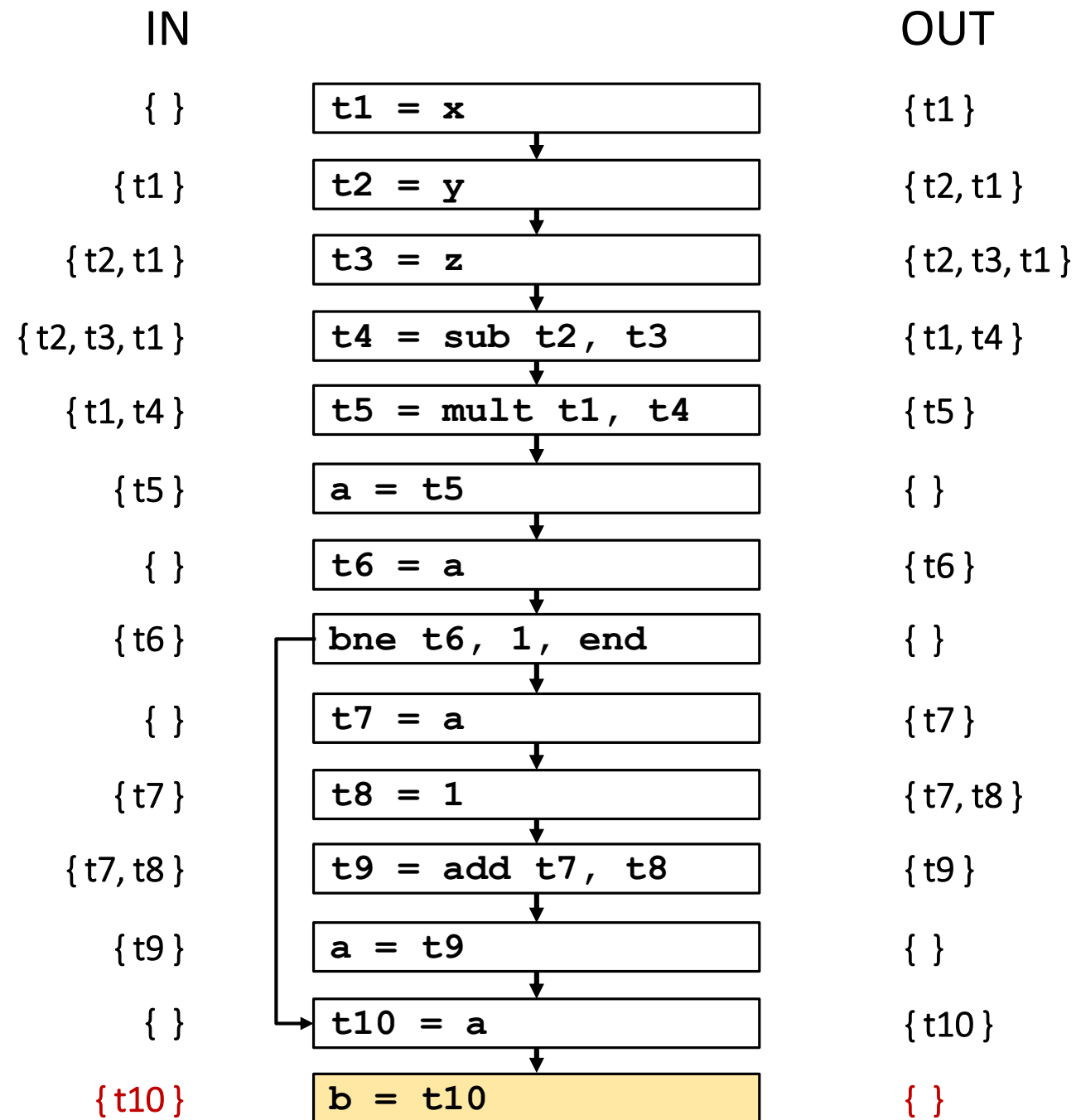


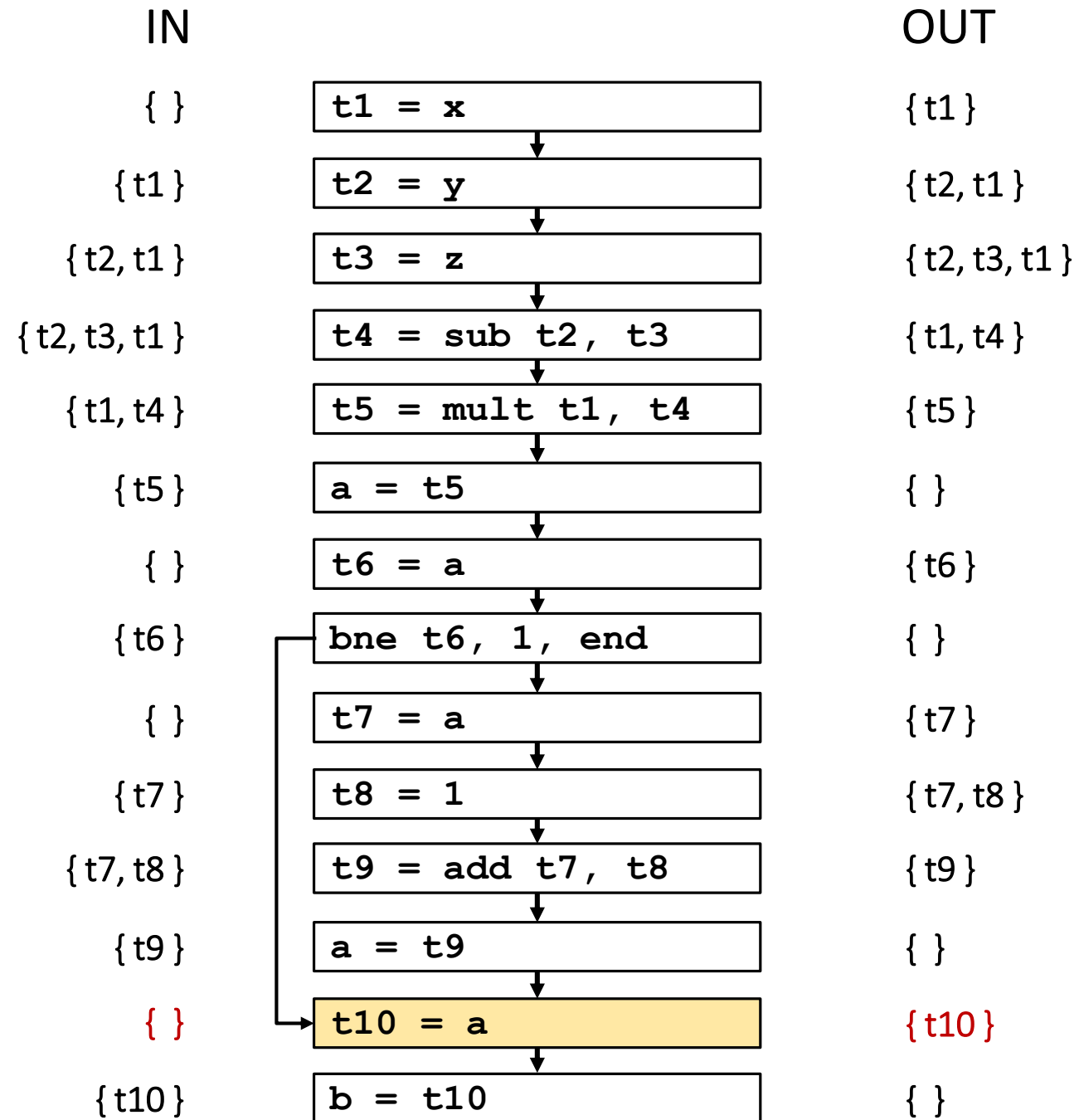
# Liveness Analysis

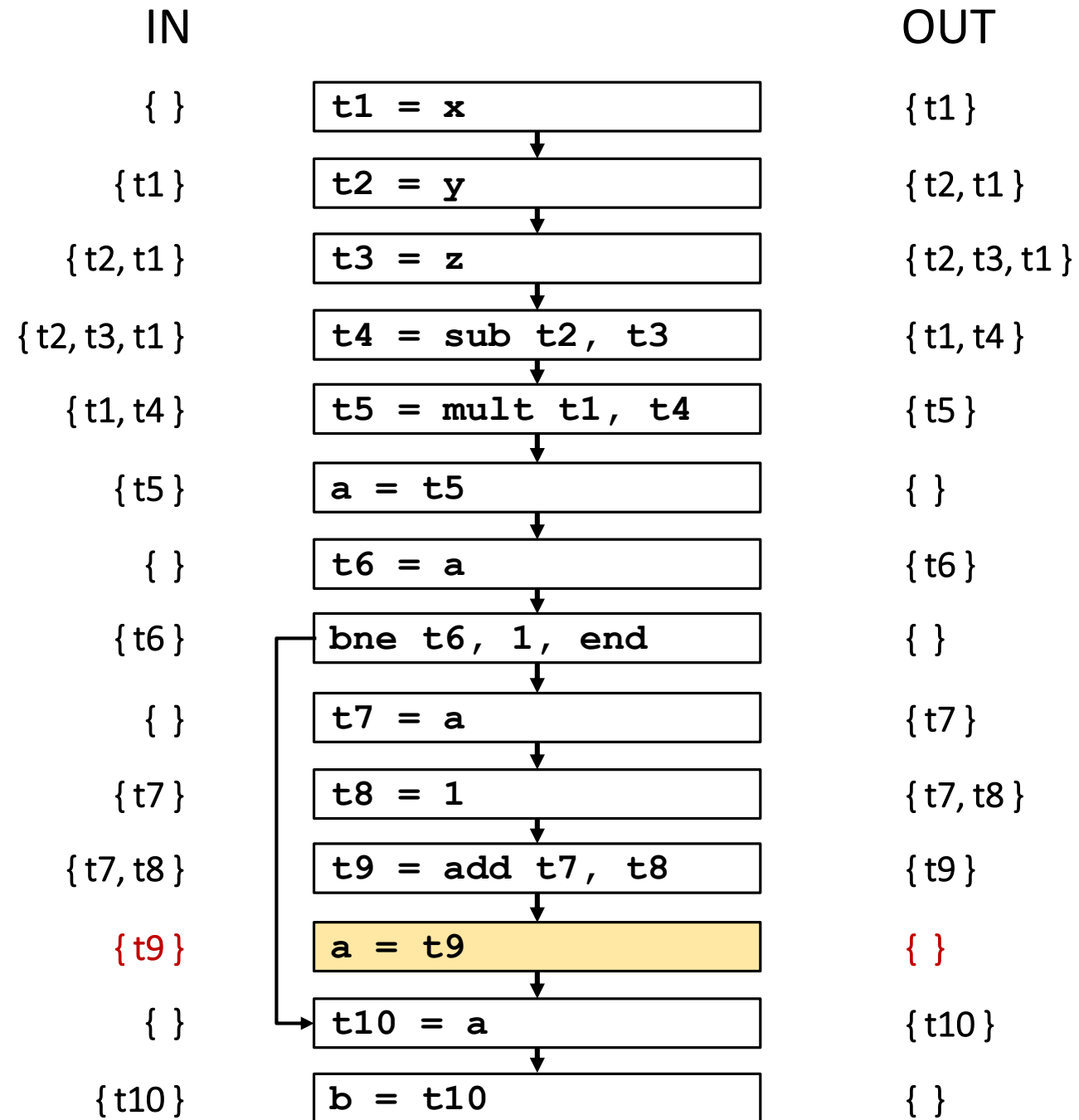
- Second pass

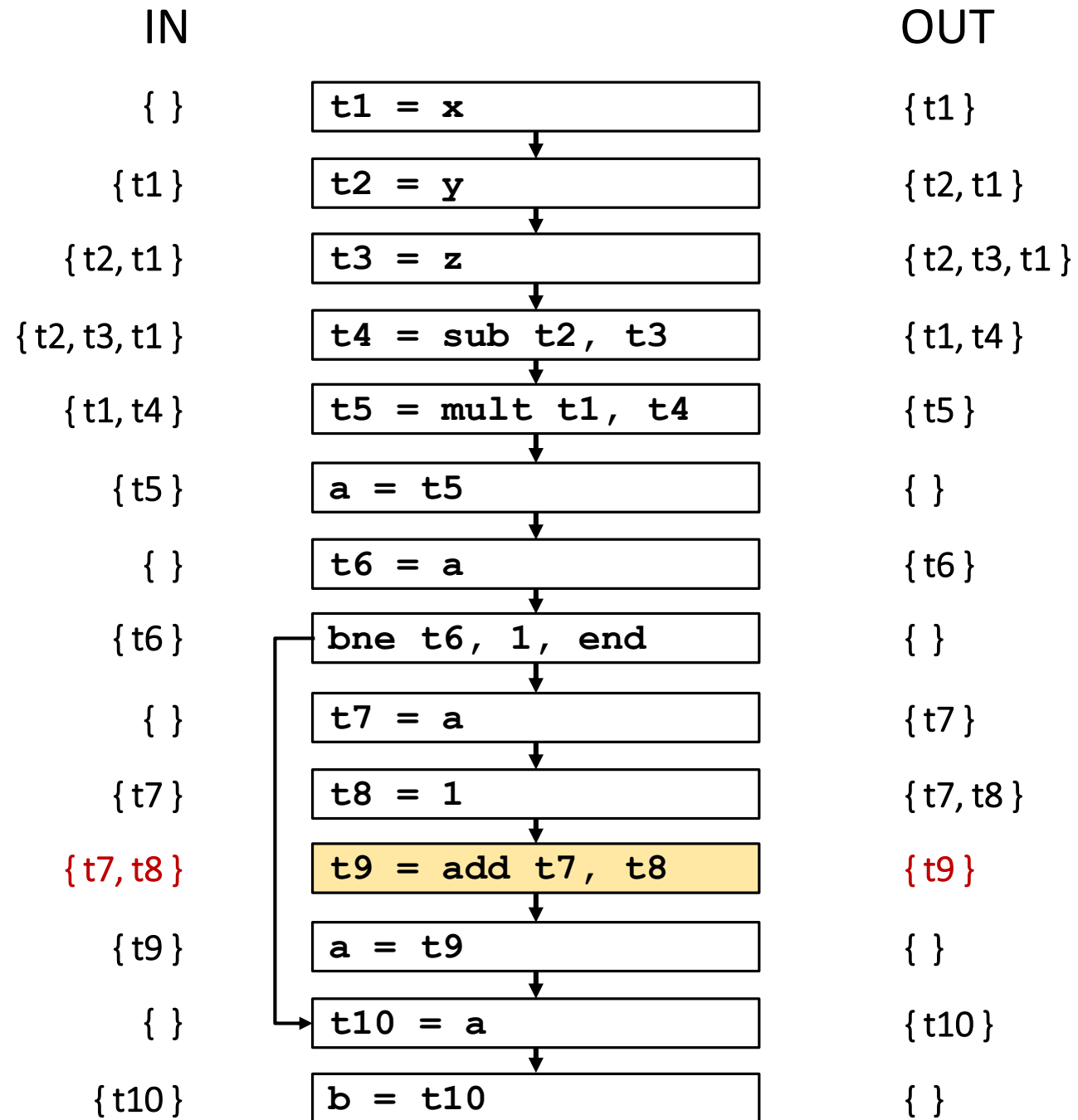


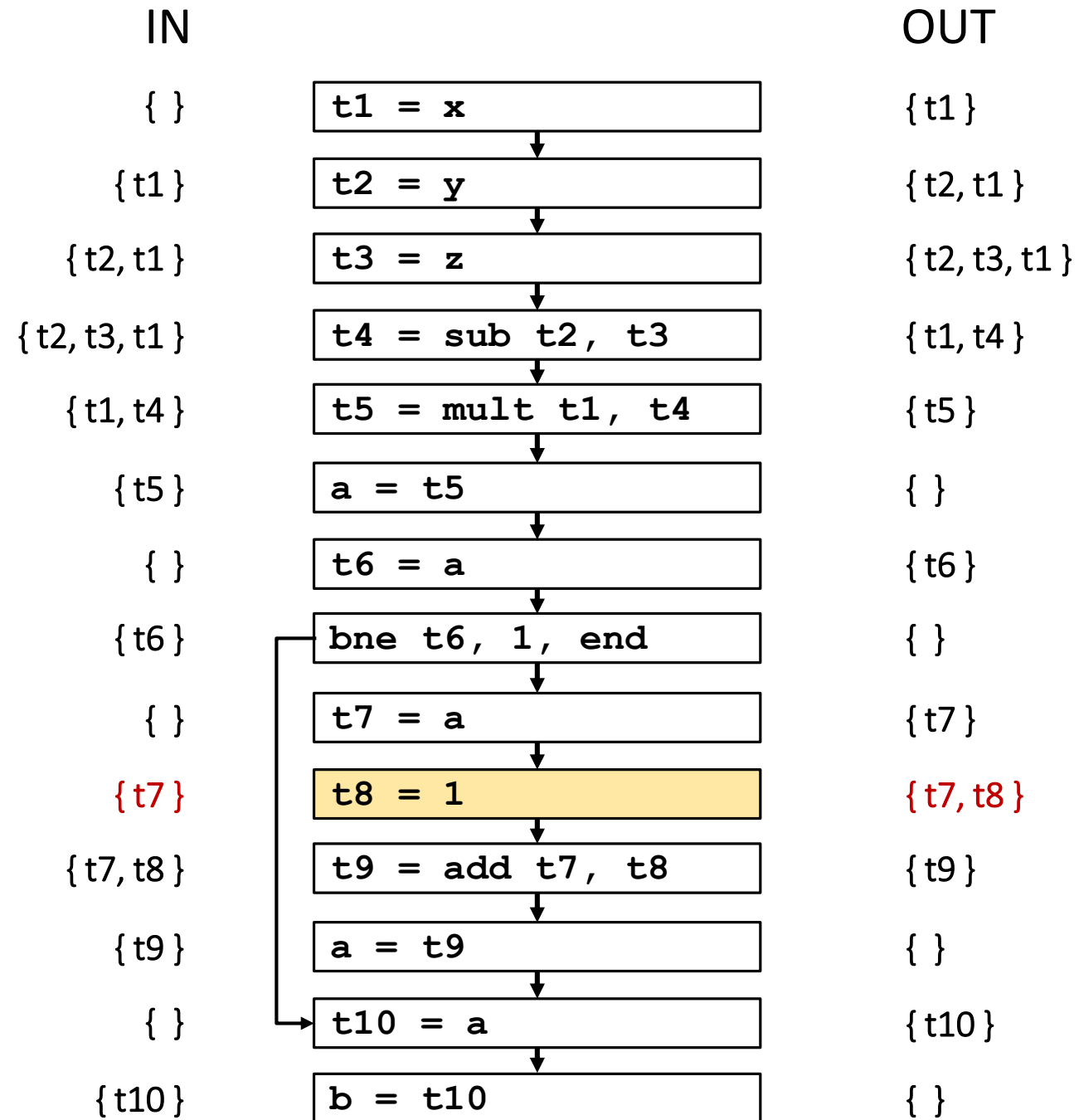


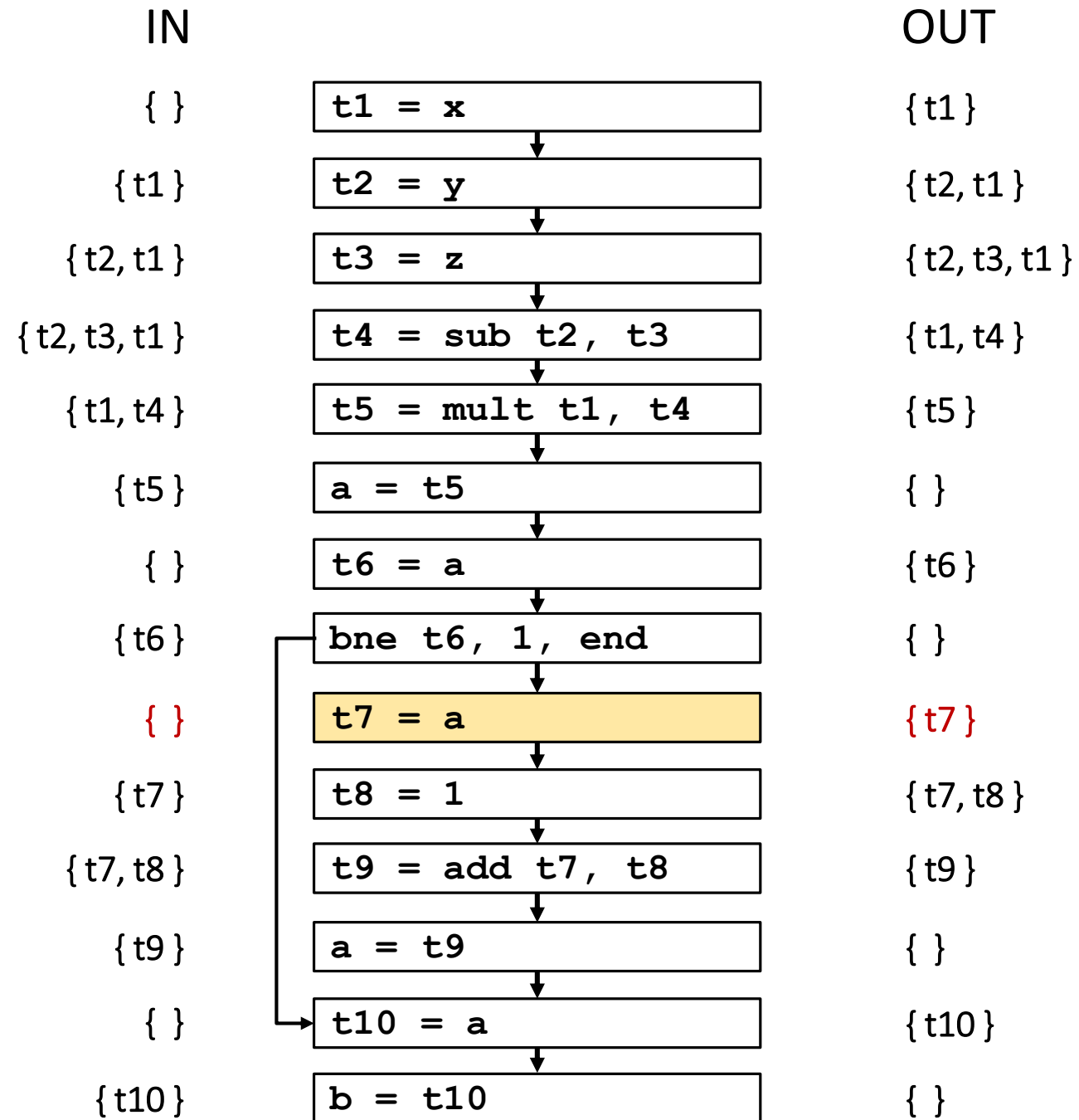


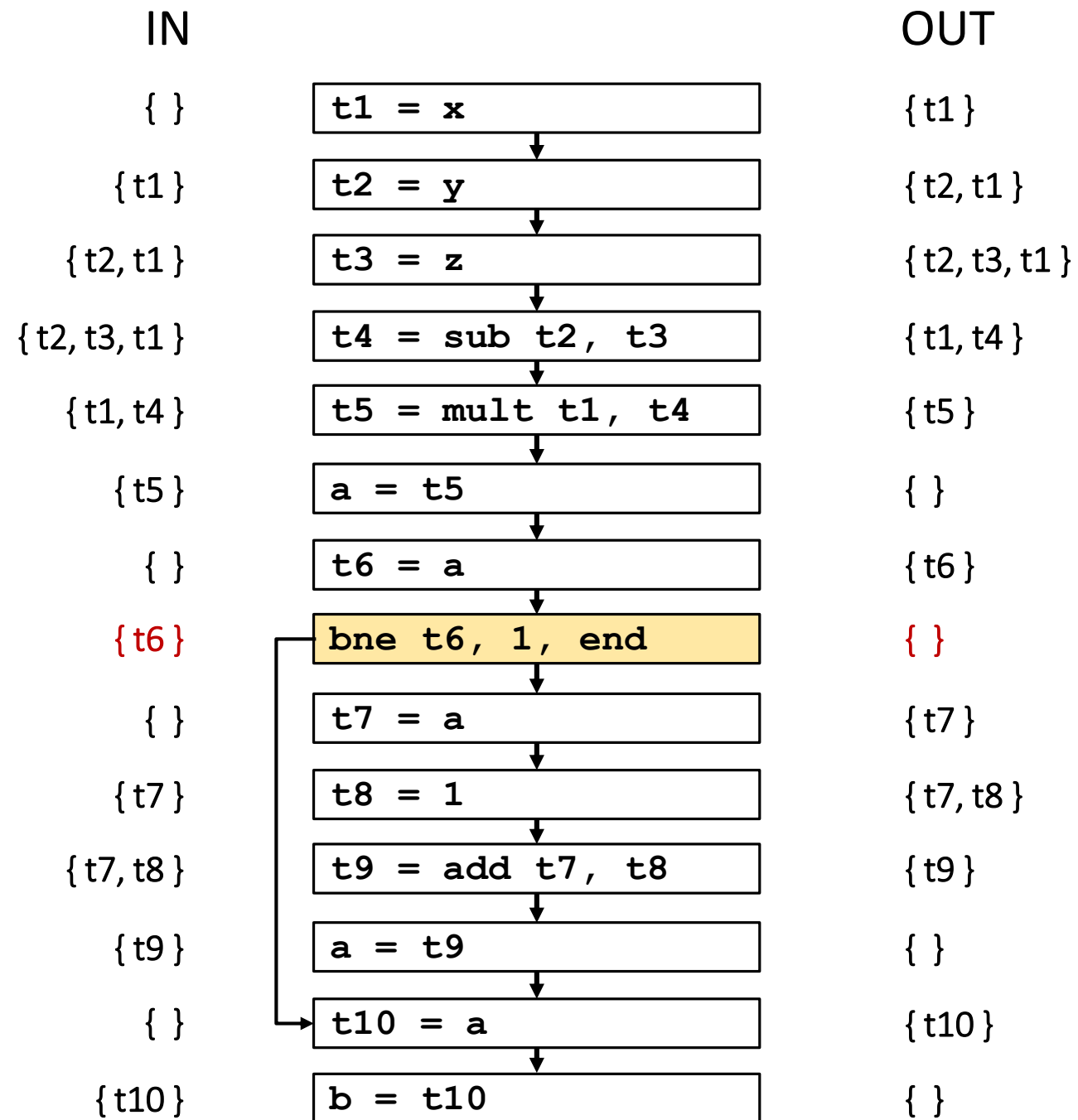




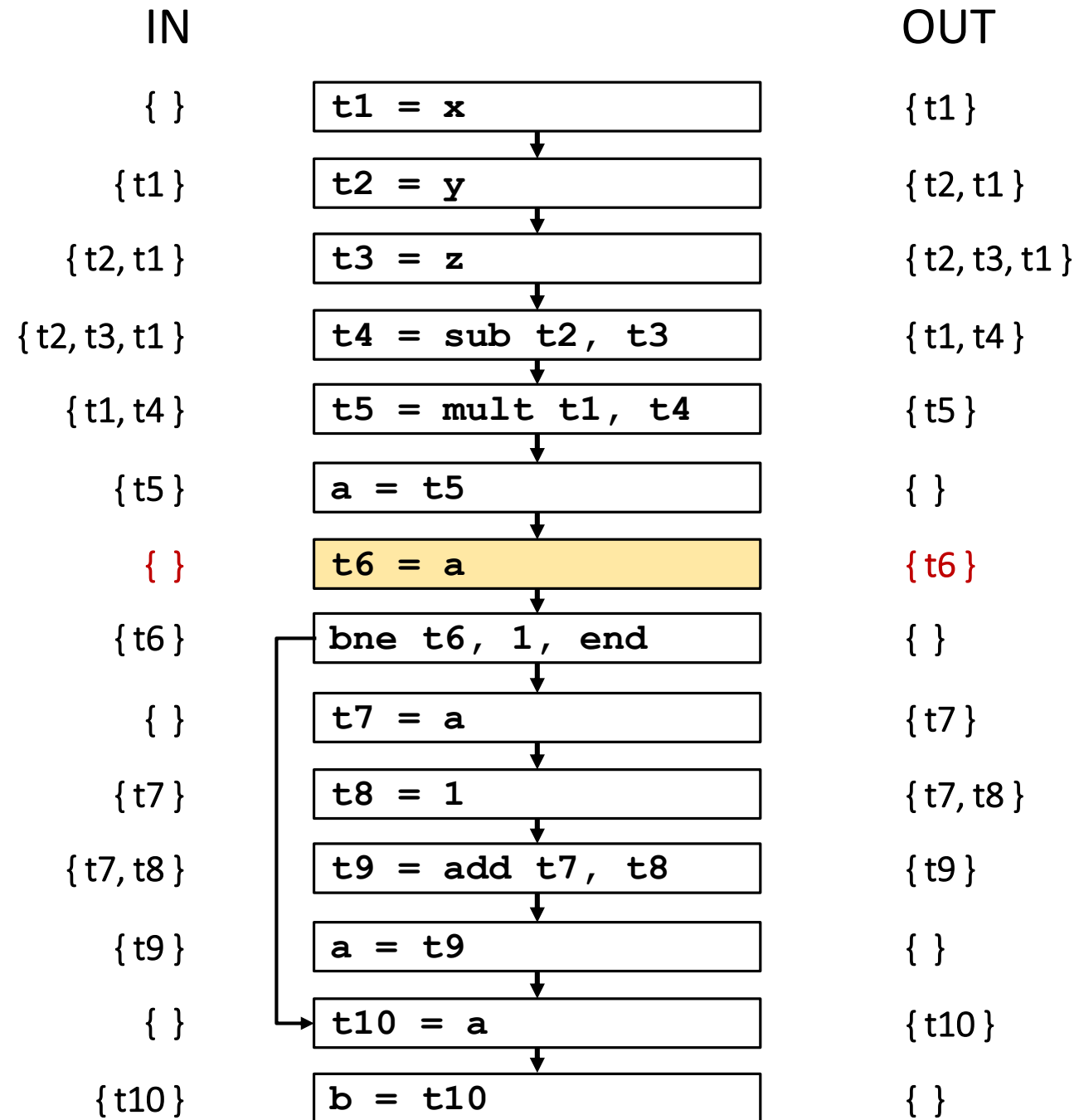


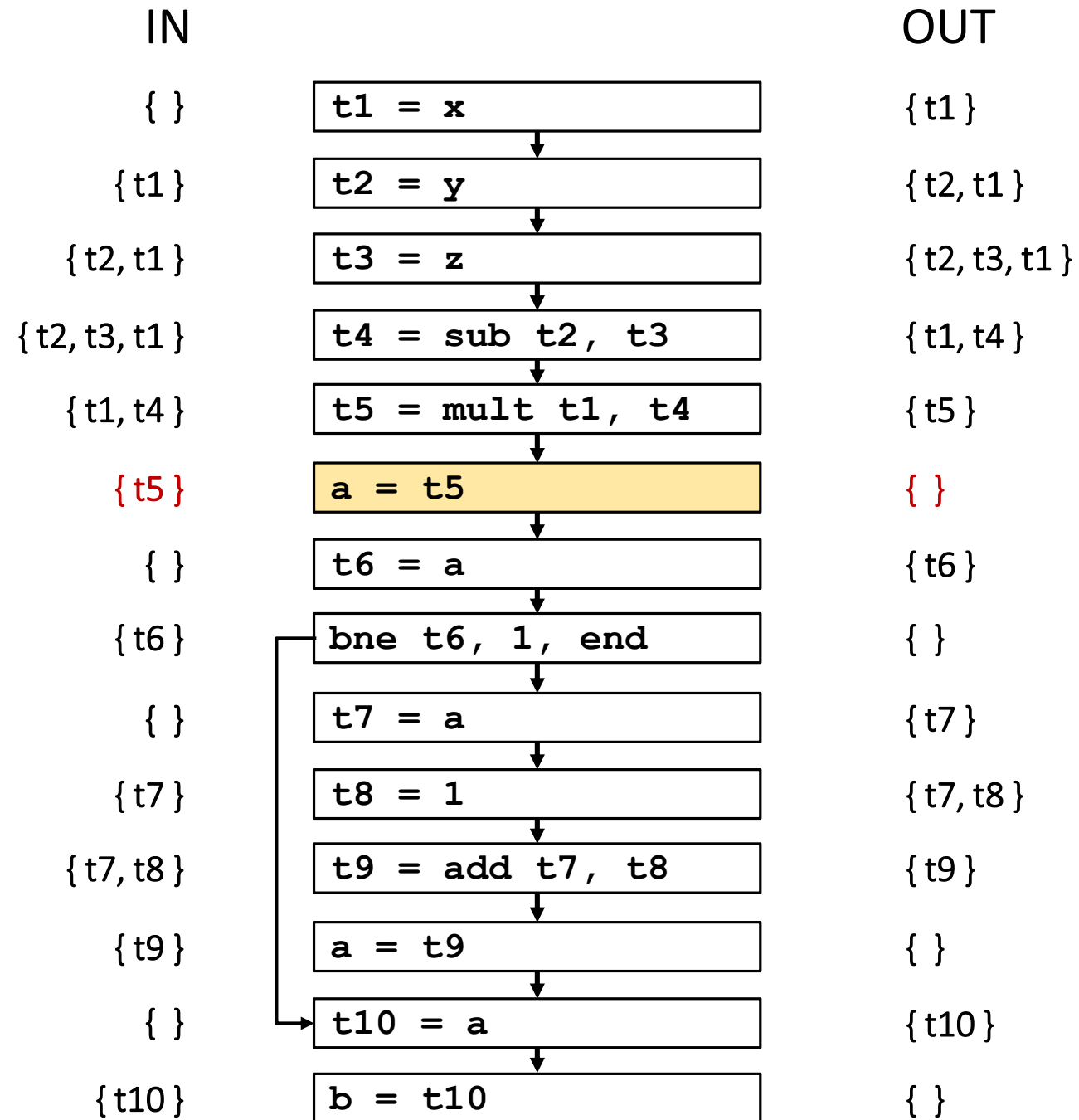


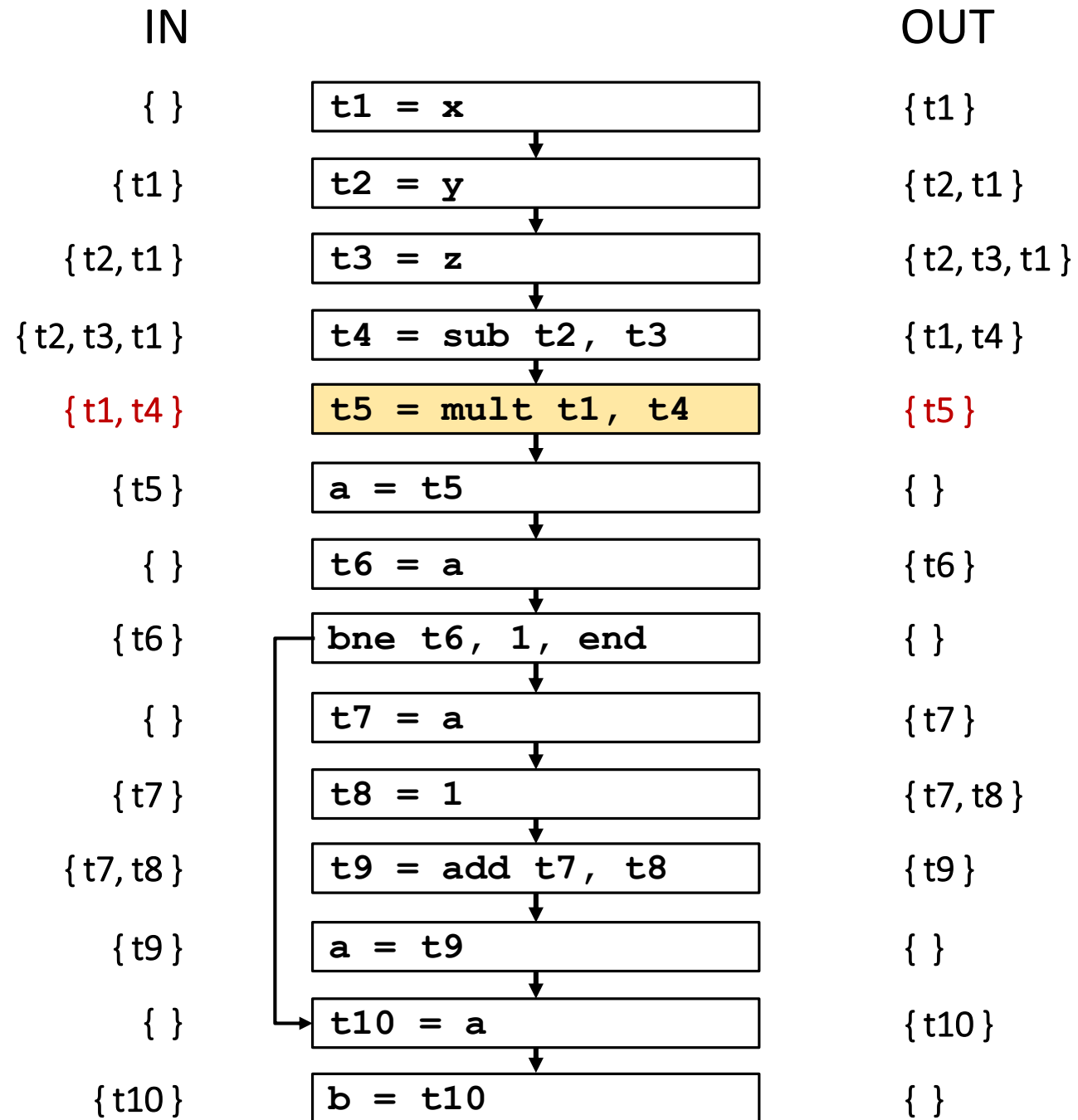


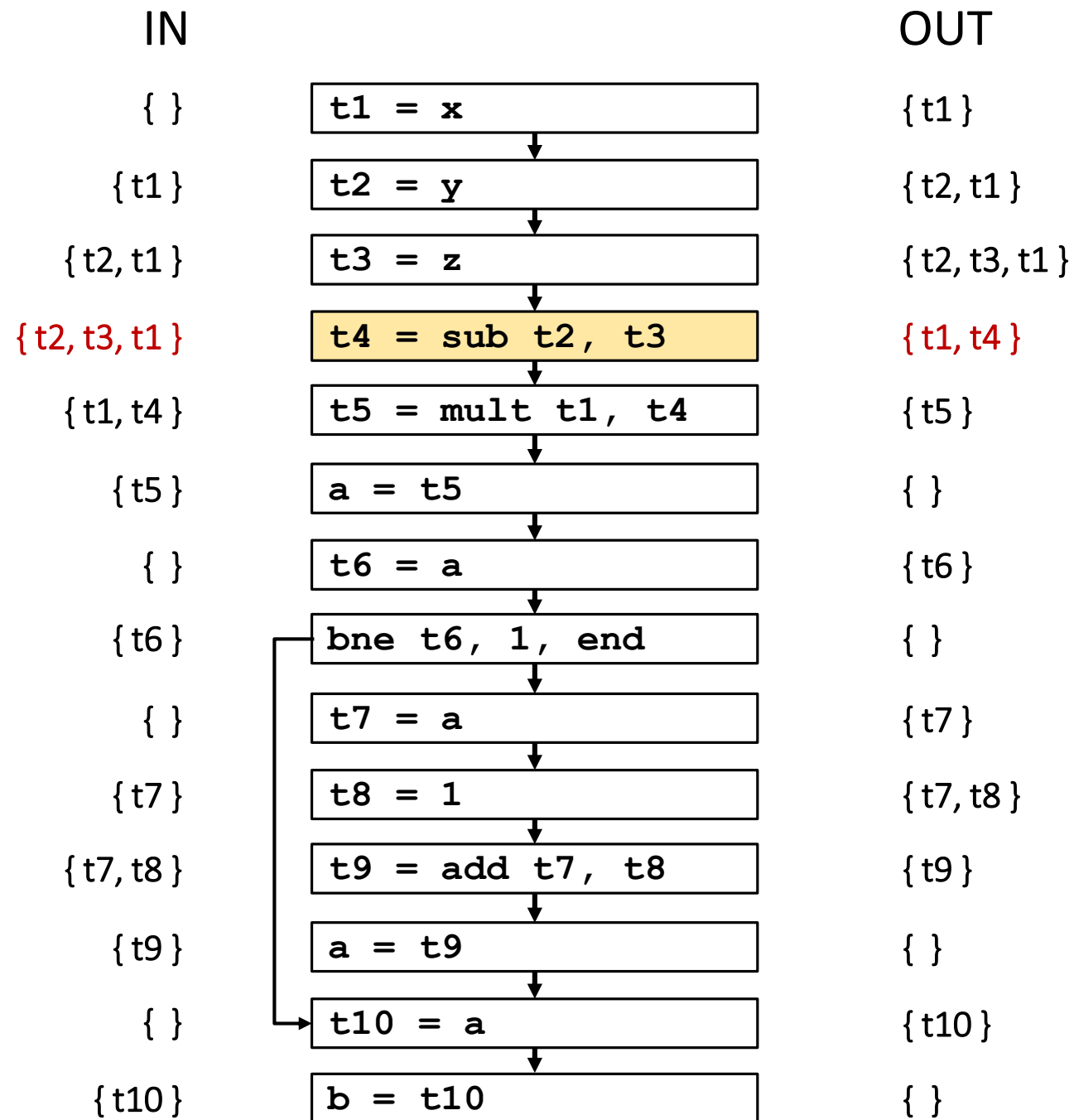


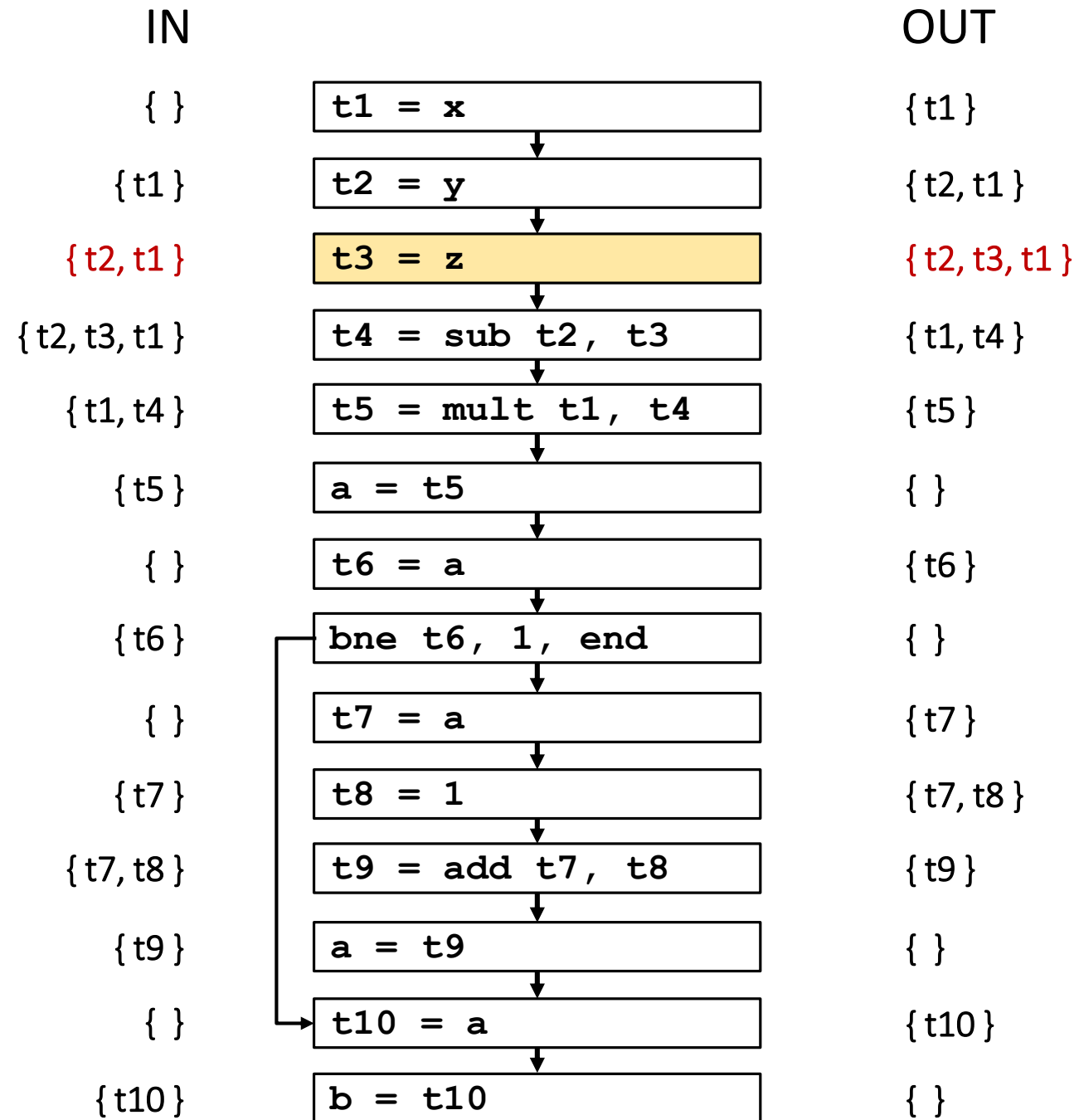


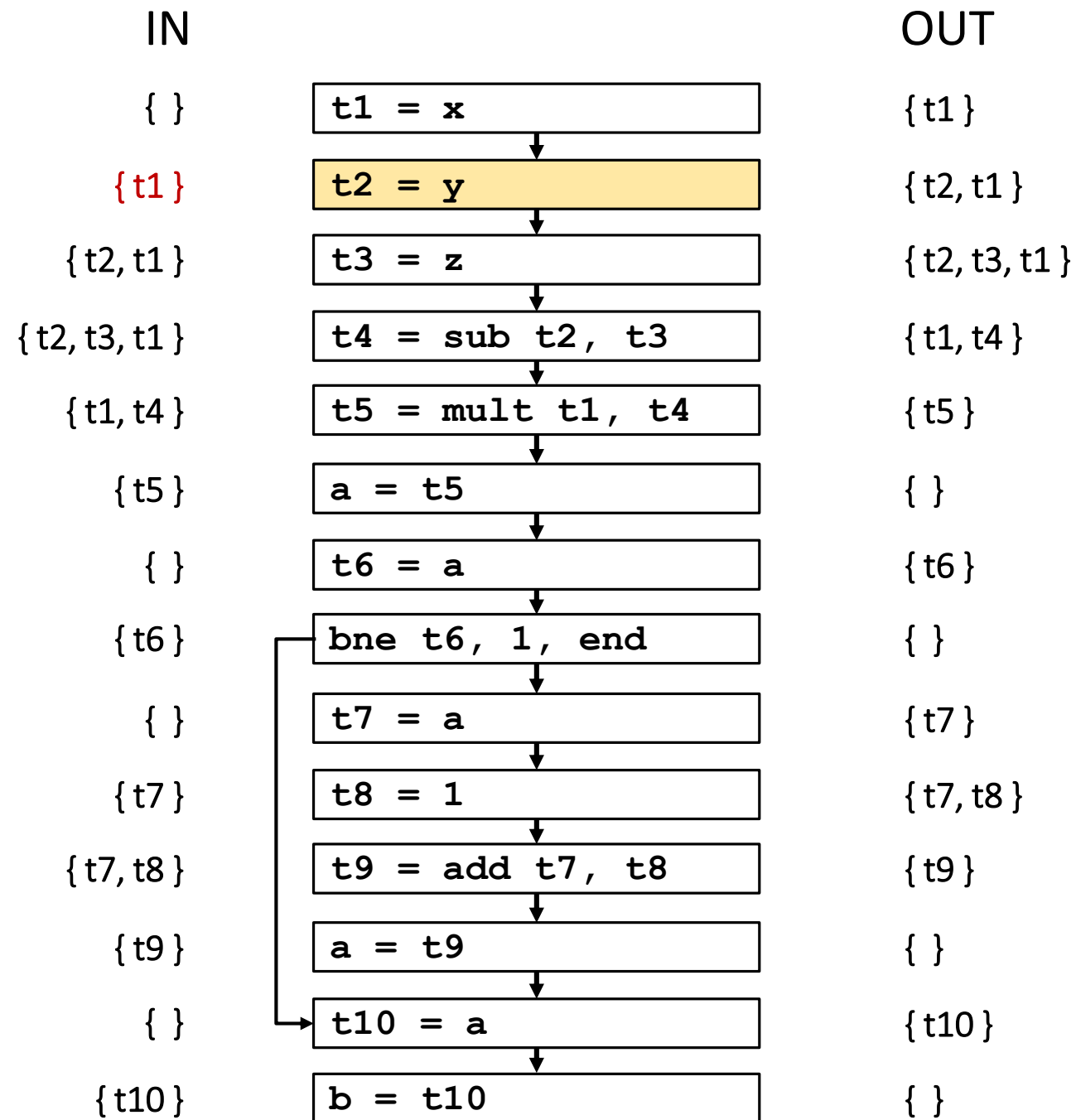






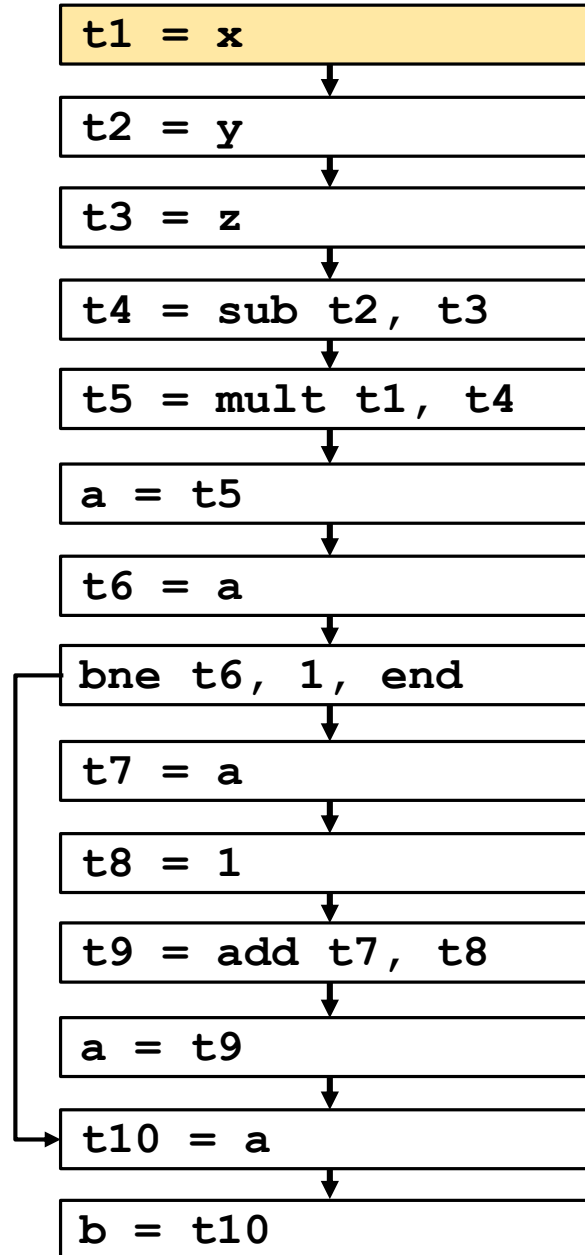






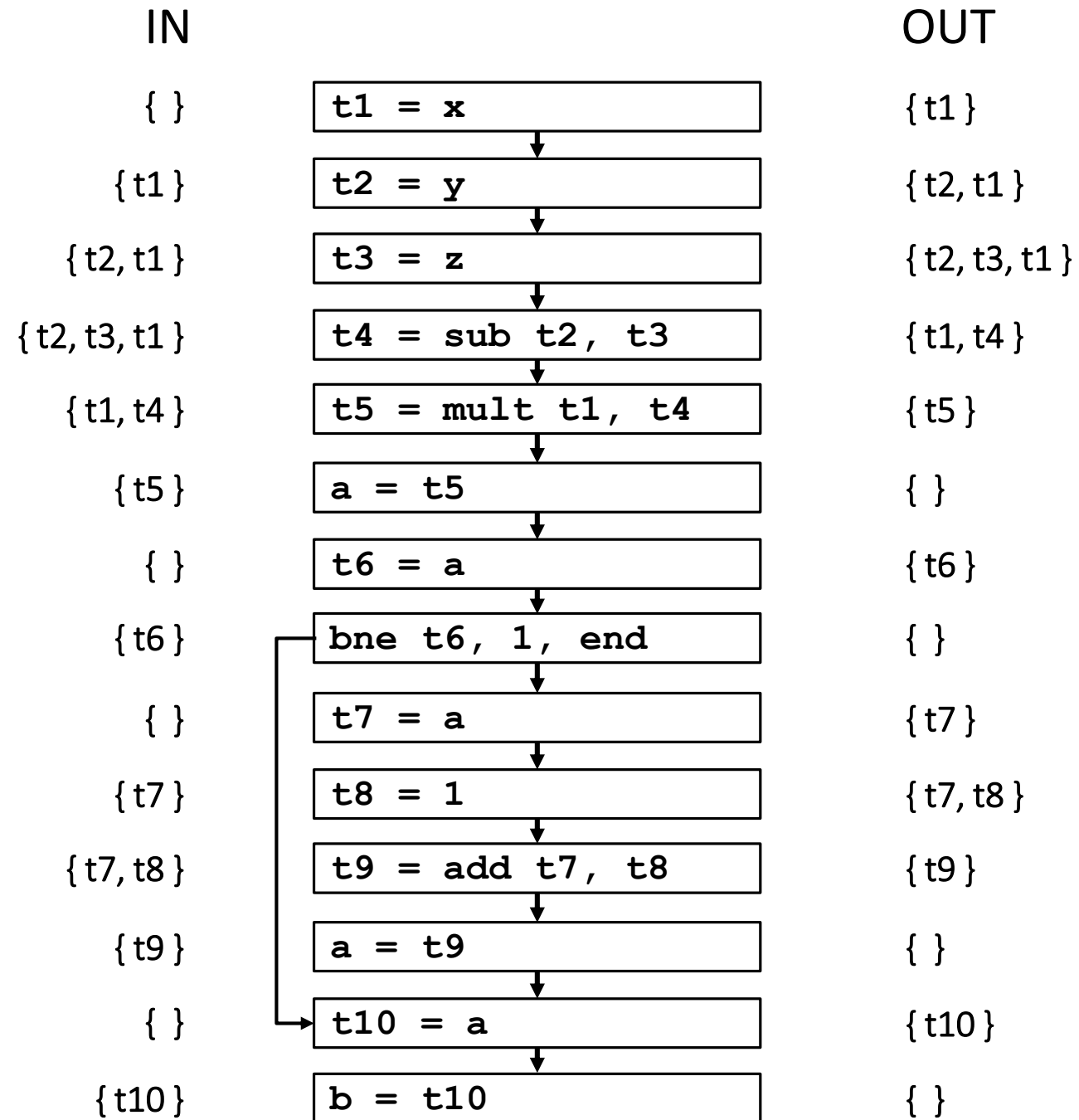
IN

{ }  
{ t1 }  
{ t2, t1 }  
{ t2, t3, t1 }  
{ t1, t4 }  
{ t5 }  
{ }  
{ t6 }  
{ }  
{ t7 }  
{ t7, t8 }  
{ t9 }  
{ }  
{ t10 }



OUT

{ t1 }  
{ t2, t1 }  
{ t2, t3, t1 }  
{ t1, t4 }  
{ t5 }  
{ }  
{ t6 }  
{ }  
{ t7 }  
{ t7, t8 }  
{ t9 }  
{ }  
{ t10 }  
{ }





# Graph Coloring

- TODO