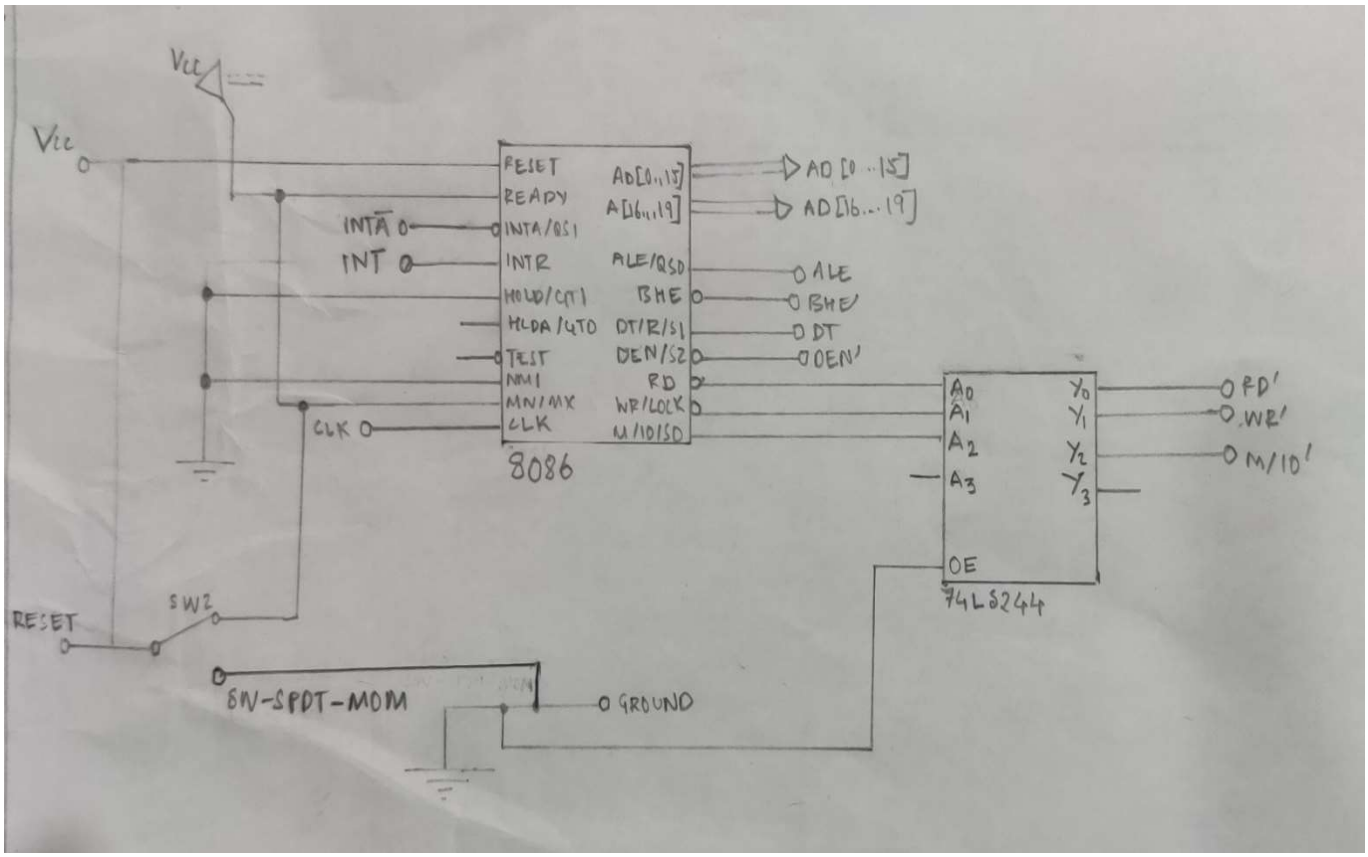
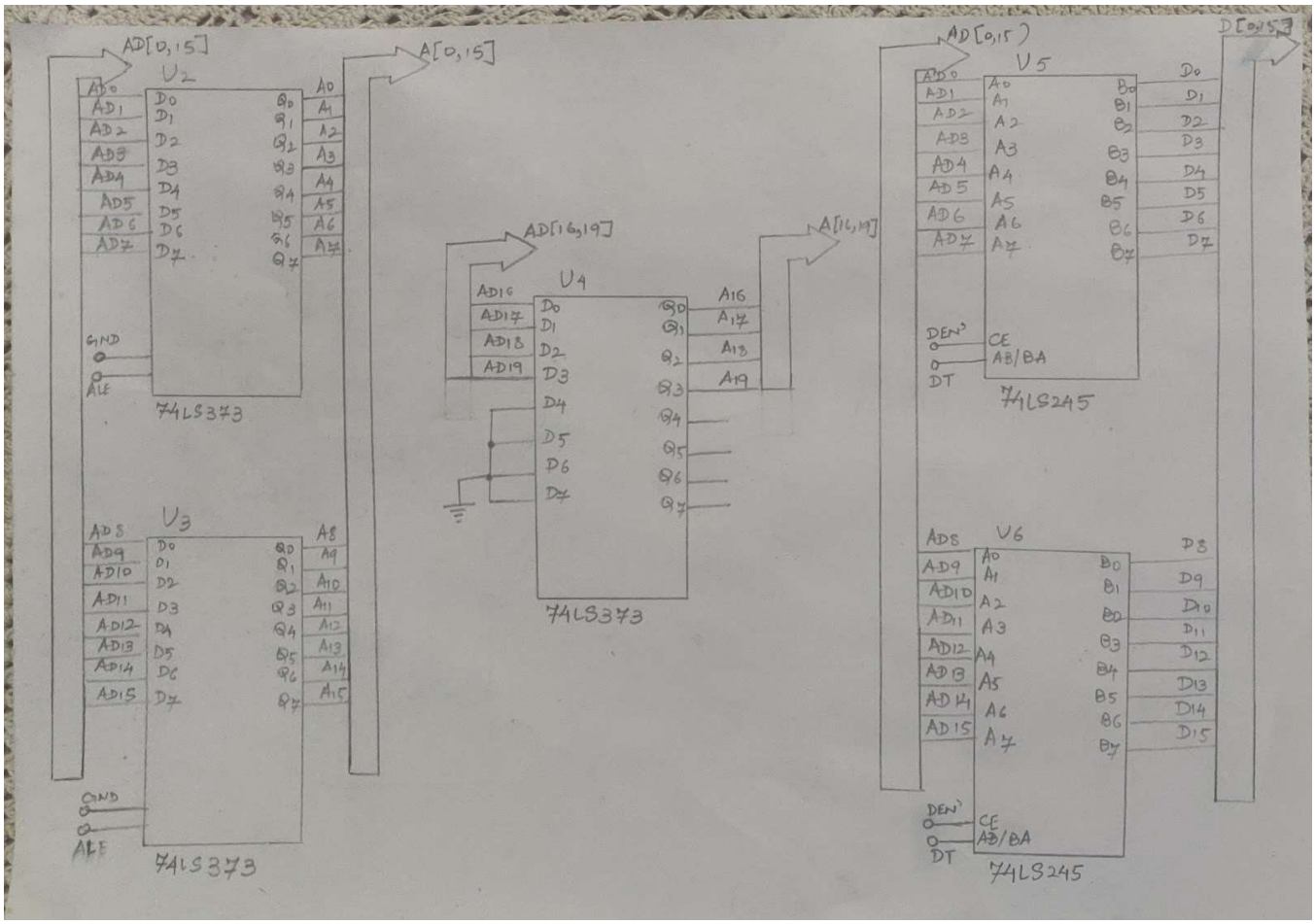
Design

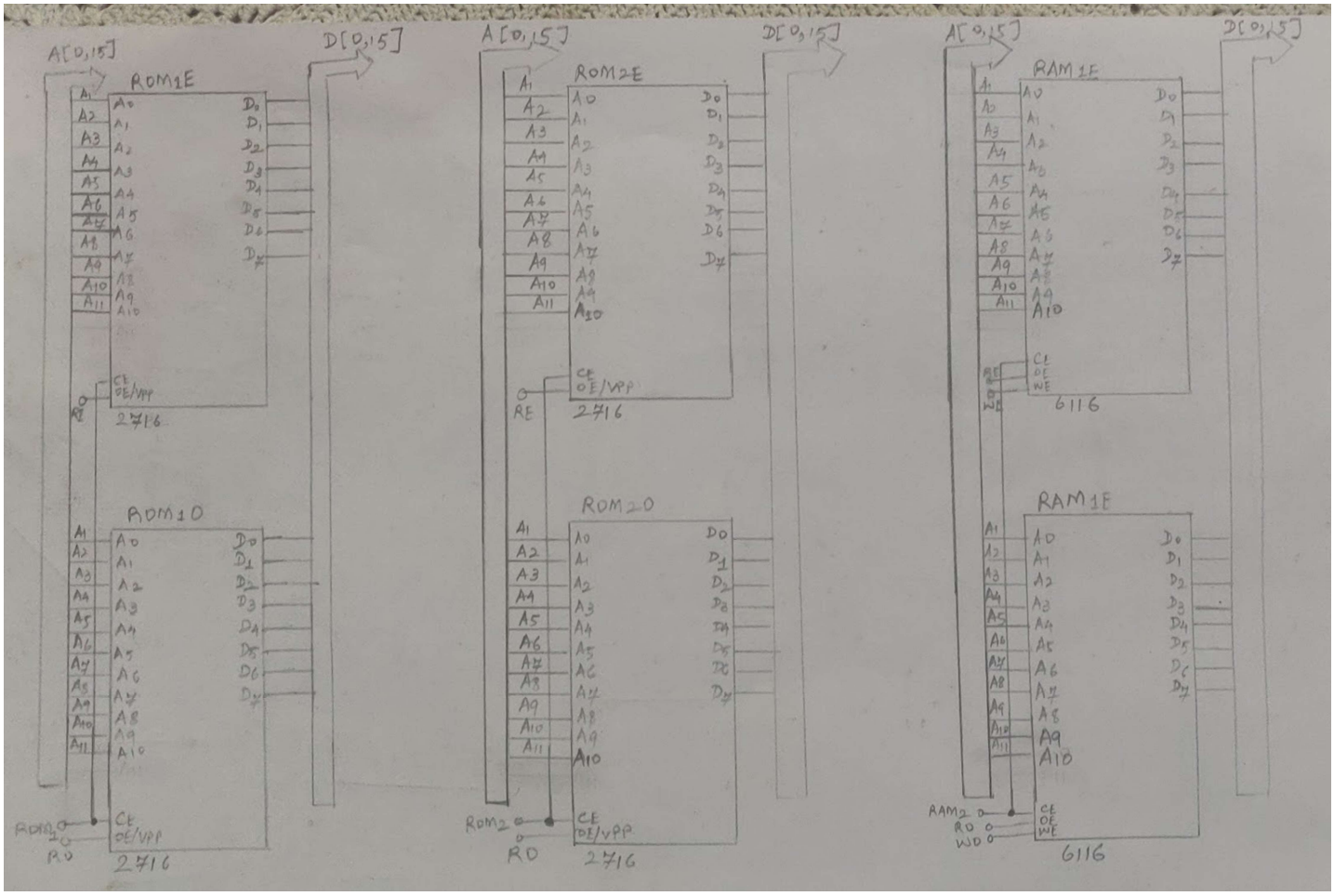
8086

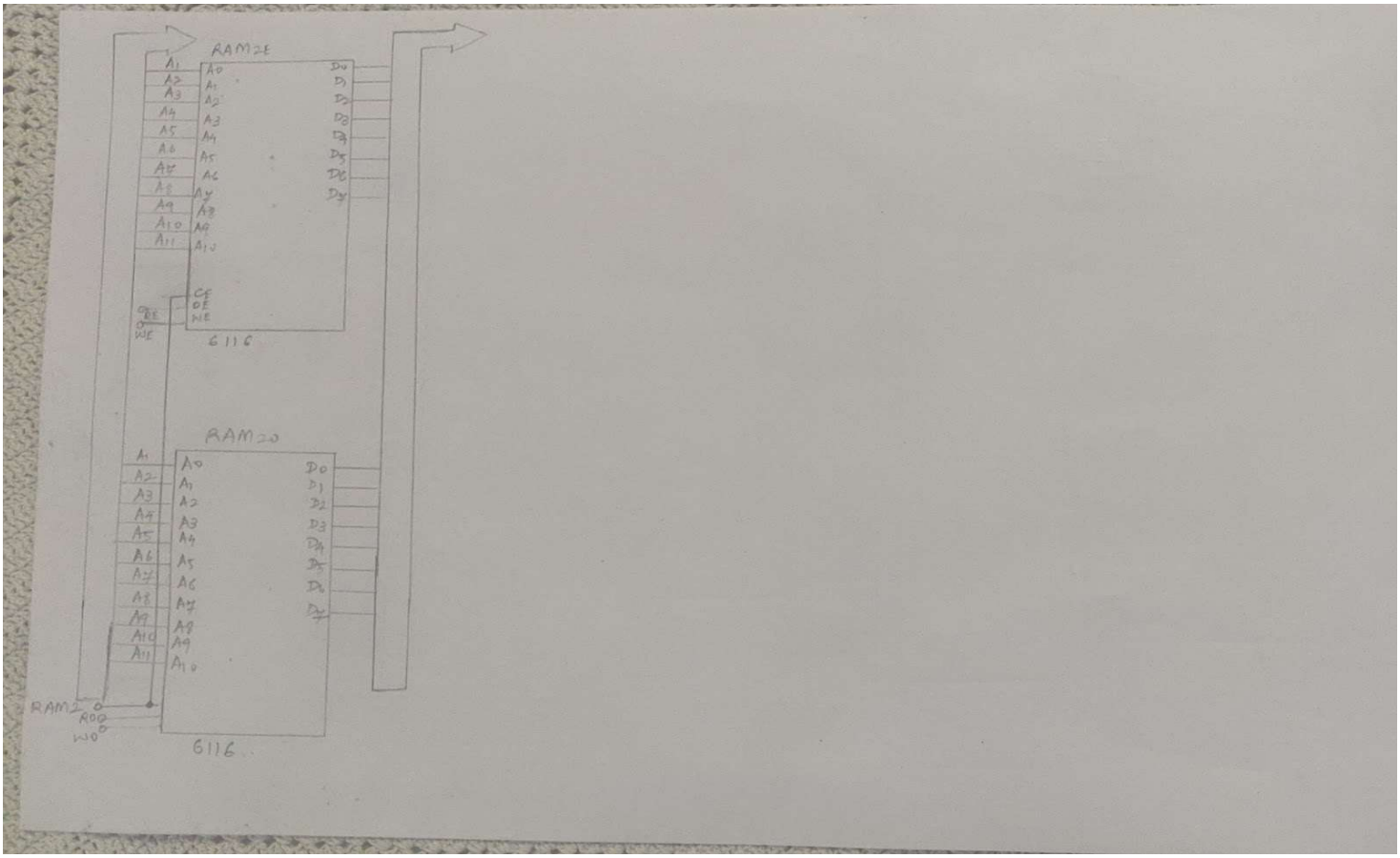

Vcc
Vcc
RESET
READY
INTA/QS1
INTR
HOLD/QT1
HLDA/QT0
TEST
NMI
MN/MX
CLK
AD[0..15]
A[16..19]
ALE/QS0
BHE
DT/R/S1
DEN/S2
RD
WR/LOCK
M/IO/S0
INTA
INT
CLK
8086
AD [0 .. 15]
AD [16 .. 19]
ALE
BHE
DT
DEN
RD
WR
M/IO
A0
A1
A2
A3
OE
Y0
Y1
Y2
Y3
74LS244
RESET
SW2
SW-SPDT-MOM
GROUND

LATCHES AND BUFFERS

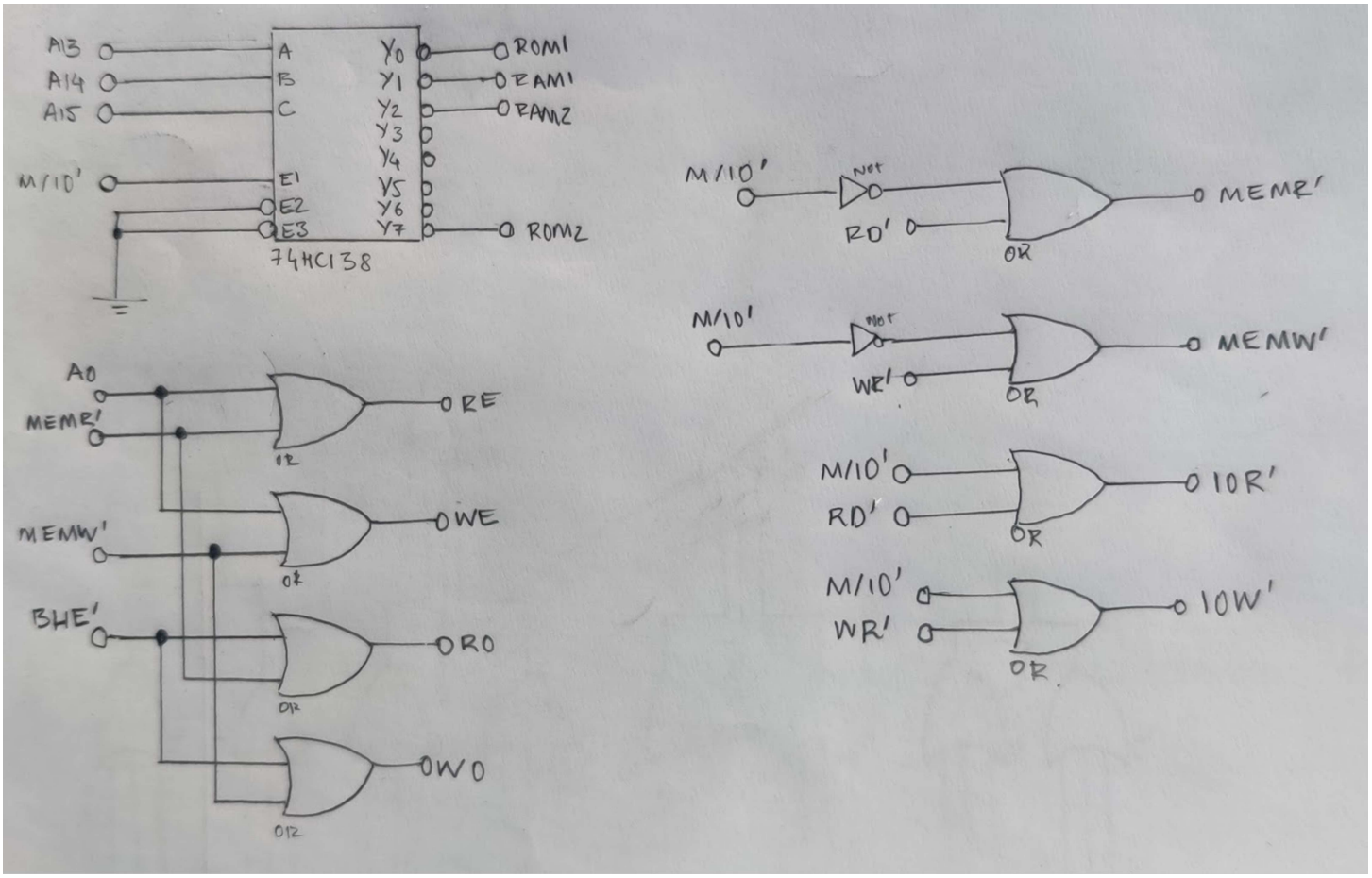


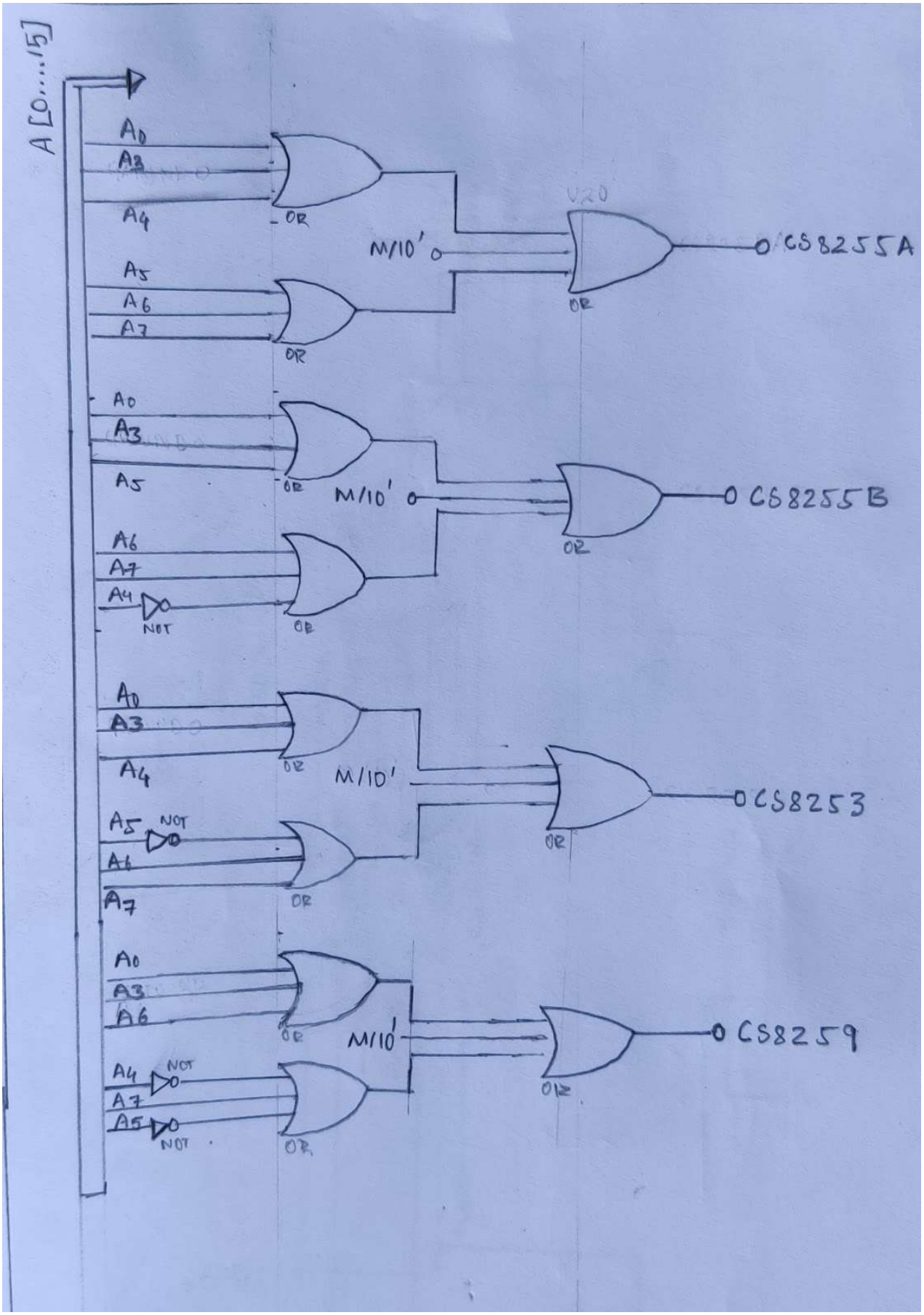
MEMORY INTERFACING



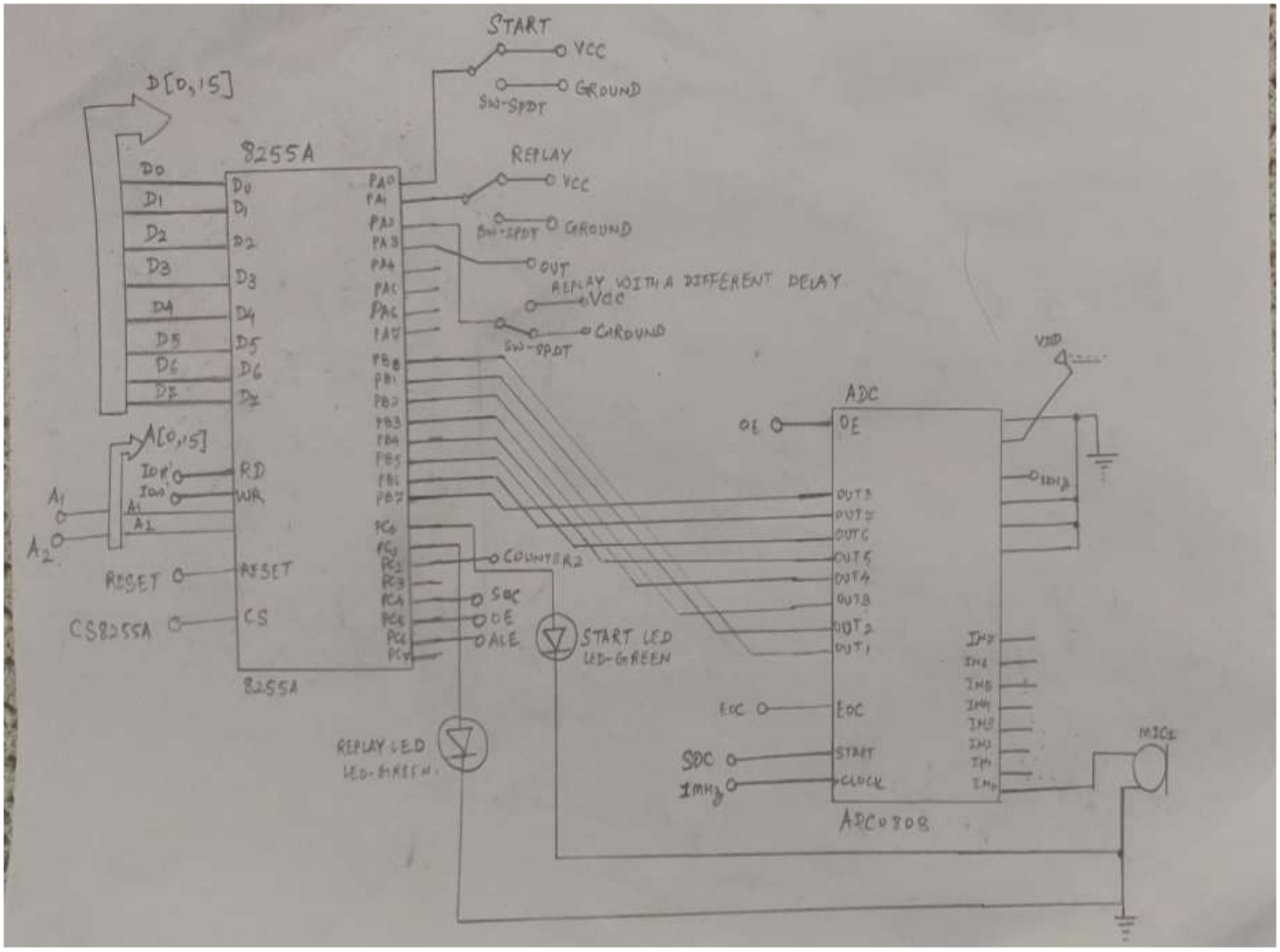

RAM2E
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
D0
D1
D2
D3
D4
D5
D6
D7
CE
OE
WE
6116
RAM2O
RAM2
RDO
WO
6116

DECODING LOGIC FOR CHIP SELECT

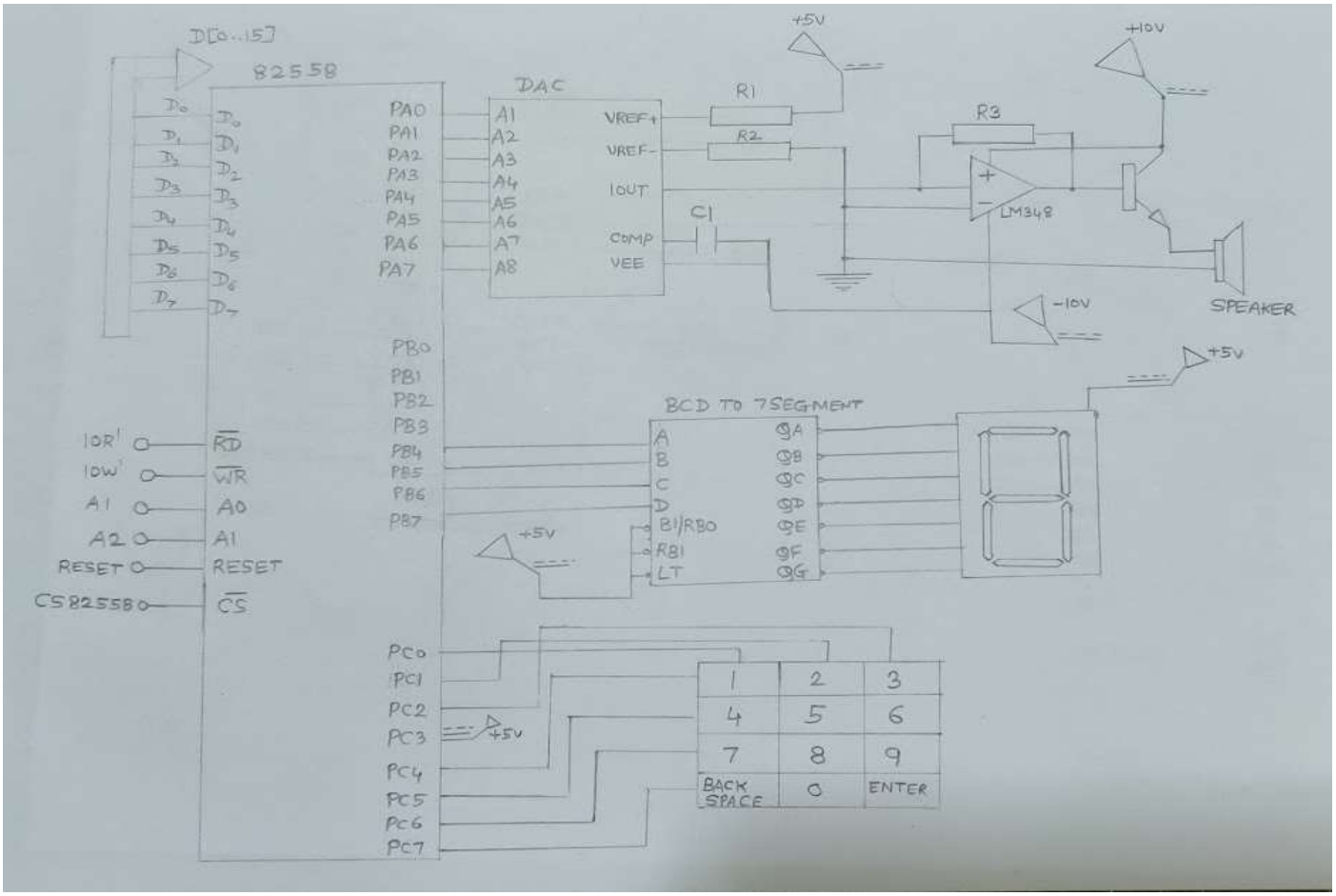



A[0....15]
A0
A3
A4
OR
A5
A6
A7
OR
M/IO'
U20
OR
CS8255A
A0
A3
A5
OR
M/IO'
OR
CS8255B
A6
A7
A4
NOT
OR
A0
A3
A4
OR
M/IO'
OR
CS8253
A5
NOT
A6
A7
OR
A0
A3
A6
OR
M/IO'
OR
CS8259
A4
NOT
A7
A5
NOT
OR

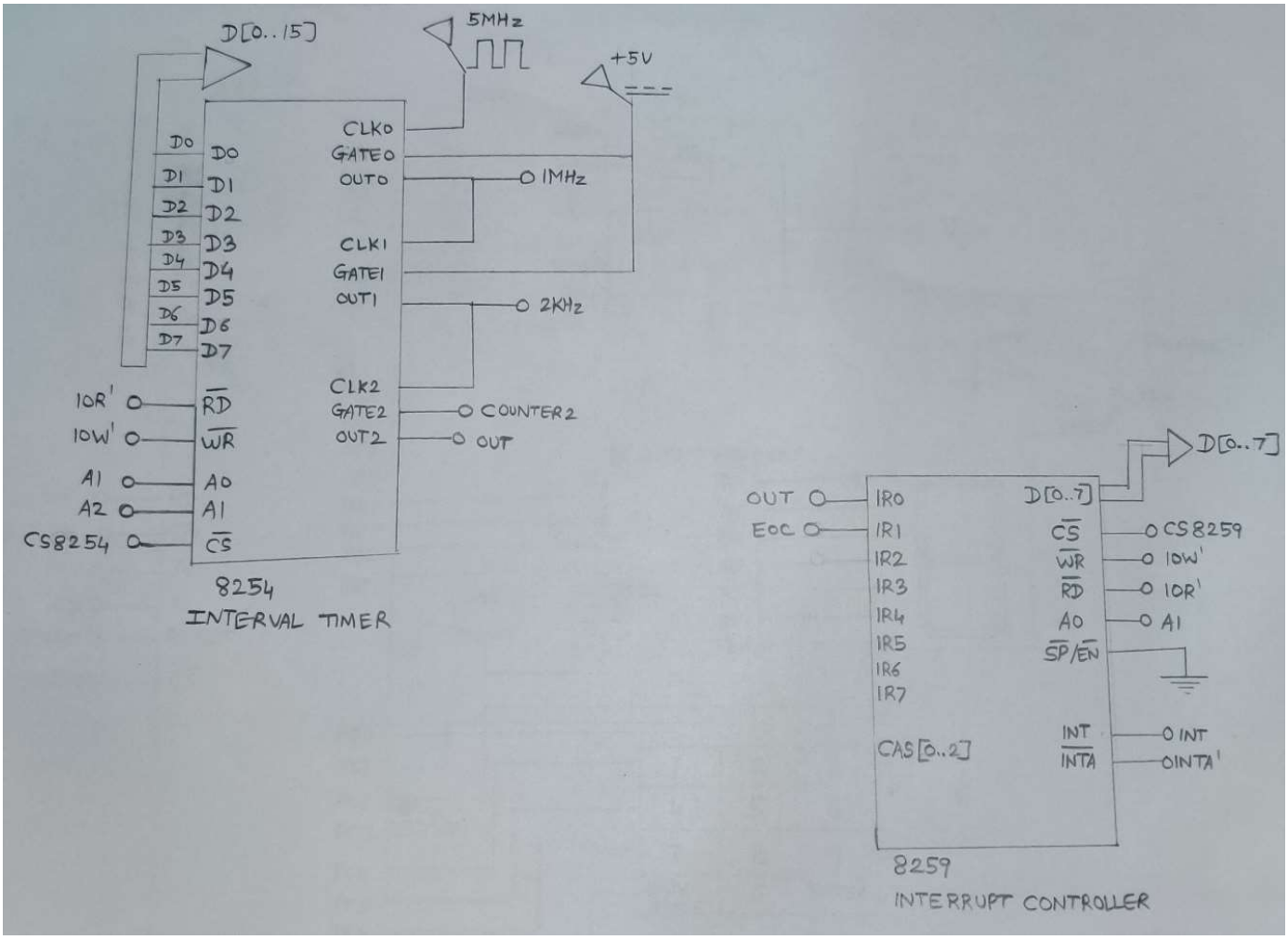
8255A


START
VCC
GROUND
SW-SPDT
D[0,15]
8255A
REPLAY
VCC
GROUND
SW-SPDT
OUT
REPLAY WITH A DIFFERENT DELAY
Vcc
GROUND
SW-DPDT
VDD
ADC
OE
A[0,15]
RD
WR
A1
A2
RESET
CS8255A
COUNTER2
SOC
OE
ALE
START LED
LED-GREEN
REPLAY LED
LED-GREEN
EOC
SOC
1MHz
START
CLOCK
ADC0808
MIC1

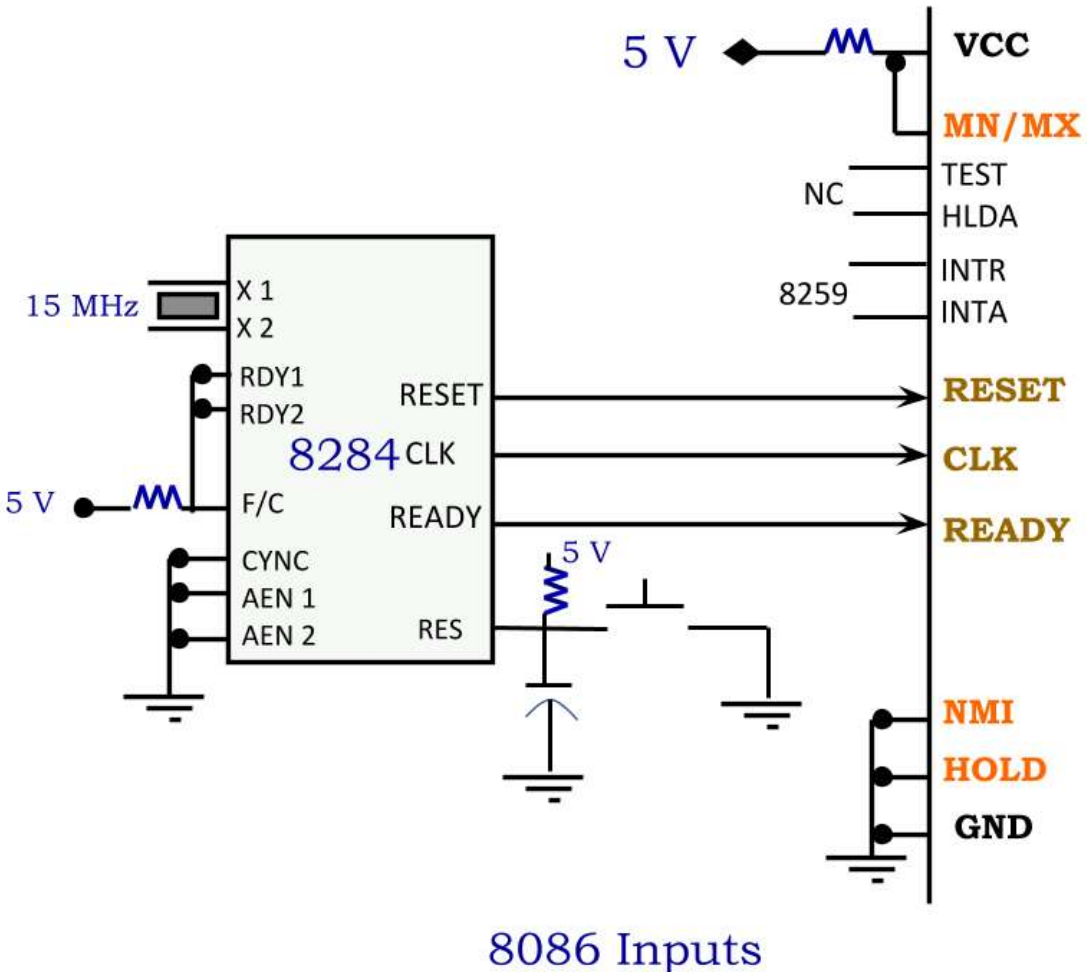
8255B


D[0..15]
82558
DAC
+5V
+10V
R1
R2
R3
C1
LM348
SPEAKER
-10V
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
A1
A2
A3
A4
A5
A6
A7
A8
VREF+
VREF-
IOUT
COMP
VEE
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
BCD TO 7SEGMENT
A
B
C
D
BI/RBO
RBI
LT
IOR'
IOW'
A1
A2
RESET
CS82558
RD
WR
A0
A1
RESET
CS
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
1
2
3
4
5
6
7
8
9
BACK SPACE
0
ENTER

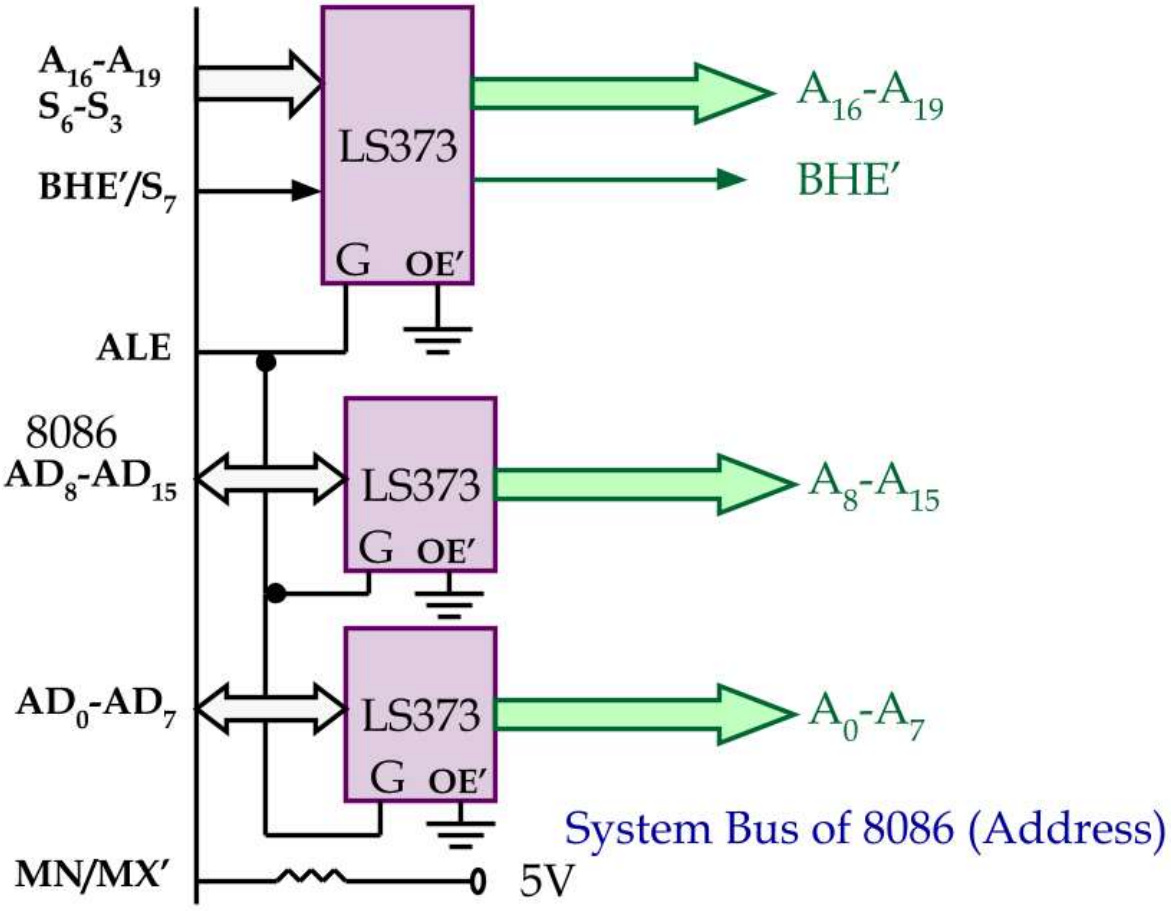
INTERRUPT CONTROLLER AND INTERVAL TIMER

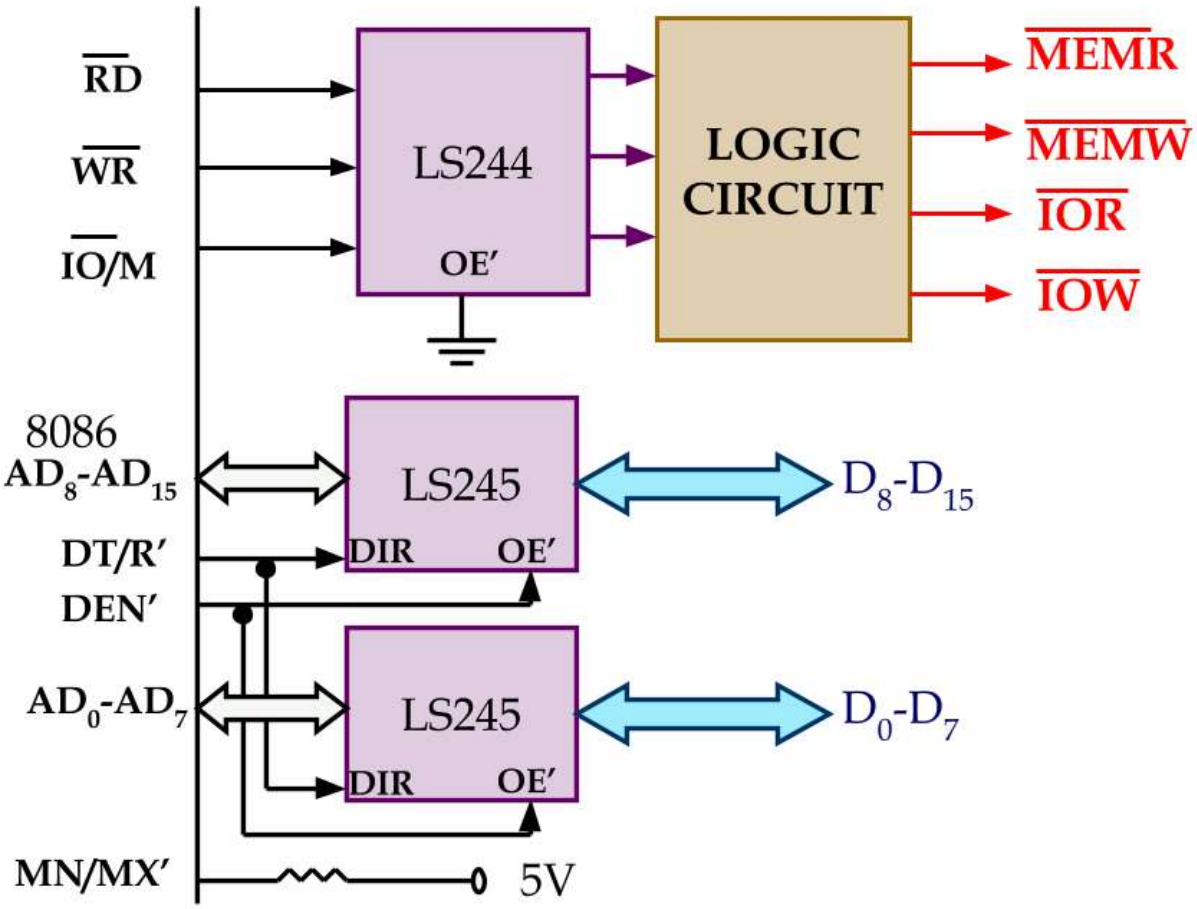


8284 CLOCK GENERATOR AND INPUTS TO 8086



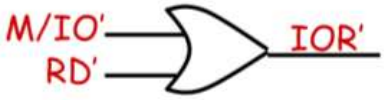
8086 Inputs

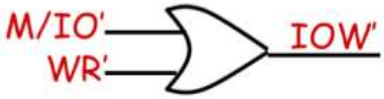

A16-A19
S6-S3
BHE'/S7
LS373
G
OE'
A16-A19
BHE'
ALE
8086
AD8-AD15
LS373
G
OE'
A8-A15
AD0-AD7
LS373
G
OE'
A0-A7
System Bus of 8086 (Address)
MN/MX'
5V



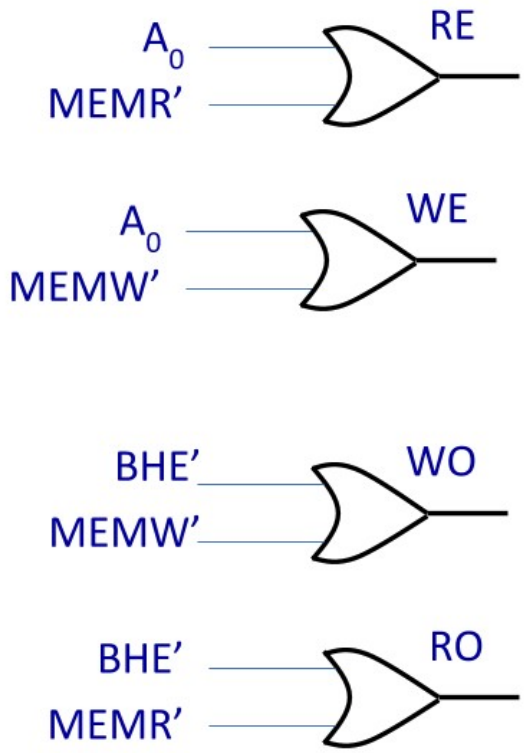
System Bus of 8086(Data + Control)

GENERATING RD' AND WR' FOR I/O DEVICES

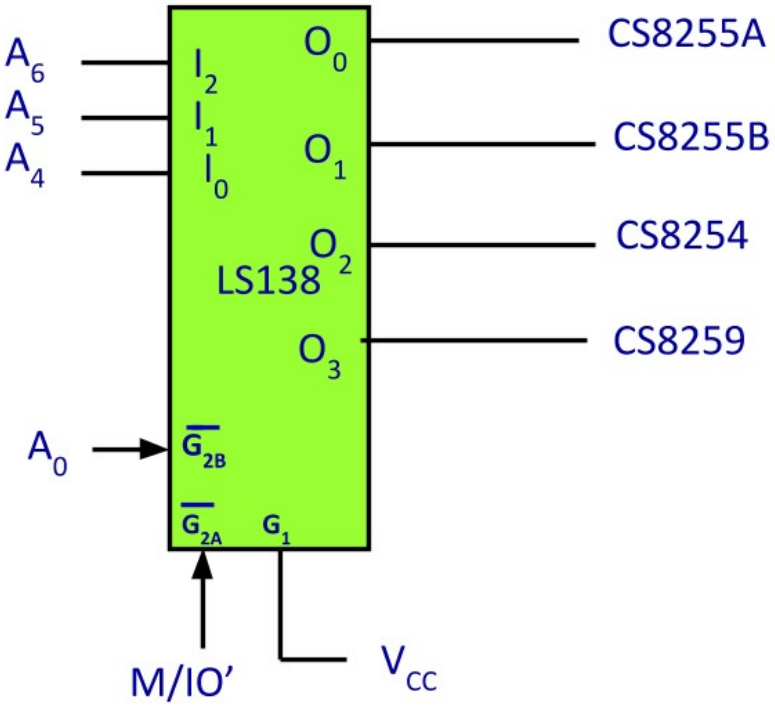




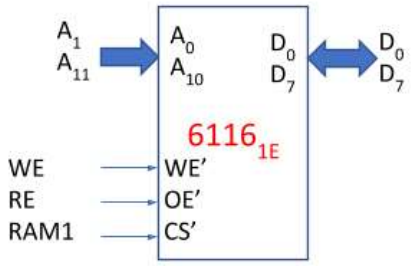
M/IO'	RD'	WR'	Bus cycle
1	0	1	MEMR'
1	1	0	MEMW'
0	0	1	IOR'
0	1	0	IOW'

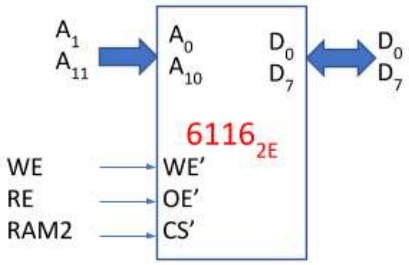

A_0
MEMR'
RE
A_0
MEMW'
WE
BHE'
MEMW'
WO
BHE'
MEMR'
RO

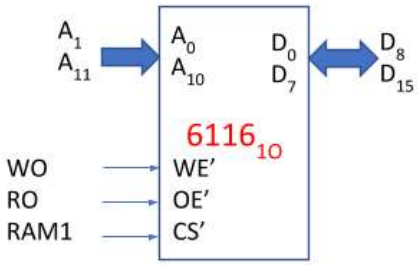
DECODING LOGIC FOR CHIPSELECT

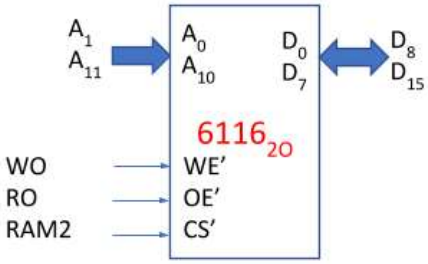


I/O Decoder

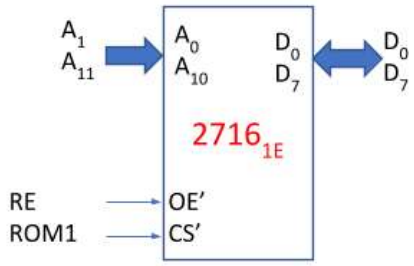


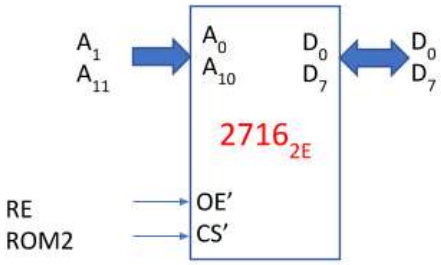


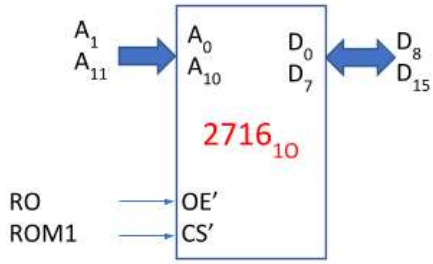


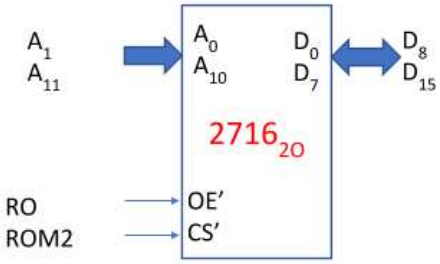


Memory Interfacing RAM

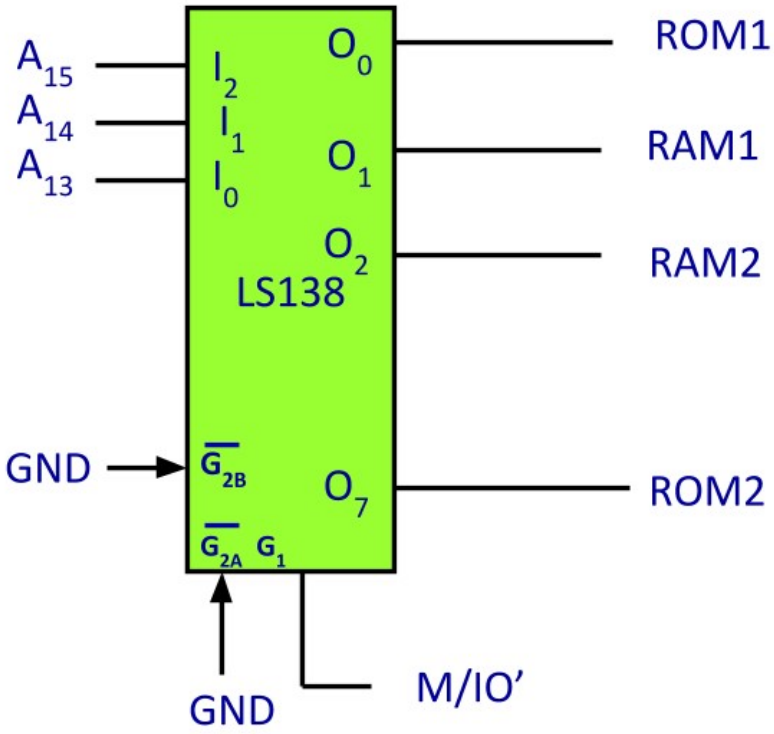






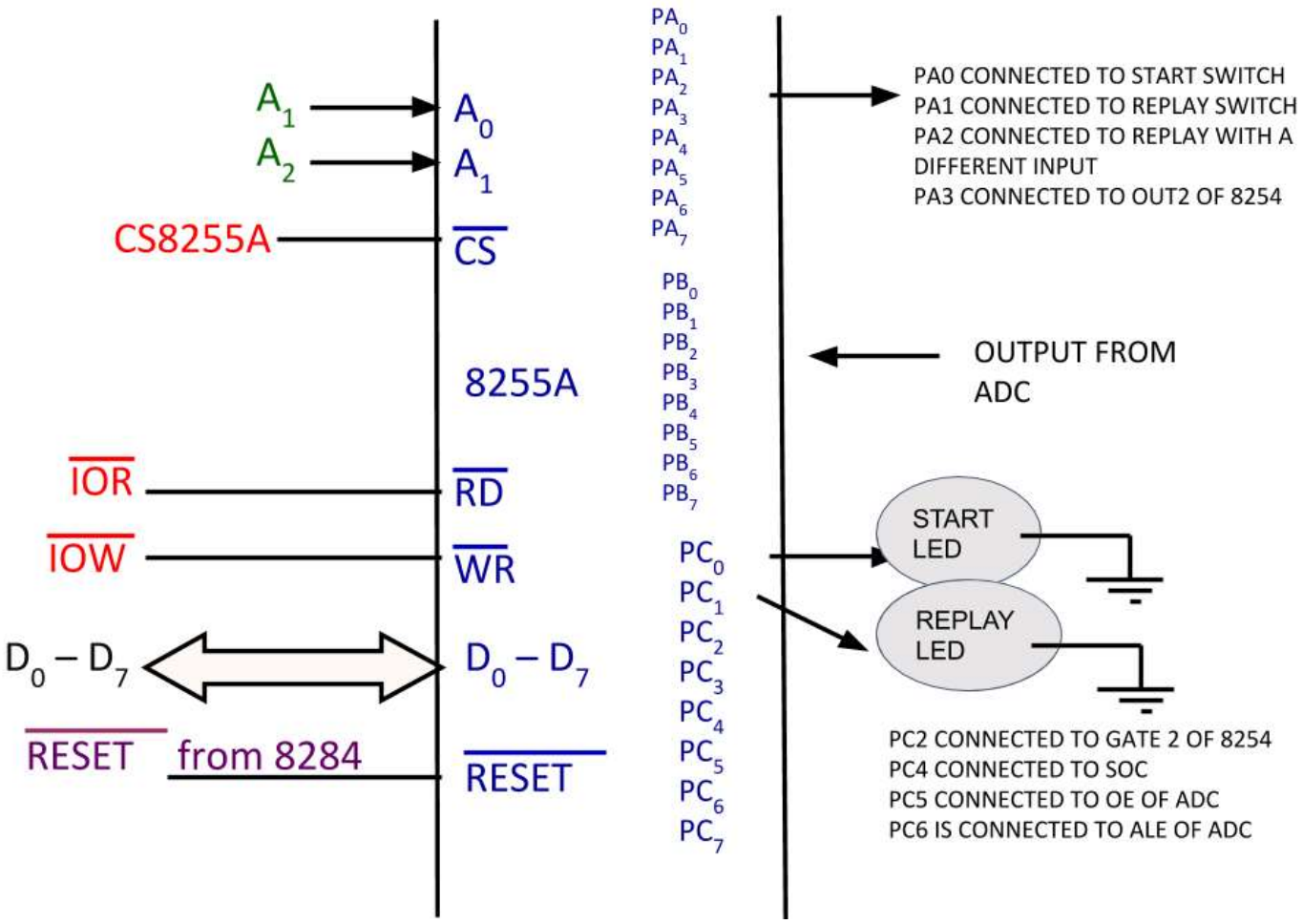


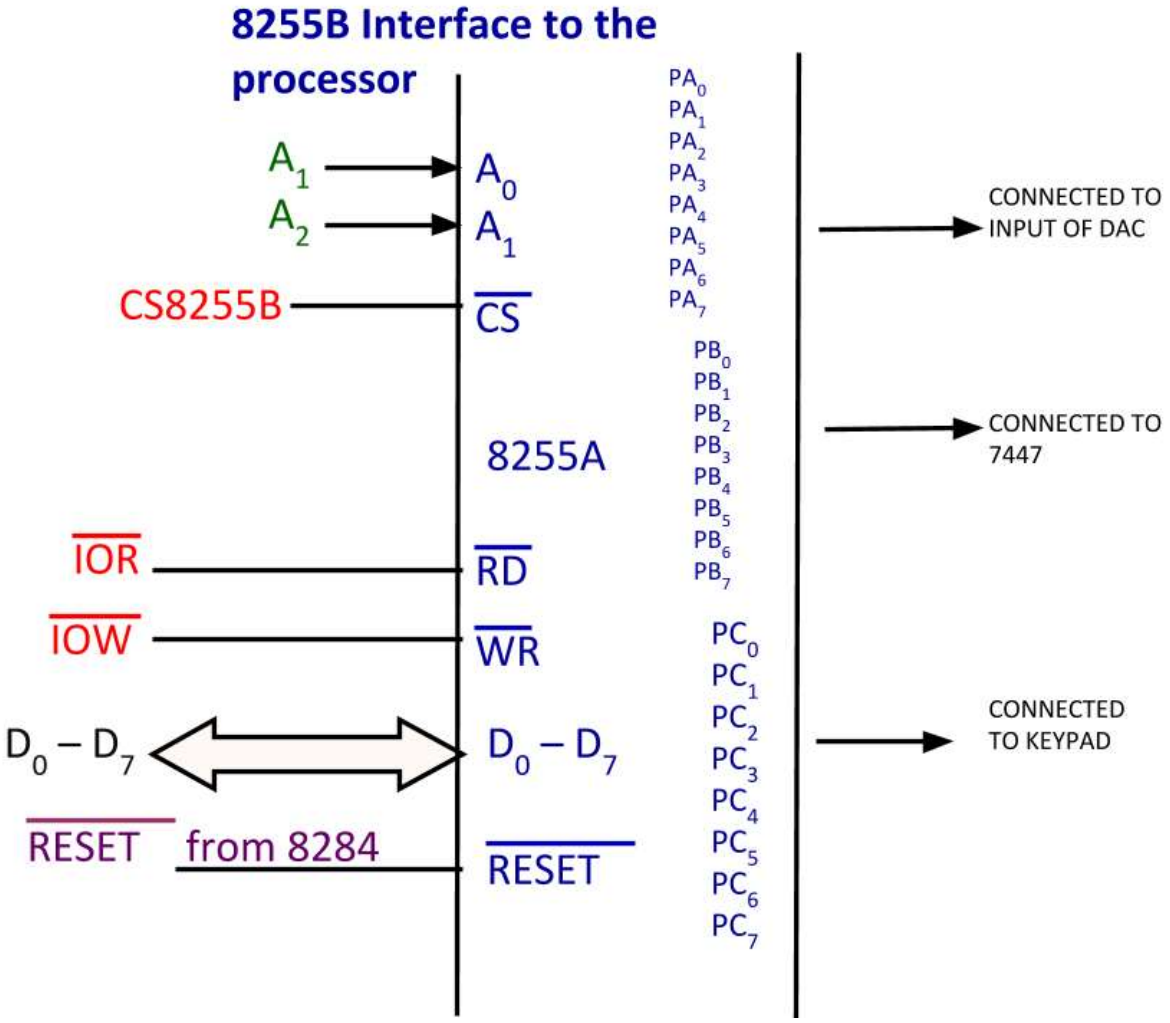
Memory Interfacing ROM

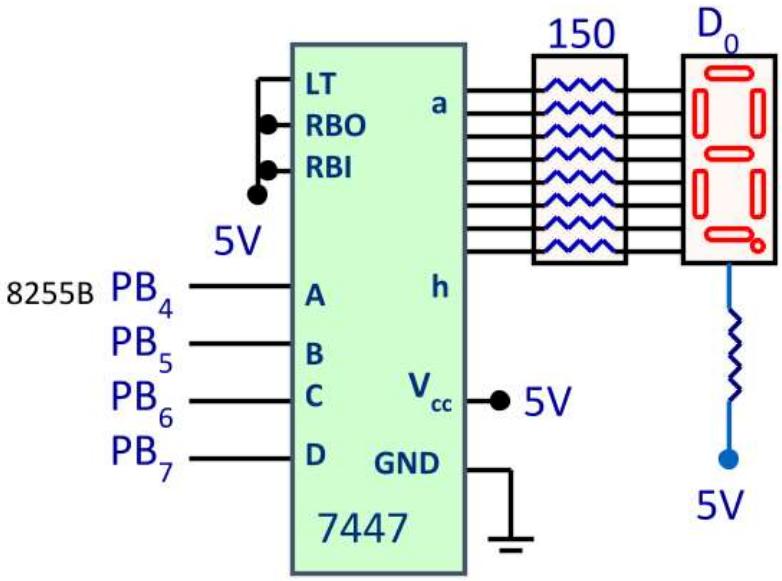


Memory Decoder for RAM and ROM

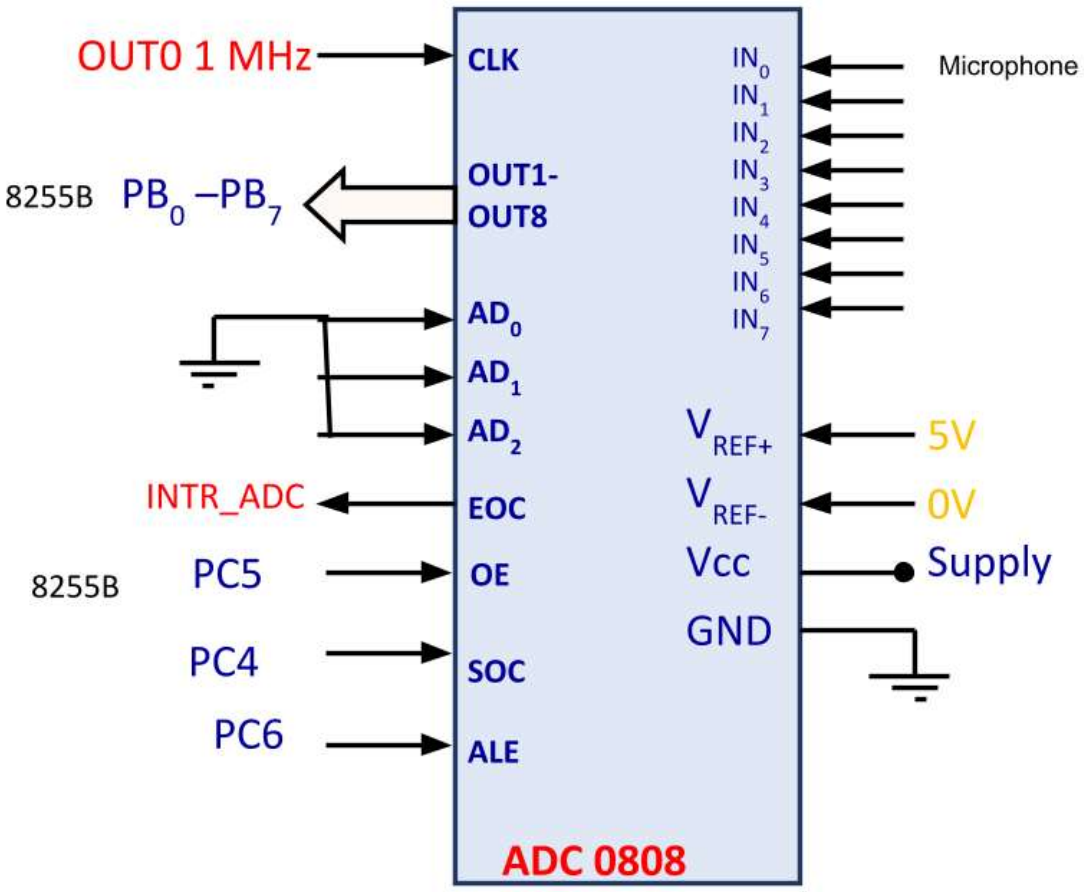
8255A Interface to the processor

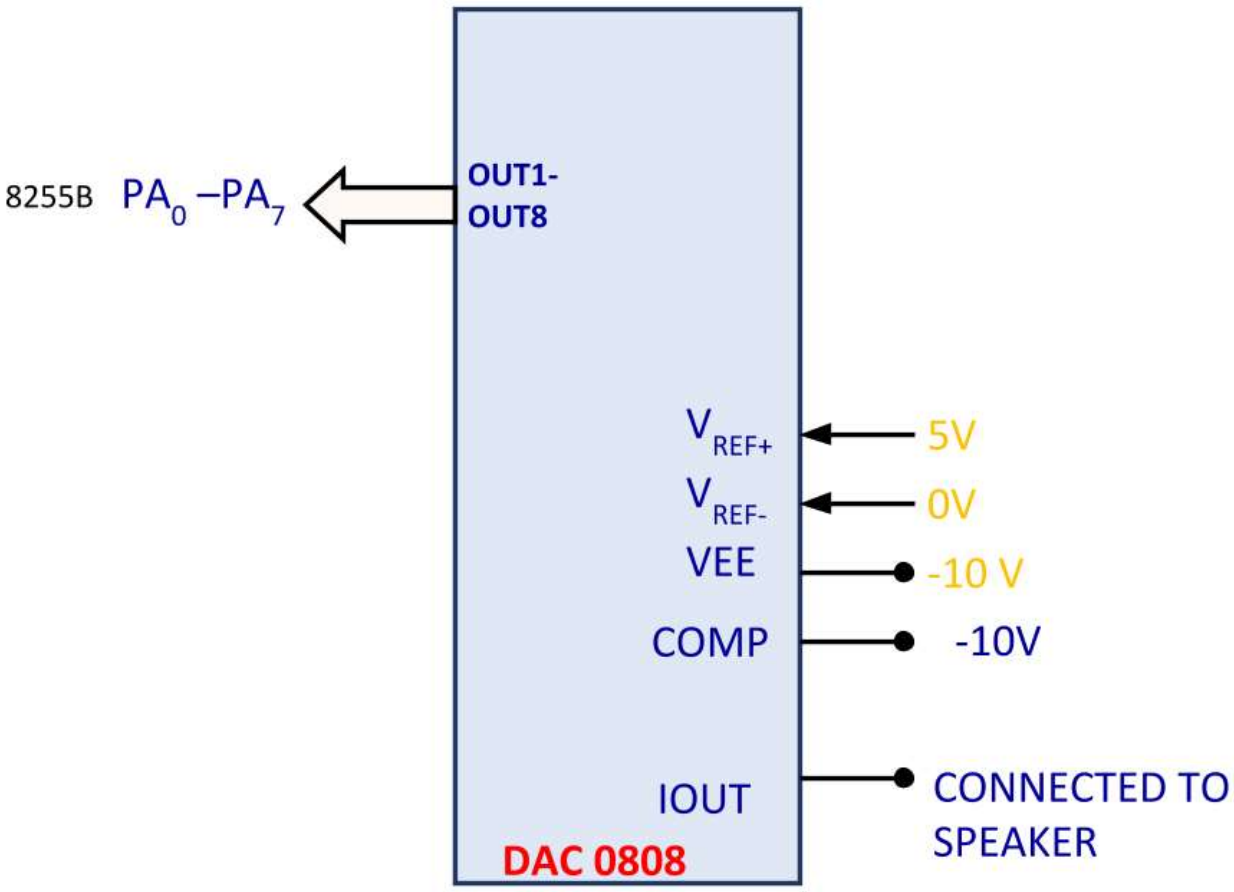



8255B Interface to the processor
A1
A2
A0
A1
CS8255B
CS
8255A
IOR
RD
IOW
WR
D0 – D7
D0 – D7
RESET from 8284
RESET
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
CONNECTED TO INPUT OF DAC
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
CONNECTED TO 7447
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
CONNECTED TO KEYPAD

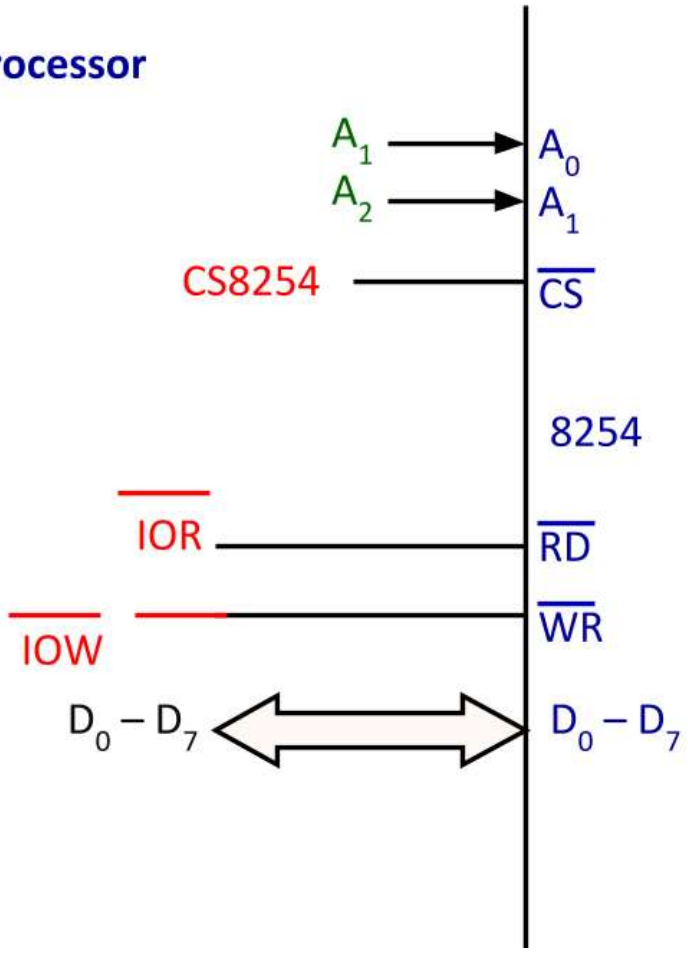


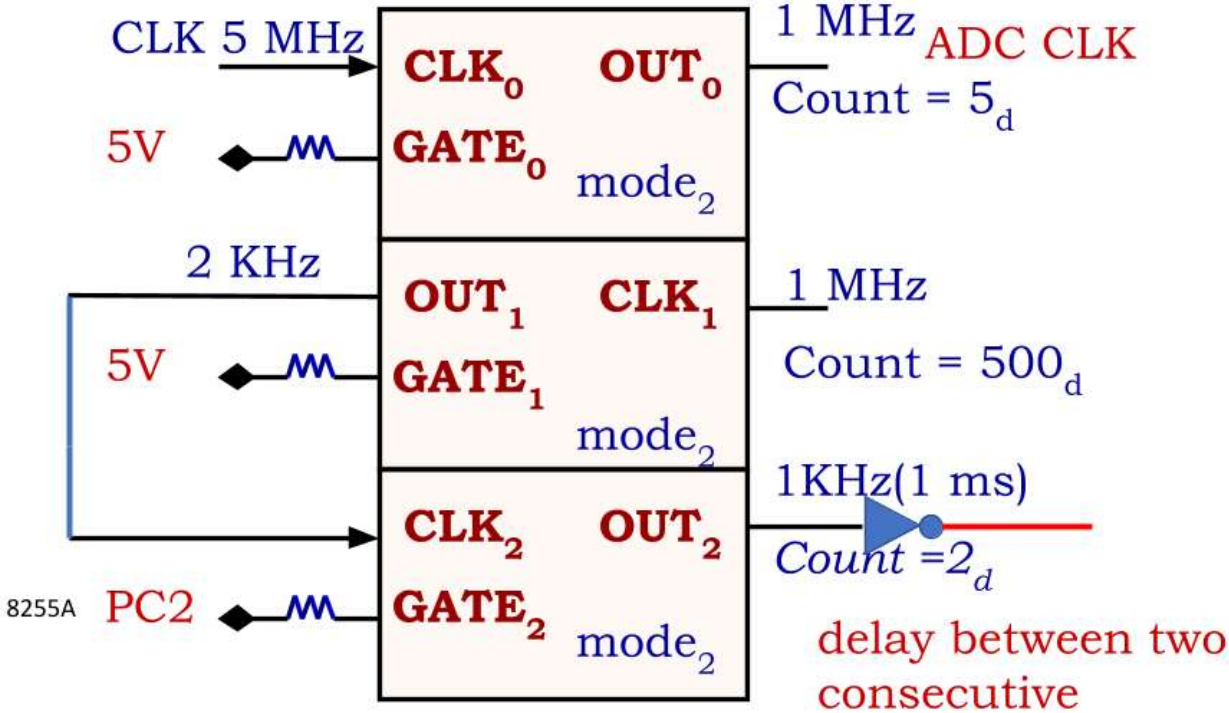
KEY PRESSED DISPLAYED ON 7SEG LED

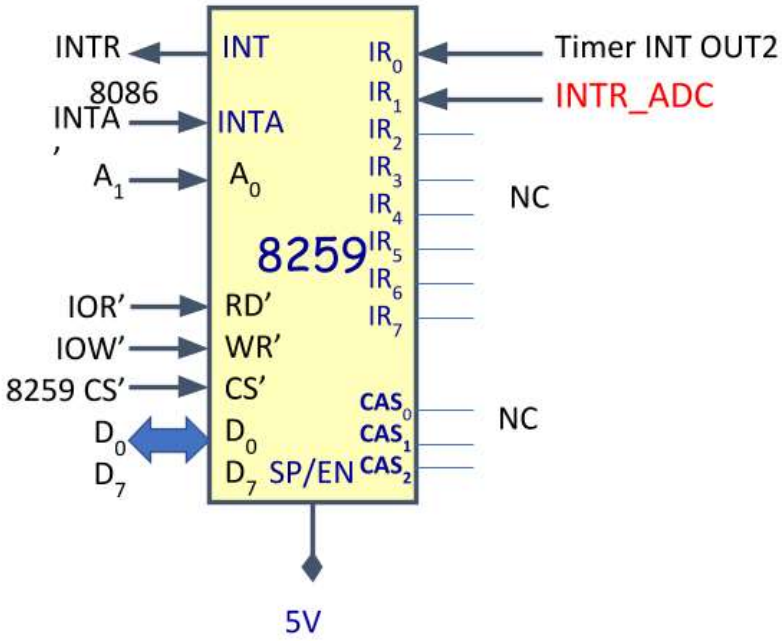

OUT0 1 MHz
CLK
8255B
PB0 –PB7
OUT1-
OUT8
AD0
AD1
AD2
INTR_ADC
EOC
8255B
PC5
OE
PC4
SOC
PC6
ALE
ADC 0808
IN0
IN1
IN2
IN3
IN4
IN5
IN6
IN7
Microphone
VREF+
5V
VREF-
0V
Vcc
Supply
GND


8255B
PA0 –PA7
OUT1-
OUT8
VREF+
5V
VREF-
0V
VEE
-10 V
COMP
-10V
IOUT
CONNECTED TO
SPEAKER
DAC 0808

8254 Interface to the processor




CLK 5 MHz
CLK0
OUT0
1 MHz
ADC CLK
Count = 5d
5V
GATE0
mode2
2 KHz
OUT1
CLK1
1 MHz
5V
GATE1
Count = 500d
mode2
1KHz(1 ms)
CLK2
OUT2
Count =2d
8255A
PC2
GATE2
mode2
delay between two consecutive samples
8254


INTR
8086
INTA
'
A1
IOR'
IOW'
8259 CS'
D0
D7
INT
INTA
A0
8259
RD'
WR'
CS'
D0
D7
SP/EN
IR0
IR1
IR2
IR3
IR4
IR5
IR6
IR7
CAS0
CAS1
CAS2
Timer INT OUT2
INTR_ADC
NC
NC
5V

8259