

Packaging Evolution: From Basics to 3D Integration

Module 3: Thermal Simulations of Semiconductor Packages Using ANSYS

This module provides a hands-on walkthrough for performing thermal simulations of Flip-Chip BGA semiconductor packages using **ANSYS Icepak**, part of the **ANSYS Electronics Desktop (AEDT)** suite. The process includes package modelling, power source assignment, meshing, and thermal analysis with visualization.

3.1 Introduction to ANSYS Electronics Desktop (AEDT)

ANSYS Electronics Desktop is a unified simulation environment that integrates:

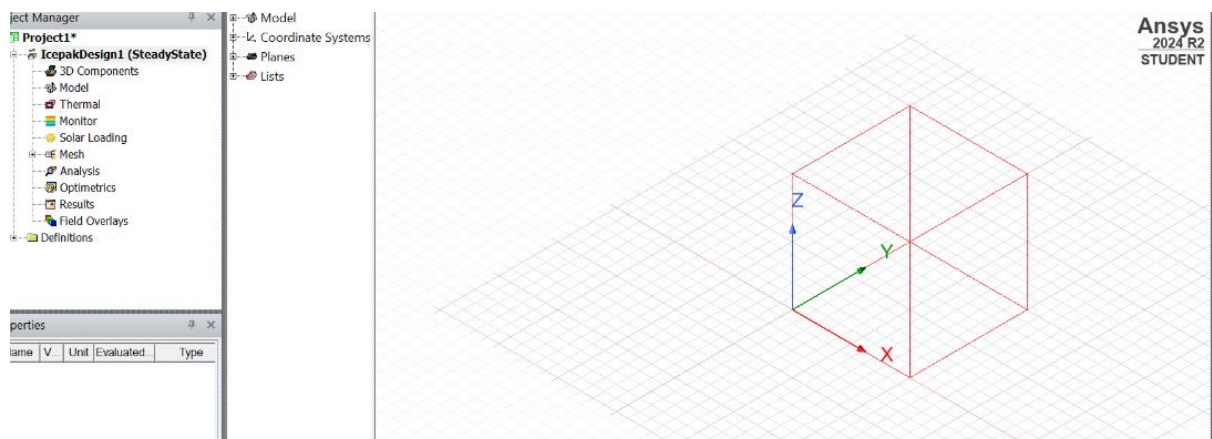
- **Electromagnetic (EM) Simulation**
- **Thermal Analysis**
- **Signal and Power Integrity Checks**
- **Electromechanical Co-simulation**

It is widely adopted in electronic systems design, particularly for PCBs, IC packages, and complete systems.

3.2 Setting Up a Flip-Chip BGA Package in Icepak

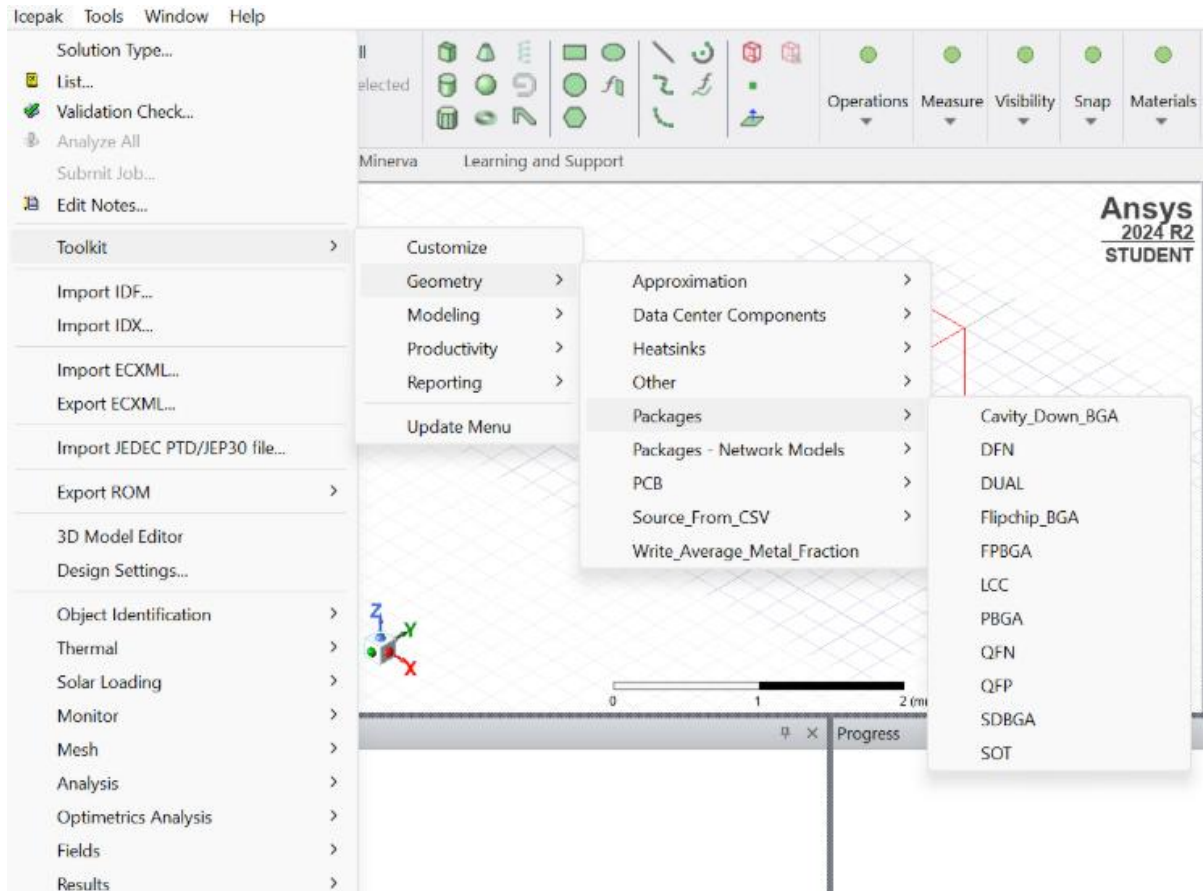
Step 1: Launch Icepak

- Open **ANSYS Workbench**
- Navigate to Project → Insert Icepak Design
- Click the **Icepak** tab to enter the modelling interface

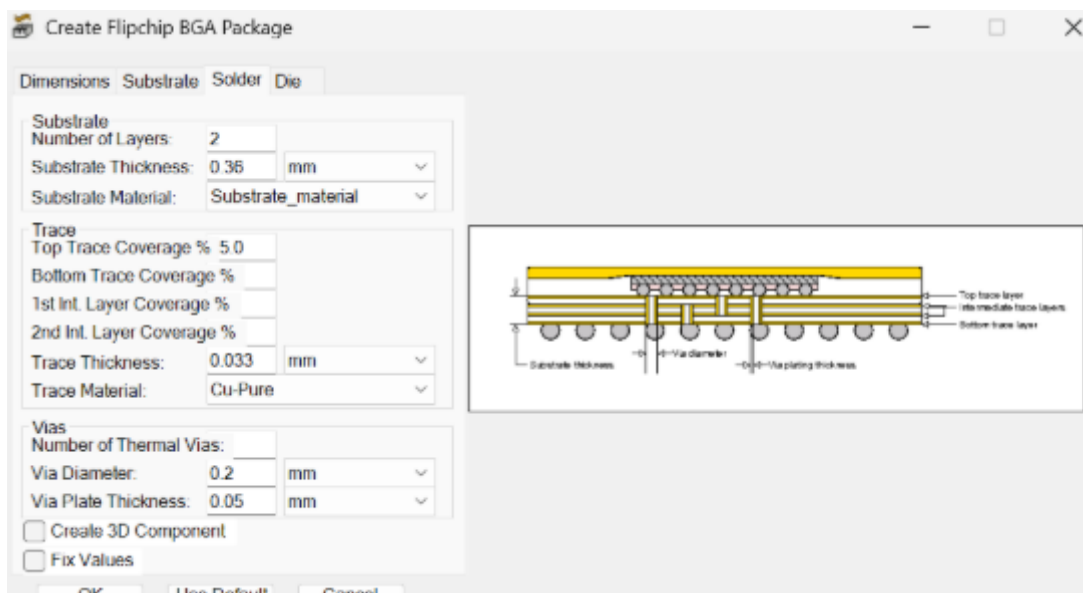
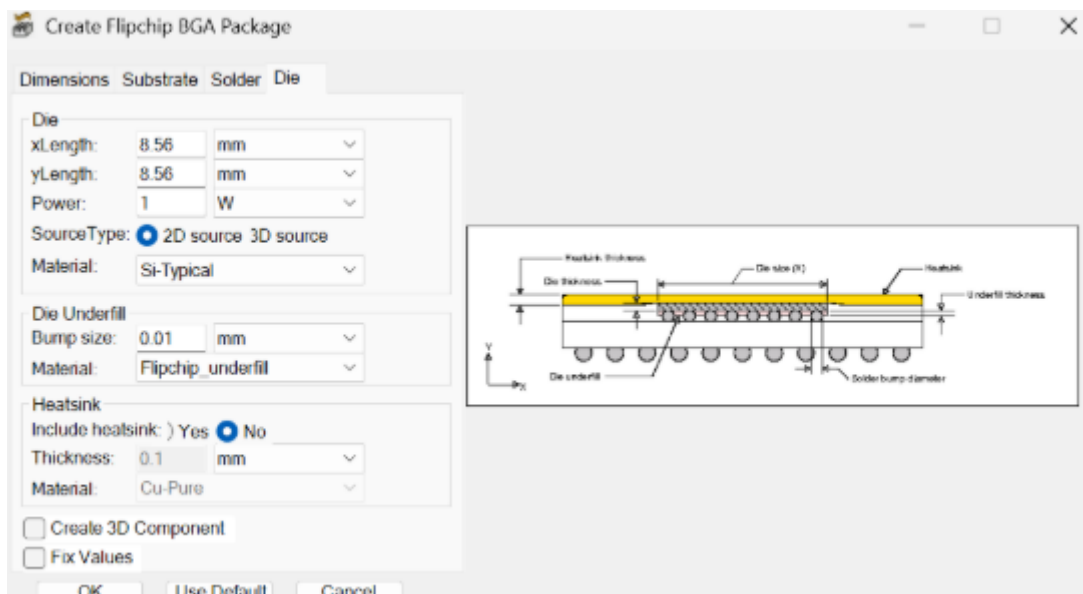
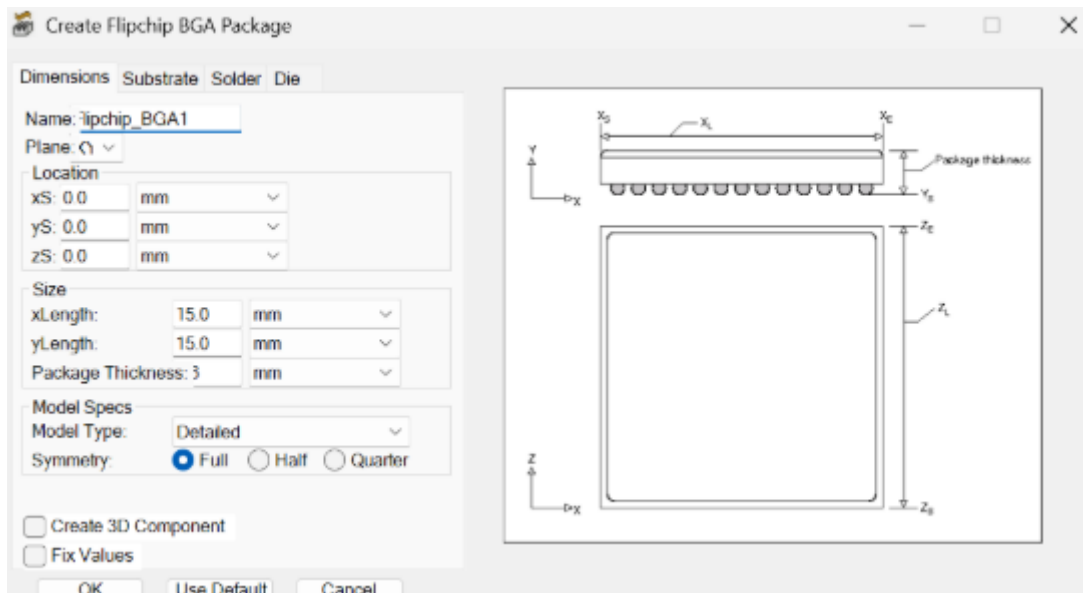


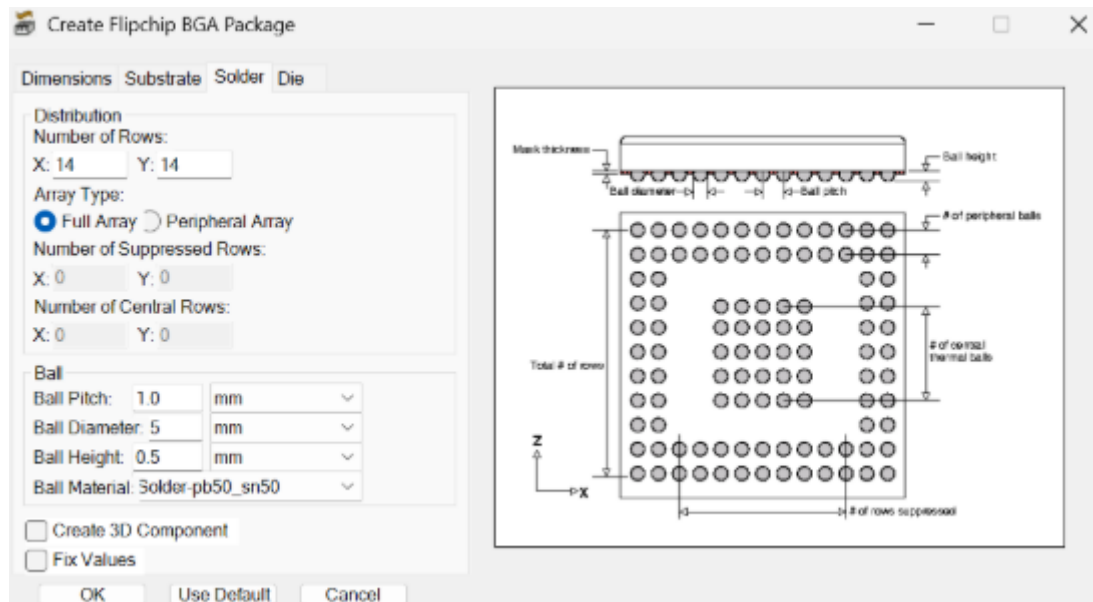
Step 2: Create Flipchip BGA Package

- Go to Toolkit → Geometry → Packages → Flipchip_BGA

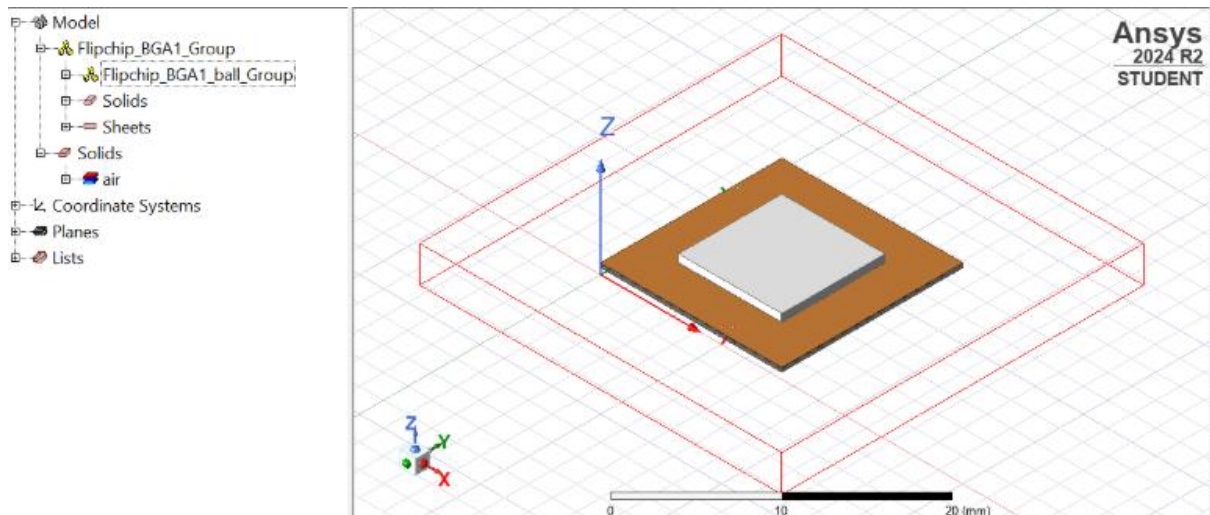


- In the configuration window, input:
 - xLength:** 15 mm
 - yLength:** 15 mm
 - Package Thickness:** 3 mm
 - Model Type:** Detailed
 - Symmetry:** Full



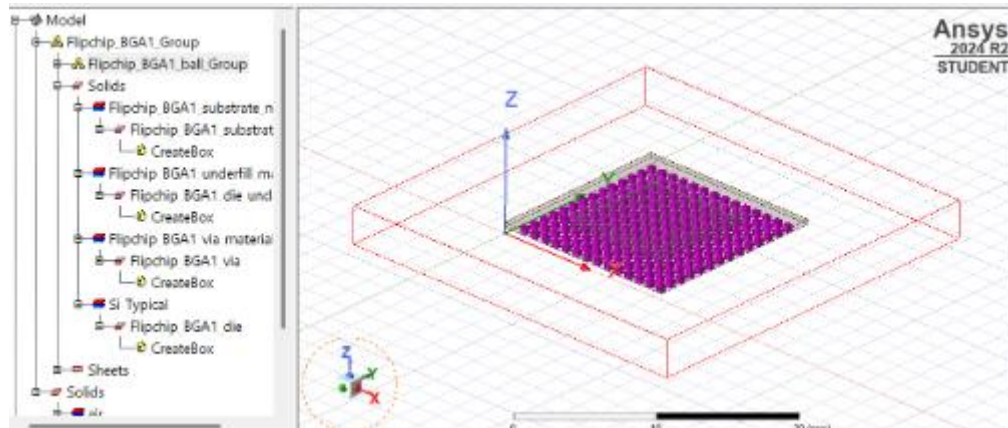


- Click **OK** to generate the 3D model

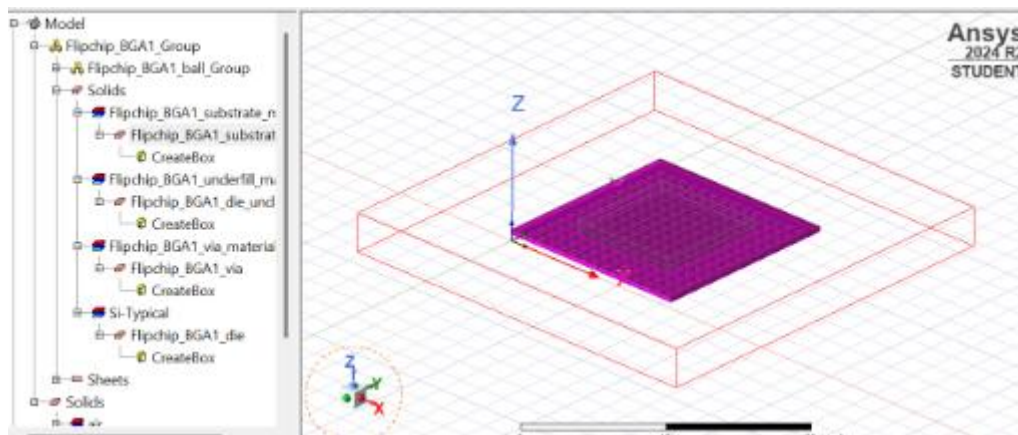


Step 3: Explore the Package Components

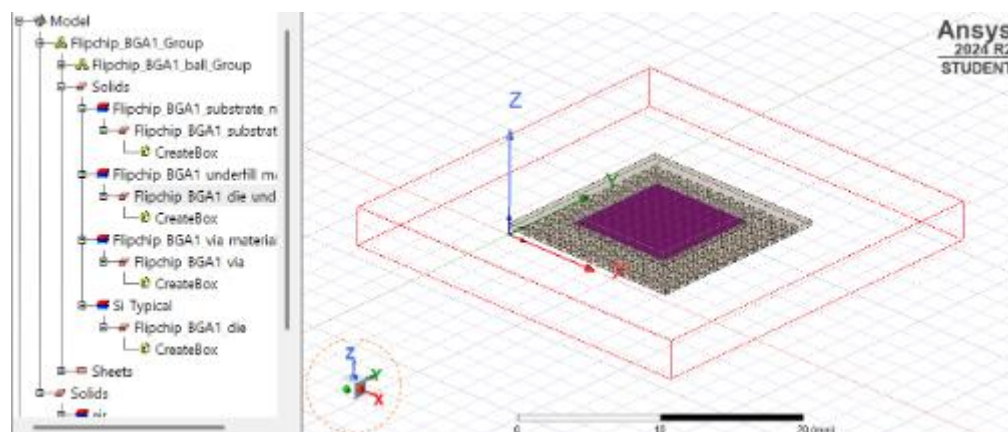
- In the **Model Tree**, expand Solids to view:
 - Ball Group



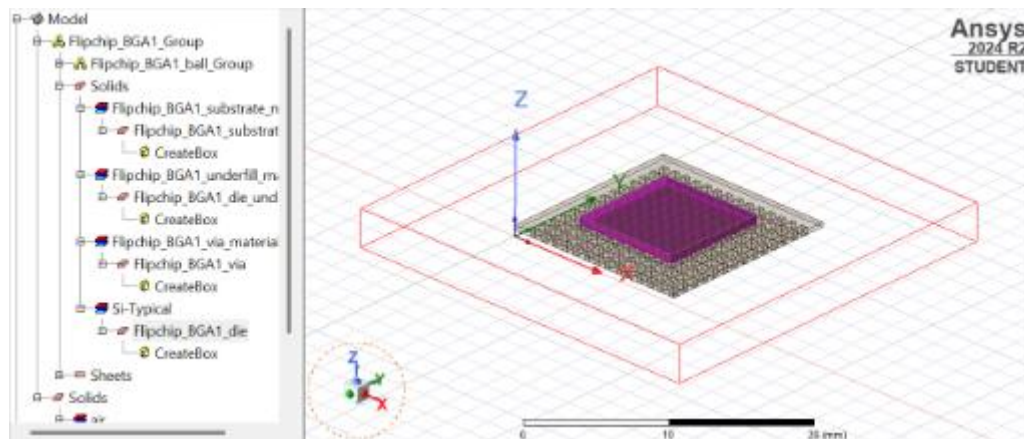
- Substrate



- Die Underfill



- Die



3.3 Material Definitions and Power Assignment

Step 4: Review Material Assignments

- Check and update material properties for all solids if needed (e.g., epoxy, silicon, copper).

Design List: Project1 - IcepakDesign1

Model | Thermal | Monitors | SolarLoading | Mesh Region | Mesh Operation | Analysis Setup

Name	Color	Model	Display Wire...	Visible	Material	Type
Region		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	air	Solid
Flipchip_BGA1_die		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Si-Typical	Solid
Flipchip_BGA1_die_source		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		Sheet
Flipchip_BGA1_die_underfill		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Flipchip_BGA1_underfill_material	Solid
Flipchip_BGA1_substrate		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Flipchip_BGA1_substrate_material	Solid
Flipchip_BGA1_via		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Flipchip_BGA1_via_material	Solid
Flipchip_BGA1_trace1		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>		Sheet
Flipchip_BGA1_ball		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Solder-pb50_sn50	Solid
Flipchip_BGA1_ball_1		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Solder-pb50_sn50	Solid
Flipchip_BGA1_ball_2		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Solder-pb50_sn50	Solid
Flipchip_BGA1_ball_3		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Solder-pb50_sn50	Solid
Flipchip_BGA1_ball_4		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Solder-pb50_sn50	Solid
Flipchip_BGA1_ball_5		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Solder-pb50_sn50	Solid
Flipchip_BGA1_ball_6		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	Solder-pb50_sn50	Solid

Delete | Properties | Select | Done

Step 5: Assign Thermal Power Sources

5.1 For the Die:

- Under Project Manager → Thermal, locate BGA1_die_source
- Set **Thermal Power Input: 1 W**

- Choose “Source Thermal Model”

Source Thermal Model

General | Defaults

Name: Flipchip_BGA1_die_source

Thermal Specification

Thermal Condition: Total Power

Total Power: 1 W ☐ Temp Dep [Edit](#)

☐ Radiation

Voltage/Current Specification

☐ Voltage/Current

☒ Current: 0 A

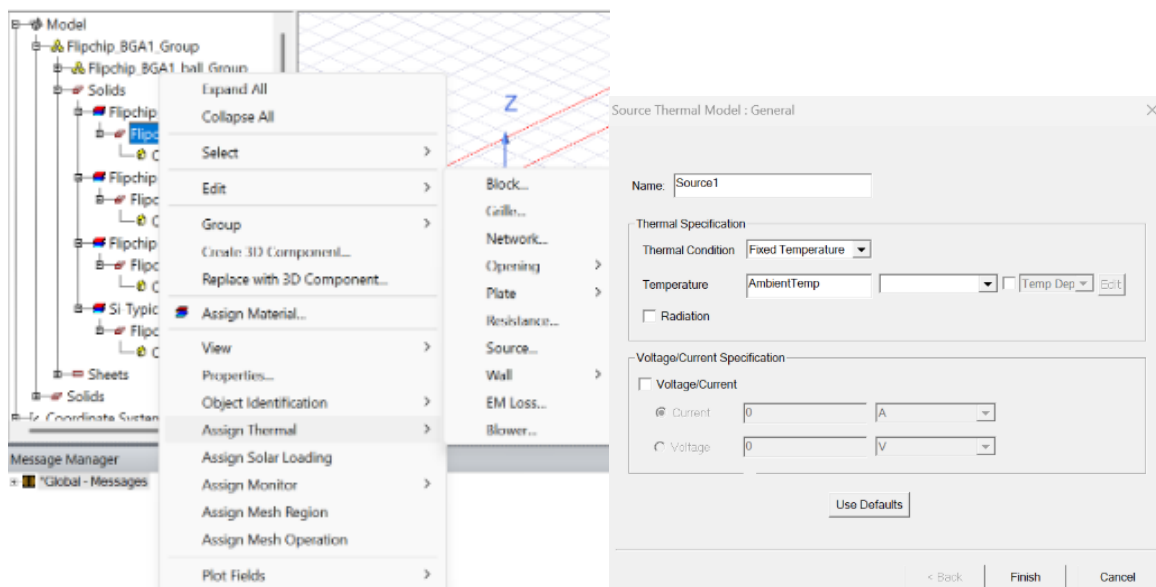
☐ Voltage: 0 V

[Use Defaults](#)

[OK](#) [Cancel](#)

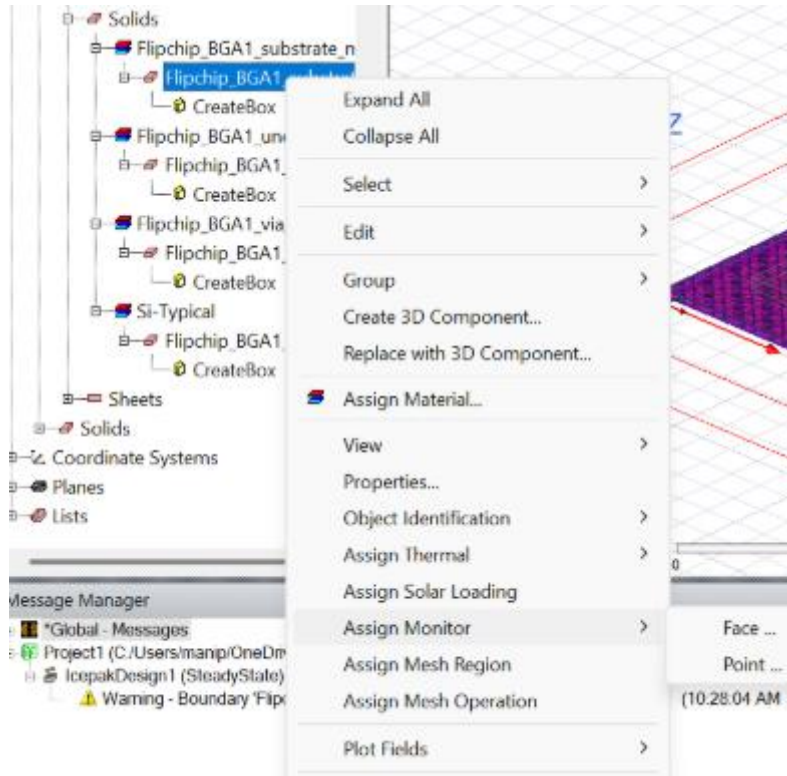
5.2 For the Substrate:

- Right-click Flipchip_BGA1_substrate → Assign Thermal → Source
- Set **Thermal Condition** to **Fixed Temperature (Ambient)**



Step 6: Add Temperature Monitors

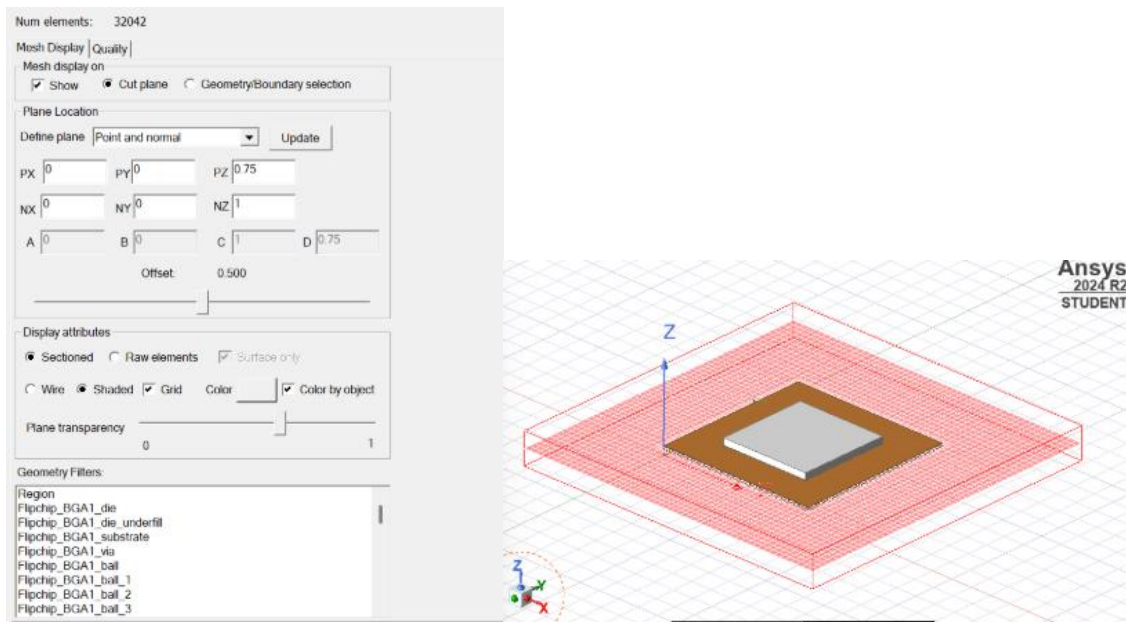
- Right-click each component (Substrate, Die, Underfill)
- Choose Assign Monitor → Point
- Select **Temperature** and click **OK**



3.4 Meshing and Analysis Setup

Step 7: Generate Mesh

- Go to the Simulation tab → Click Generate Mesh
- Save the file if prompted
- Wait for the mesh to complete; resolve or note any warnings

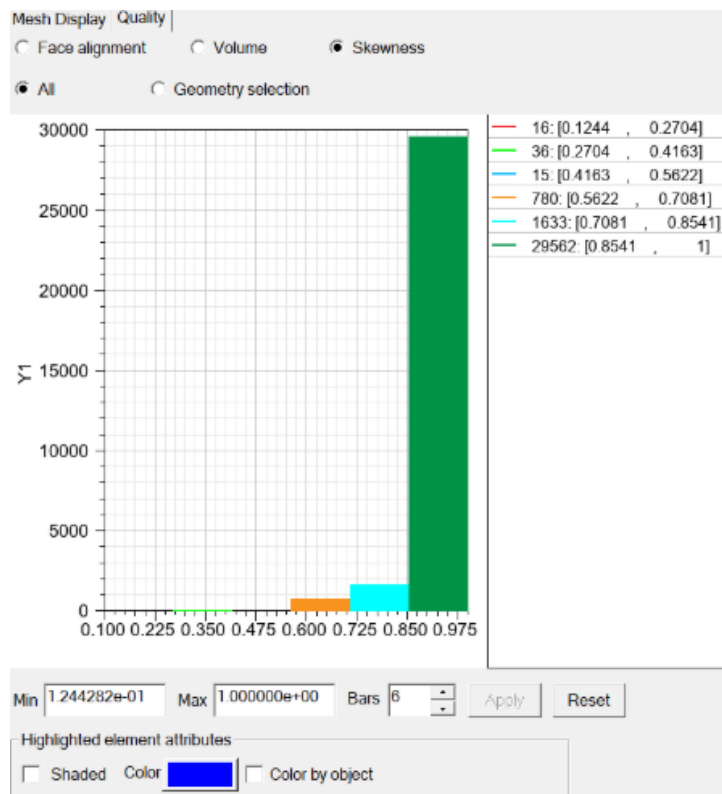


Step 8: Review Mesh Quality

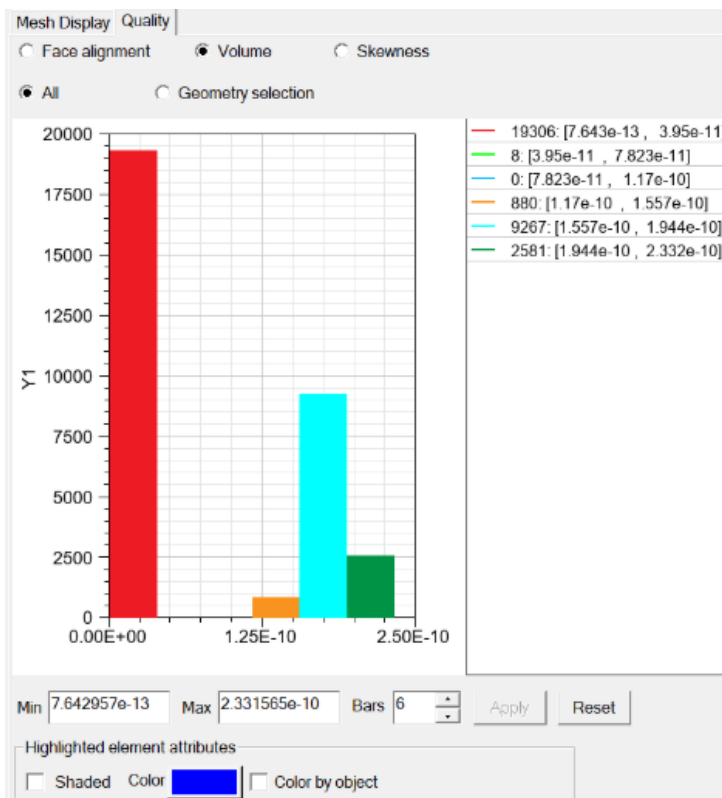
- Go to Mesh Visualization → Quality
- Inspect:
 - Face Alignment



- **Skewness**

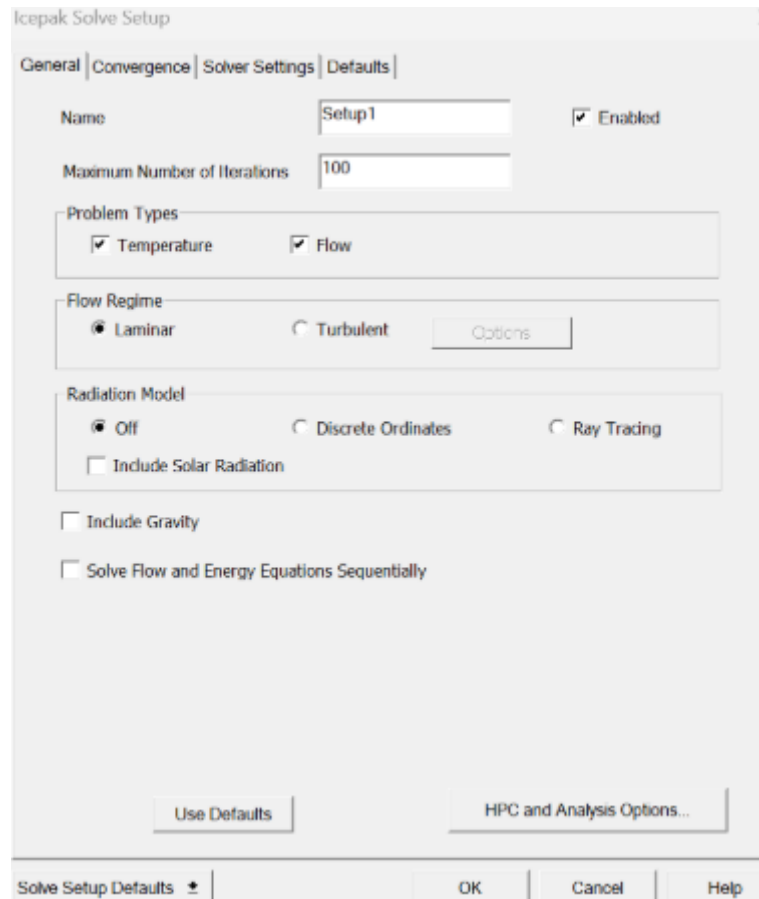


- **Element Volume**



Step 9: Add Thermal Analysis Setup

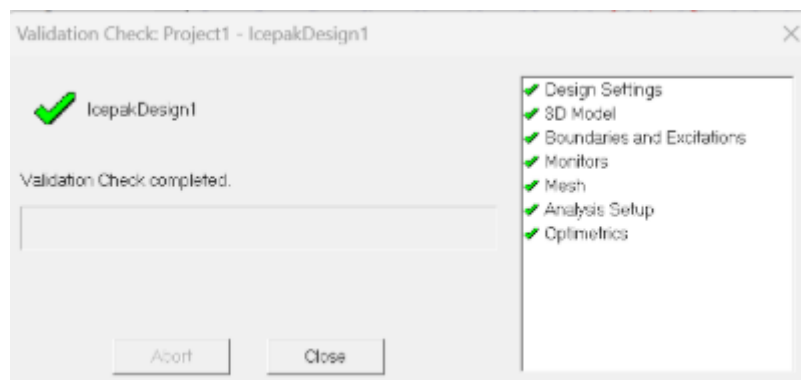
- In Project Manager, right-click Analysis → Add Analysis Setup
- Use default solver settings unless customization is required



3.5 Running Simulation and Viewing Results

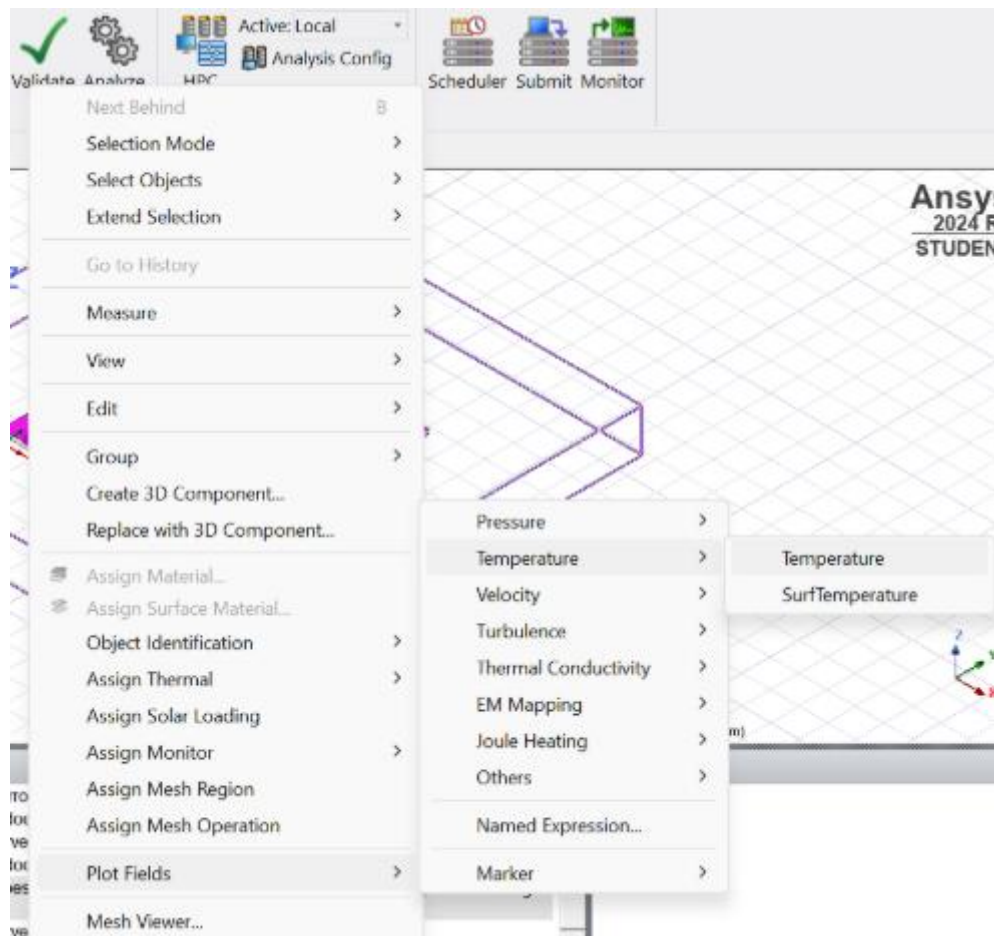
Step 10: Validate the Simulation

- Click Validate in the top toolbar
- Ensure all green ticks are shown, this confirms a correct setup



Step 11: Run Simulation and Plot Temperature Field

- Click Analyse All to start the solver
- Upon completion, select the Flipchip - BGA package in 3D view
- Right-click → Plot Fields → Temperature → Temperature
- In Plot Settings:
 - Enable **Specify Name/Folder**
 - Choose **Plot on Surface Only**
 - Enable **Gaussian Smoothing** for clarity



Final Output

A complete thermal simulation of the Flipchip BGA package is successfully executed for a **1 W power input**, with the temperature distribution visualized over the package components.

