Packaging Evolution: From Basics to 3D Integration

Module 1: Evolution of Semiconductor Packaging – From Fundamentals to Advanced Integration

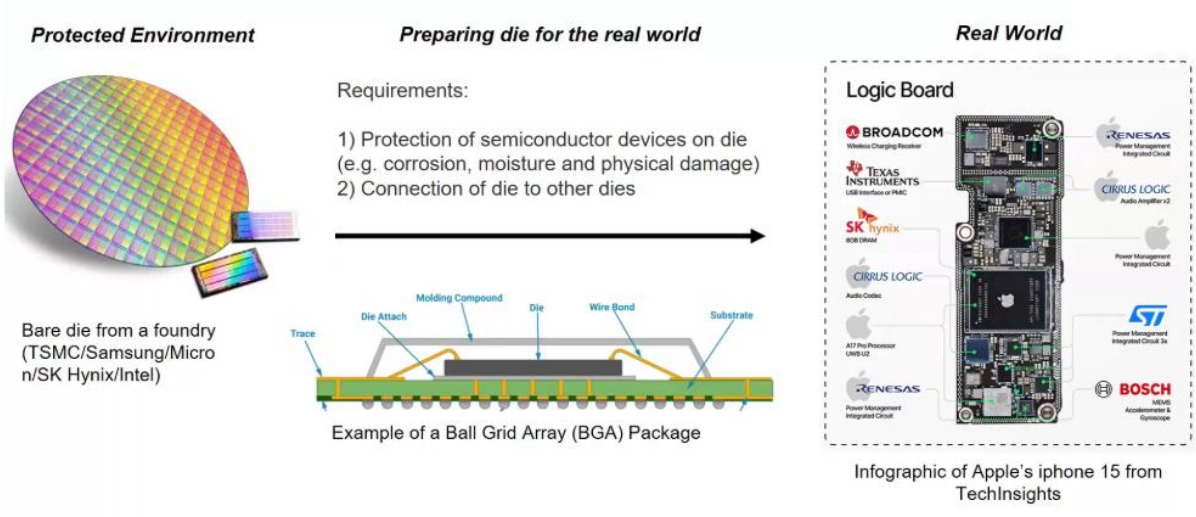
This module offers a comprehensive overview of semiconductor packaging, starting from the basics and progressing through advanced integration technologies such as 2.5D and 3D packaging.

1.1 Introduction to Semiconductor Packaging and the Industry Landscape

Semiconductor packaging is the final stage of device manufacturing, where the silicon die is enclosed in a protective structure. This process not only enables electrical connectivity but also provides environmental protection, turning the raw chip into a usable component for electronic systems.

Key Functions of a Semiconductor Package:

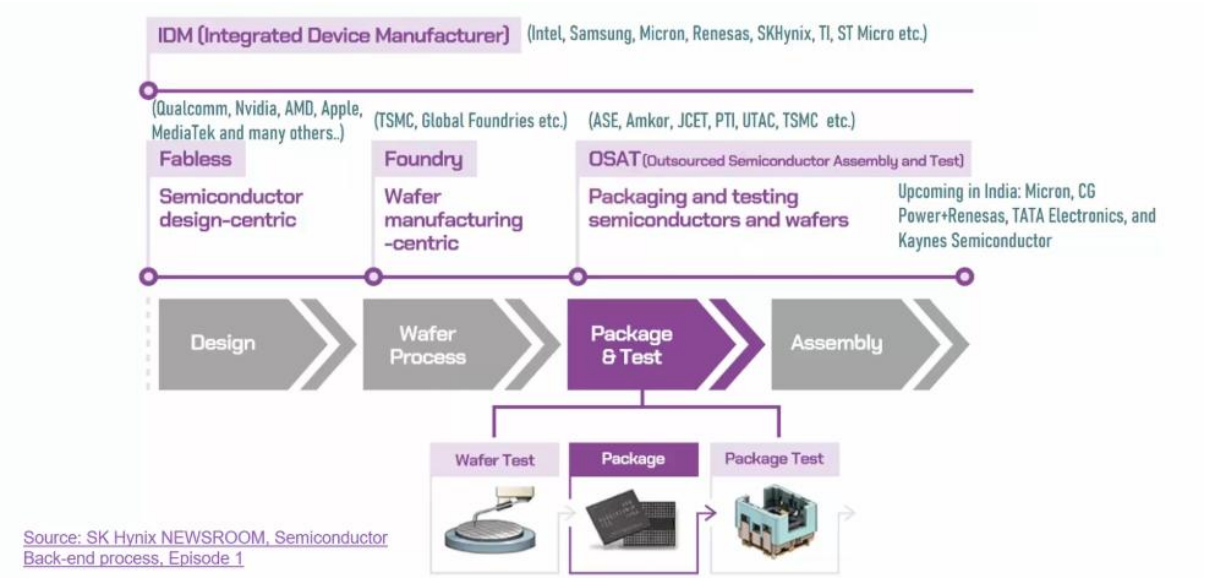
- **Protection:** Shields the chip from physical damage, dust, moisture, corrosion, and electrostatic discharge.
- **Electrical Interface:** Offers connectivity through pins, balls, or pads for integration with circuit boards.
- **Mechanical Support:** Provides structural stability within the electronic assembly.
- **Thermal Management:** Facilitates heat dissipation to maintain performance and prevent overheating.



Infographic of Apple's iphone 15 from TechInsights

Key Industry Stakeholders:

- **Fabless Designers:** Companies like Apple and Qualcomm that design chips but outsource fabrication.
- **Foundries:** Facilities such as TSMC and GlobalFoundries that manufacture the chips.
- **OSATs (Outsourced Semiconductor Assembly and Test):** Companies like ASE and Amkor that handle packaging and testing.
- **IDMs (Integrated Device Manufacturers):** Vertically integrated firms like Intel that manage everything from design to production.



1.2 Understanding Packaging Requirements and Common Types

Choosing the right packaging solution depends on a variety of interrelated factors:

Package Selection Criteria:

- **Application Type:** Requirements vary for logic, memory, power, or RF chips.
- **Electrical Characteristics:** Signal integrity, I/O density, and power handling.
- **Thermal Performance:** Heat dissipation and temperature management.
- **Form Factor:** Physical dimensions and integration needs.
- **Cost Considerations:** Balancing performance with economic feasibility.
- **Reliability:** Resistance to environmental stress, aging, and mechanical strain.

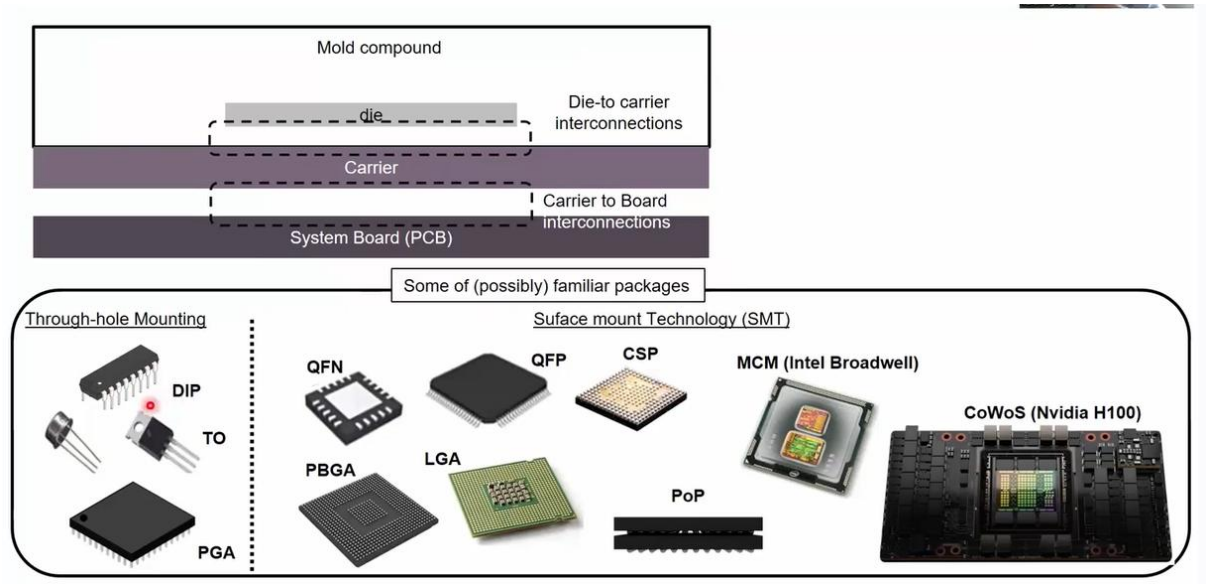
Typical Package Structure:

- **Die (Chip):** The core silicon component.
- **Substrate/Carrier:** Provides mechanical and electrical interfacing.

- **Interconnects:** Wires or bumps connecting the die to the substrate.
- **External I/Os:** Pins, balls, or lands that connect to the PCB.
- **Encapsulation:** A protective molding that seals the package.

Mounting Technologies:

- **Through-Hole:** Includes DIP, SIP, PGA.
- **Surface Mount:** Includes QFP, QFN, LGA, BGA.
- **Advanced Types:** PoP (Package-on-Package), MCM (Multi-Chip Module), SiP (System-in-Package), CoWoS (Chip-on-Wafer-on-Substrate).



1.3 Transition from Single-Chip to Multi-Chip Packaging

Packaging technologies continue to evolve based on system requirements:

By Integration Approach:

- **Conventional Packaging:** Performed after wafer dicing.
- **Wafer-Level Packaging:** Initiated while dies are still on the wafer.

By Substrate Type:

- **Lead frame-Based:** Used in simple packages like DIP, QFN.
- **Laminated Substrates:** Support complex routing (e.g., PBGA, Flip-Chip PBGA).
- **Advanced Substrates:** Enable high-performance multi-die systems using interposers.

These approaches are tailored to markets ranging from consumer electronics to high-performance computing (HPC).

1.4 Advanced Interconnect Technologies: RDLs and Interposers

Redistribution Layers (RDLs):

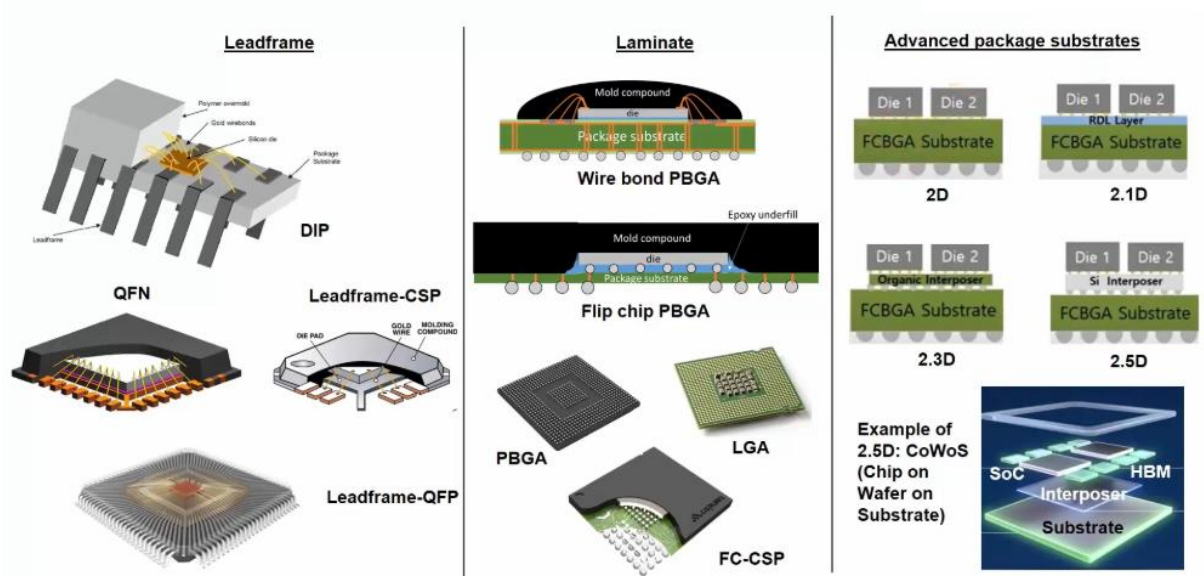
- Serve to reroute I/O pads on the die.
- Allow custom bump layouts and better I/O alignment.
- Common in FO-WLP (Fan-Out Wafer-Level Packaging), PLP (Panel-Level Packaging), and multi-die setups.

Interposers:

- Act as intermediate layers between the die and the substrate.
- Provide high-density signal routing and better thermal/electrical properties.
- Types include **silicon**, **organic**, and **glass**.
- Can be **passive** (routing only) or **active** (with integrated functionality).

2.5D and 3D Packaging:

- **2.5D Integration:** Multiple dies are placed side-by-side on an interposer.
- **3D Integration:** Dies are stacked vertically and connected through **Through-Silicon Vias (TSVs)**, enabling shorter interconnects and smaller footprints.



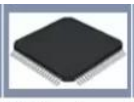
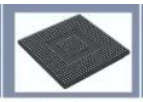
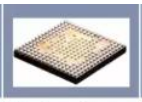
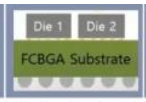
1.5 Comparative Analysis: Selecting the Right Packaging Solution

Evaluating packaging solutions involves balancing various factors:

- **Performance:** Electrical speed, power delivery, and signal integrity.
- **Cost:** Budget for both packaging and system-level integration.

- **Size Constraints:** Area and height limitations.
- **Thermal Efficiency:** Heat removal capability.
- **Reliability:** Long-term performance under mechanical and environmental stress.

The best choice depends on the application requirements, integration strategy, and overall system goals, often requiring trade-offs between performance, cost, and complexity.

IC package Type								
Pros	Low cost, easy to manually assemble, durable	Compact, good thermal performance, lightweight	Higher pin density, ease of inspection, ease of solderability	Higher pin count, good electrical and thermal performance	Reduced package size, higher electrical performance at lower cost	Higher level of integration, better performance, and power efficiency	Higher density I/O and routing at lower cost	high I/O throughput, hetero-geneous integration, lower latency
Cons	Bigger size, low pin count, incompatible with automated assembly	Testing accessibility, Reparability, smaller I/O pins than QFP	Pins susceptible to damage, difficult to repair bent pins	Difficult to inspect and rework, limited shelf life, costlier than QFN	Limited I/O pins, reliability issues (solder joint and warpage)	Longer die-to-die connections	Reliability issues in polymer RDL, lower I/O density than 2.5D	Costlier than 2.1D, reliability concerns
Common Application	Consumer electronics, industrial applications, legacy systems	Smartphone, tablets, automotive, telecommunications	Micro-controllers and micro-processors, ASICs	High performance ICs	Smartphones, IoT, wearable devices	Data centre chips, RF wireless modules, Space avionics	High performance computing segments	Data centre GPU for AI