Packaging Evolution: From Basics to 3D Integration

Module 4: Ensuring Package Reliability – Testing and Performance Evaluation

This module addresses the critical testing and quality assurance processes that ensure semiconductor packages function correctly and reliably under real-world and accelerated conditions.

4.1 Functional and Electrical Testing Overview

Testing is performed at various points along the semiconductor manufacturing pipeline to detect defects, verify performance, and classify components.

A. Foundry-Side Testing

• Wafer Probing:

- o Conducted on each die using a **probe station**.
- Electrical parameters such as I-V characteristics and leakage currents are measured.
- o Dies are binned based on performance and functionality before packaging.

B. OSAT-Side (Assembly & Test) Testing

• Assembly Open/Short Test (AOST):

- Checks for electrical shorts and opens in the package interconnects (wires, balls, leads).
- o Includes vision inspection and product grading (e.g., PGSRT).

• Burn-In Test:

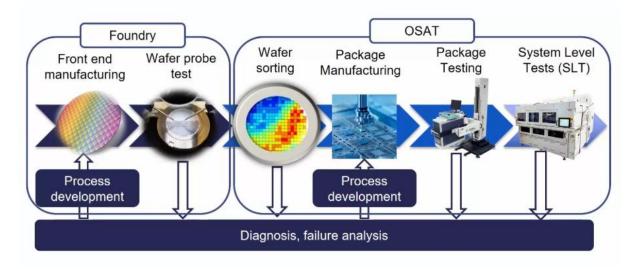
- o Devices operate at **elevated temperature and voltage** (e.g., 125°C, 1.2x nominal VDD).
- Used to detect infant mortality (early-life failures).

• Final Electrical Test:

- Performed on completed packages.
- o Includes:
 - Voltage margin testing
 - Functional and timing verification
 - Parametric measurements (e.g., drive strength, leakage)

C. System-Level Test (SLT)

- Mimics **end-user environment** by running actual **firmware or software** on the device.
- Captures **integration-level failures** and hard-to-detect bugs.
- Particularly important for complex SoCs or memory systems.



4.2 Reliability and Stress Testing

These tests simulate long-term operating and environmental stress to ensure robust field performance.

A. Assembly Open and Short Test (AOST)

- Identifies interconnect issues (missing, bridged, or damaged leads).
- Often automated with **vision inspection systems**.
- Provides **product grading** for classification.

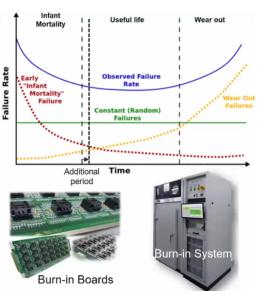


B. Burn-In Test

- Operates device under **high stress** to accelerate potential failures.
- Typical conditions: 125–150°C, high voltage, extended hours.
- Removes weak or marginal devices before customer delivery.

Objective: Testing of package components under elevated (stressful) conditions. temperature, voltage, and power cycling

- > The goal of Burn-in is to identify "Infant Mortality" failures before it reaches the customer.
- > Parts are loaded from trays onto Burn-in boards and then, into ovens (Burn-in system) during testing.
- ➤ Burn-in accelerates the failures by applying high voltage and high temperature stress.
- > The test is carried out long enough to catch the initial rate of failures and then to test slightly over the point where the curve flattens out.
- > Defects like dielectric & metallization failures, electromigration can be detected during burn-in.
- Although it removes the unreliable components with a high probability of early failure, the total life span of components is shortened with a burn-in test.



C. Final Test (FT)

- Ensures conformance to datasheet specifications.
- Conducted **post-packaging**, includes:
 - Voltage and current margin tests
 - Timing and frequency sweep tests
 - Functional and I/O tests
- Usually executed with Automated Test Equipment (ATE).

Objective: A temperature corner test to verify that the ATE (Electrical Testing Unit) with Handler (Placing DUT) packaged product meets the specifications > Parts are loaded into handler with temperature controlled test fixtures

- (not ovens) during testing.
- > Hot Test: Elevated temperatures according to product specifications. Parts are electrically tested at high temperatures to verify if the specifications are met.
- > Cold Test: Parts are subjected to low temperatures according to

product spec	incations and electrical	ily testeu.						
6 Specifications		LM741 C	LM741 OPAmp (TI) Datasheet					
6.1 Absolute Maxim over operating free-air temp	num Ratings perature range (unless otherwise noted)[1](2)(06			6.5 Electrical Char			
		MIN	MAX	UNIT	PARAMETER			
Supply voltage	LM741, LM741A		122		input offset voltage			
	LM741C		±18	· v				
Power dissipation (4)			500	mW	Input offset voltage adjustment range			
Differential input voltage			±30	V	adjustment range			
Input voltage (5)			±15	V	Input offset current			
Output short circuit duration		Continu	Continuous					
Operating temperature	LM741, LM741A	-50	125	°C	Input bias current			
	LM741C	0	70	-0	Input resistance			
	LM741 LM741A		150	7,0000	T Part Tourisher Sec			

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input offset voltage	R ₀ ≤ 10 kΩ	T _A = 25°C		1	5	mV
		TANN STASTAMAX			6	mV
Input offset voltage adjustment range	T _A = 25°C, V _S = ±20 V			±15		mV
Input offset current	T _A = 25°C			20	200	nA
	$T_{AMPN} \le T_A \le T_{AMMX}$			85	500	
Input bias current	T _A = 25°C			80	500	nA
	TAMEN S TA S TAMAX				1.5	μA
Input resistance	T _A = 25°C, V _S = ±20 V		0.3	2		MΩ
Input voltage range	$T_{AMPN} \le T_A \le T_{AMAX}$		±12	±13		٧
Large signal voltage gain	$V_8 = \pm 15 \text{ V}, V_0 = \pm 10 \text{ V}, R_L \ge 2 \text{ k}\Omega$	T _A = 25°C	50	200		V/m/V
		TARRES TA S TARRAX	25			
Output voltage swing	V _S = ±15 V	R _L ≥ 10 kΩ	±12	±14		- 62
		R _c ≥ 2 kΩ	±10	±13		٧

Summary Table: Test Methods Across Manufacturing Stages

Test Phase	Tool Used	Purpose		
Wafer Probing	Probe Station (ATE)	Die-level electrical		
water Frobing	Frode Station (ATE)	validation		
Assembly Open/Short Test	Vision + ATE	Interconnect integrity, defect		
Assembly Open/Short Test	VISIOII + AI E	detection		
Burn-In	Thermal Chambers	Early failure screening		
Final Test (FT)	Automated Testers	Full electrical verification		
System Level Test (SLT)	Towart Doords/Londows	End-use simulation &		
System-Level Test (SLT)	Target Boards/Loaders	validation		

Testing and reliability validation are essential for ensuring **functionality**, **robustness**, **and longevity** of semiconductor packages. These processes significantly reduce the risk of failure in the field and help maintain product quality standards across high-volume manufacturing.