# Packaging Evolution: From Basics to 3D Integration

## Module 2: From Silicon Wafer to Complete Package – Assembly and Fabrication Processes

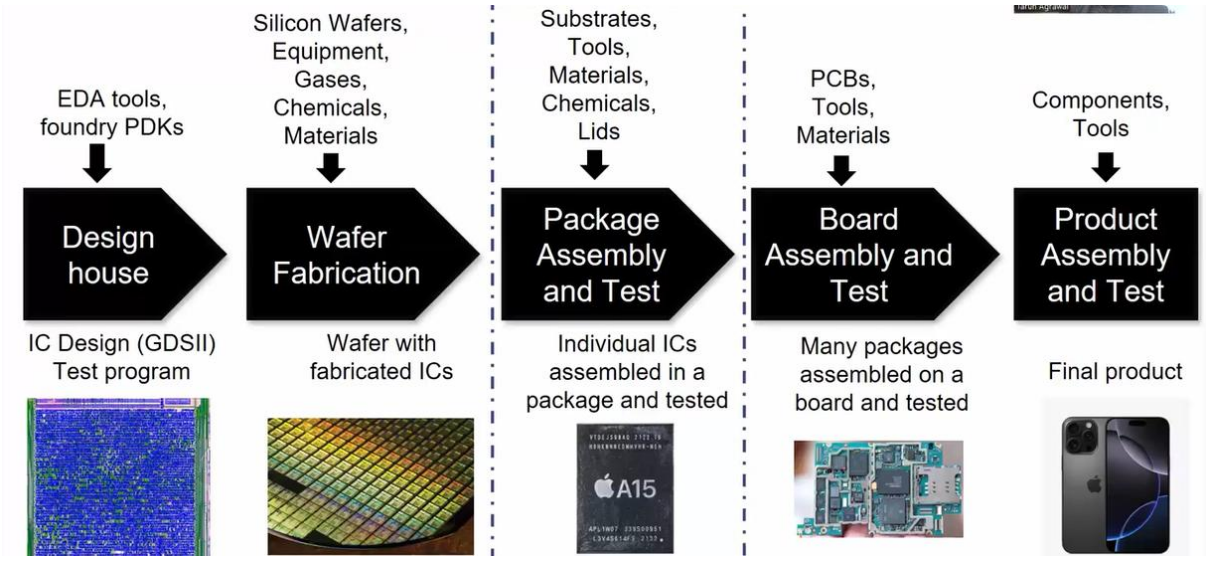
This module outlines the complete journey of semiconductor packaging, starting from wafer preparation through advanced assembly methods such as wire bonding, flip-chip, and wafer-level packaging.

### 2.1 Setting the Stage – Supply Chain and Assembly Facilities

The path from a chip design to a fully packaged integrated circuit involves several key players and steps:

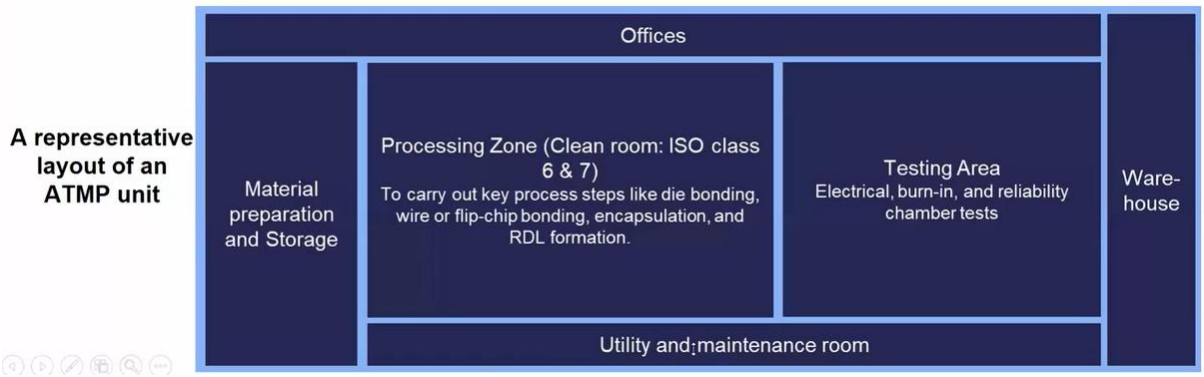
**Key Supply Chain Stages:**

- **Design House:** Engineers develop circuit layouts using EDA tools and licensed IP.
- **Foundry:** Manufactures the silicon wafer using photolithography, doping, and etching processes.
- **ATMP (Assembly, Test, Marking, and Packaging):** Dies are separated, assembled, encapsulated, and tested for performance and reliability.
- **Board Assembly:** Packaged chips are mounted onto printed circuit boards (PCBs).
- **System Integration:** End-user devices (e.g., smartphones, laptops, servers) are assembled with functional boards.



**Typical ATMP Facility Layout:**

- **Material Preparation:** Storage for wafers and supporting materials.
- **Cleanroom Assembly:** Controlled environment for critical processes like die bonding, wire bonding, and encapsulation.
- **Testing Labs:** Conduct electrical, reliability, and burn-in tests.
- **Logistics:** Warehousing and outbound shipment of finished ICs.

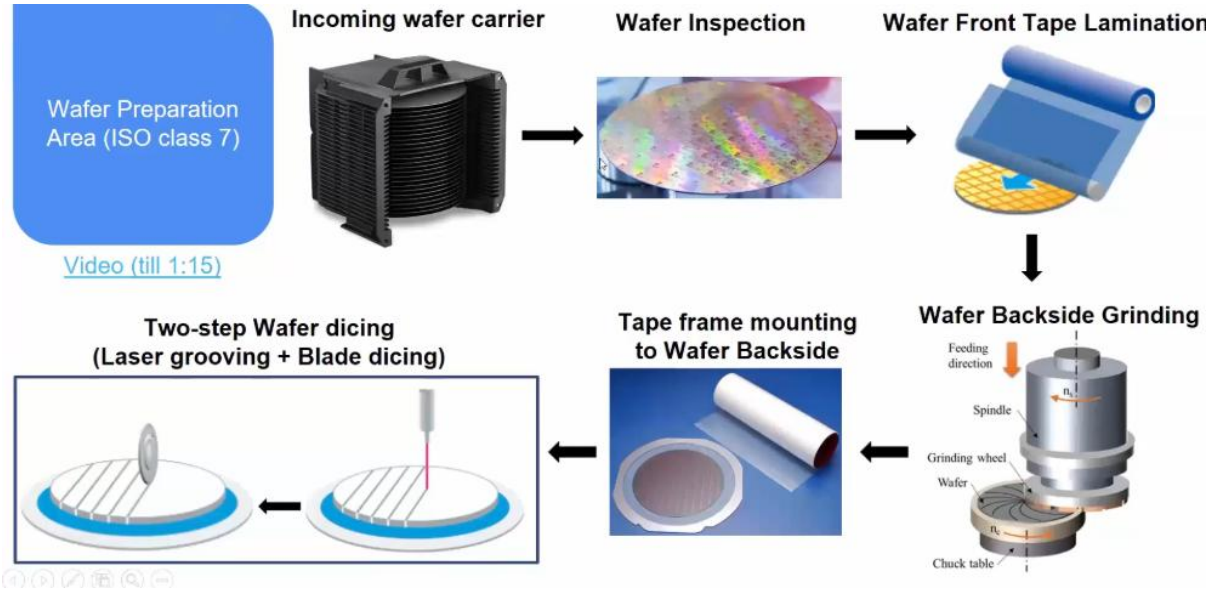



## 2.2 Wafer Pre-Preparation – Grinding and Dicing

Before packaging, wafers undergo several preparation steps to ensure manufacturability and performance:

**Wafer Preparation Process:**

- **Incoming Inspection:** Wafers are checked for mechanical or surface defects.
- **Protective Tape Lamination:** Applied to the wafer front to protect active regions during thinning.
- **Back Grinding:** Reduces wafer thickness for better thermal and structural characteristics.
- **Ring Frame Mounting:** Holds the wafer in place for stable processing.
- **Laser Grooving:** Defines scribe lines between dies for controlled breakage.
- **Blade Dicing:** Physically separates the wafer into individual chips.

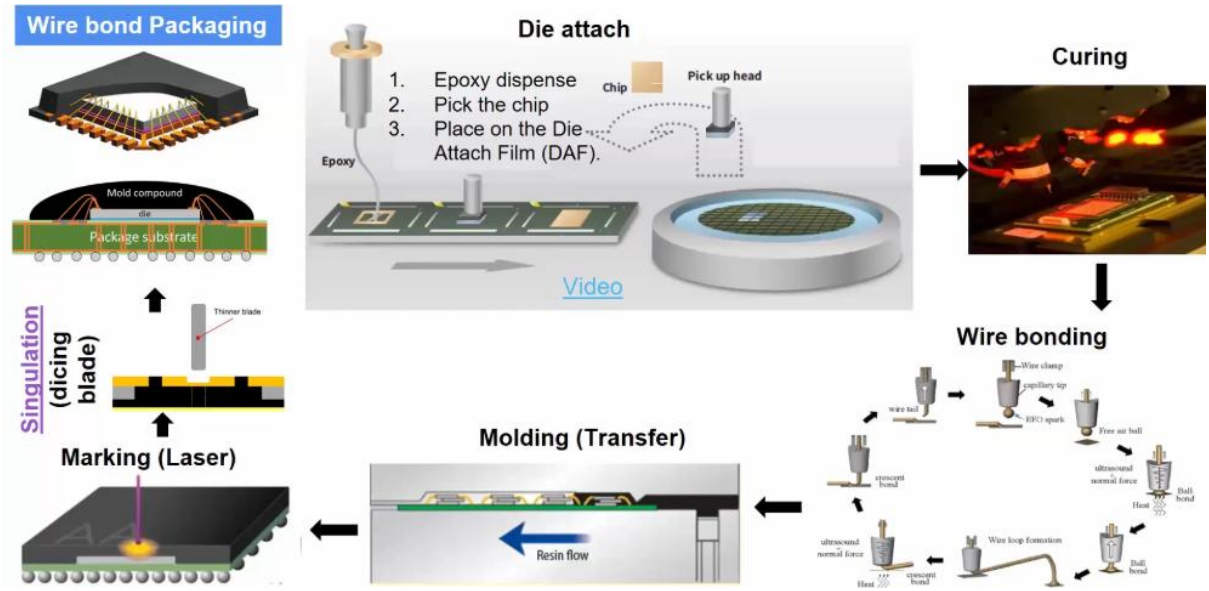



### 2.3 Wire Bond Packaging – Die Attach to Molding

Wire bonding is a mature and cost-effective packaging method used for many semiconductor devices:

**Wire Bonding Process Flow:**

- **Die Attach:** Die is mounted onto the substrate using conductive or non-conductive epoxy.
- **Epoxy Curing:** Ensures long-term mechanical and thermal stability.
- **Wire Bonding:** Fine gold or aluminium wires connect die bond pads to substrate or lead frame.
- **Encapsulation (Molding):** A protective epoxy compound seals the assembly from the environment.
- **Laser Marking:** Adds product identification and traceability information.
- **Final Singulation:** Individual packages are separated from the panel or lead frame strip.

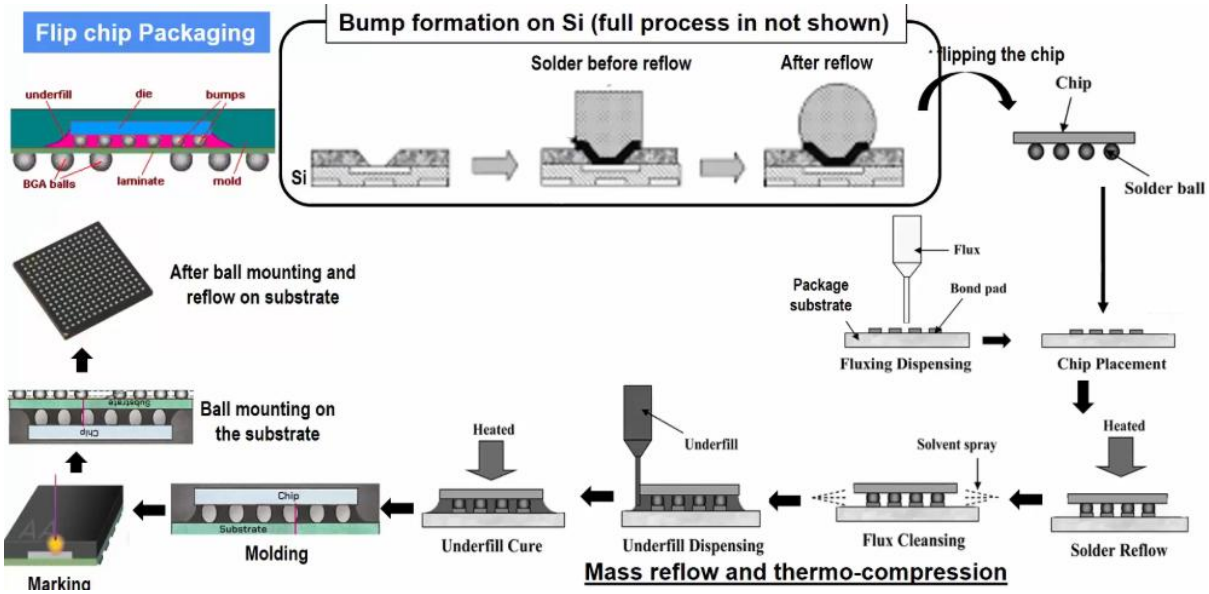



### 2.4 Flip-Chip Packaging – Bump Formation to Final Assembly

Flip-chip technology improves performance by offering shorter interconnect paths and higher I/O density:

**Flip-Chip Process Steps:**

- **Solder Bump Formation:** Tiny solder balls are formed on die pads.
- **Chip Placement:** The die is flipped face-down and aligned with the substrate.
- **Reflow Soldering:** Heat melts the bumps, creating strong electrical and mechanical joints.
- **Flux Removal:** Cleaning step eliminates residue to prevent corrosion or electrical failure.
- **Underfill Application:** Fills the gap between die and substrate for enhanced mechanical support and thermal performance.
- **Final Packaging:** Mold compound, marking, solder ball attach (for BGA), and final reflow complete the process.

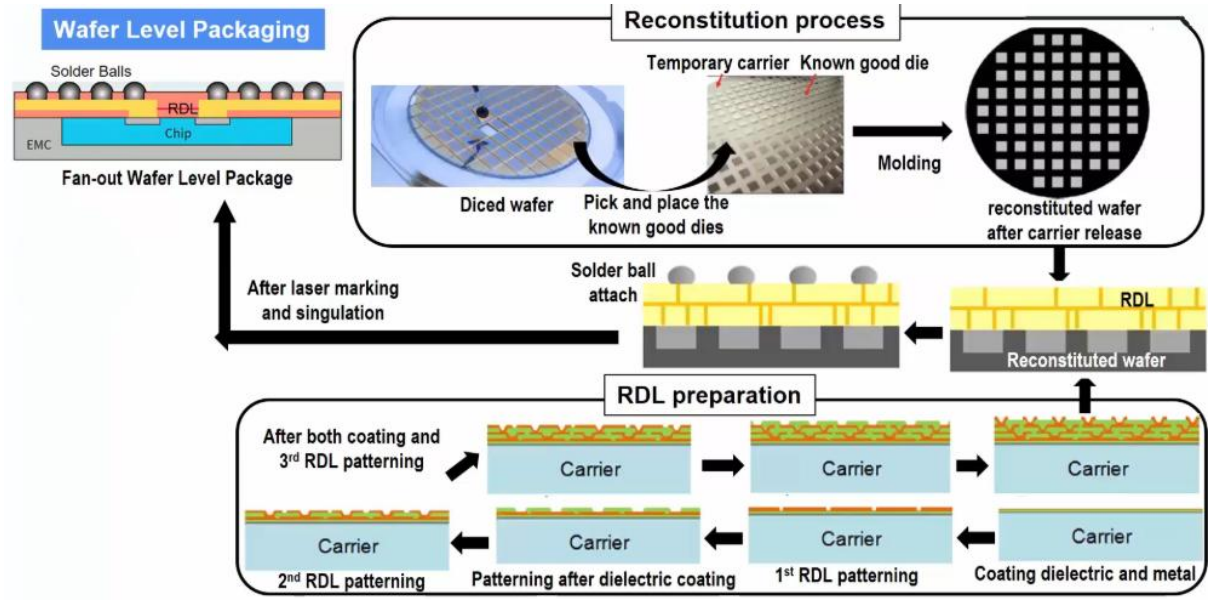



### 2.5 Wafer-Level Packaging (WLP) – Fully Integrated Wafer-Based Process

WLP integrates packaging directly at the wafer level, improving size, cost, and electrical performance.

**WLP Categories:**

- **Fan-In WLP:** Solder balls are confined within the die outline.
- **Fan-Out WLP (FO-WLP):** RDLs extend the I/O area beyond the die footprint.




**FO-WLP Process Flow:**

1. **Known Good Die (KGD) Selection:** Only tested, functional dies are used.

2. **Reconstitution:** Dies are embedded in an epoxy mold compound on a carrier wafer.
3. **RDL Formation:** Redistribution layers are patterned to fan out the die connections.
4. **Ball Attach:** Solder balls are mounted for board-level connectivity.
5. **Singulation:** The reconstituted wafer is diced into finished packages.