VERIFICATION TEST PLAN

Fundamentals Of Pre-Silicon Validation
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Project : ASYNCHRONOUS FIFO

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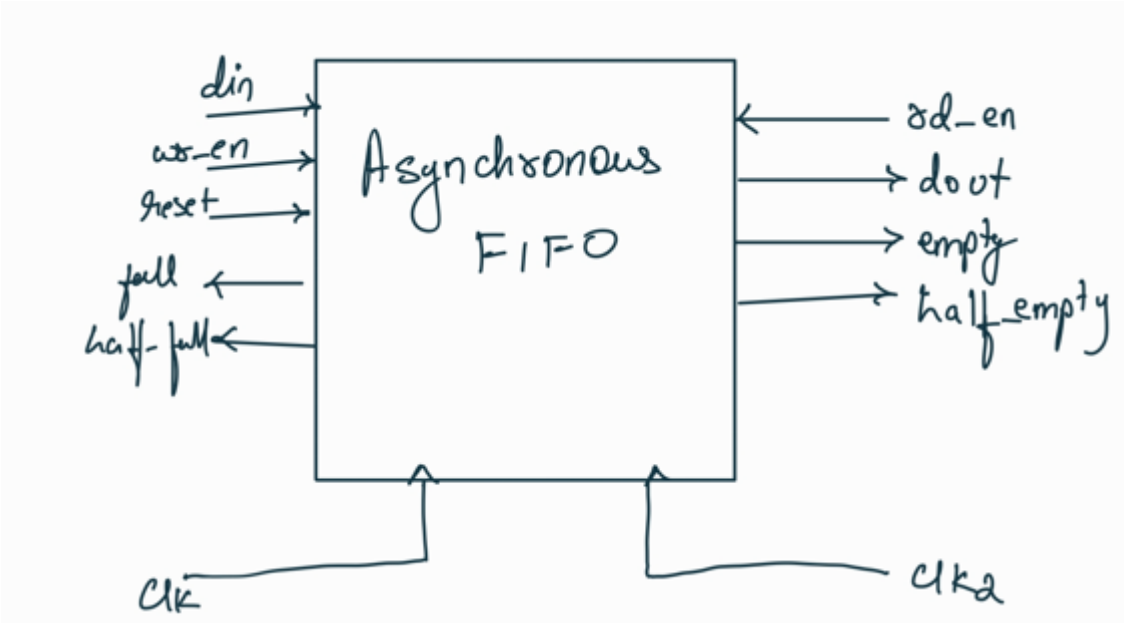
Introduction

1.1 Objective of The Verification Plan

The objective is to verify the functional correctness of the asynchronous FIFO design against the specification.

1.2 Top Level Block Diagram



1.3 Design Specifications

As per the group specifications specified our group is “J”

Sender Clock Frequency / Writing Frequency = 250Mhz.

Receiver Clock Frequency / Reading Frequency = 100Mhz.

Write Idle Cycles = 1.

Read Idle Cycles = 3.

Write Cycles:

The number of idle cycles between 2 successive writes is 1 which means after writing one data the next one is initiated after waiting for 1 clock cycle.

For every 2 clock cycles 1 data is written.

Time required to write one data item = 2 * 1/250Mhz = 2 * 4 nano sec.

Time required to write one data item = 8 nano seconds.

Read Cycles:

The number of idle cycles between 2 successive reads is 3 which means after reading one data the next one is initiated after waiting for 3 clock cycles.

For every 4 clock cycles 1 data is read.

Time required to read one data item = 4 * 1/100Mhz = 4 * 10 nano sec
Time required to read one data item = 40 nano seconds.
As per the given data the total burst of data is = 200.
So at a time the total number of writes that can be done is = 200.

Time taken to write all the 200 burst of data = 200 * 8 = 1600 nano seconds.

Total number of reads that can be done in 1600 nano seconds = 1600/40 = 40 reads.

Remaining data items to be read = 200 – 40 = 160.
The minimum depth of FIFO is = 160.
The depth of FIFO specified for the minimum requirements (i.e., 160) in this project is 256.

2.Verification Requirements

2.1 Verification Levels

2.1.1 We are verifying at the block level. This allows controllability and observability of all FIFO interfaces.

3. Required Tools

3.1 Software: QuestaSim, EDA Playground.
3.2 Hardware: Laptop/Desktop with good internet connection.

4 Risks and Dependencies

4.2 Mitigation plan will be Simulation strategies to cover timing margins.

5 Functions to be Verified

5.1 Functions from specification and implementation
5.1.1 To be verified: Read, write, empty/full flags, overflow/underflow.
5.1.2 Not verified: Performance, power, layout characteristics.
5.1.3 Critical for tapeout: Read/write functionality, empty/full flags.

6 Tests and Methods

TBD

7.Coverage Requirements

TBD

7.1 Assertions (TBD)

8 Resources Requirements

8.1 Team Members

- RTL DESIGN FIFO CALCULATION
- HLDS REPORT,VERIFICATION PLAN
- DESIGN & TB
- VERIFICATION

9 References Uses/Citations/Acknowledgements

- Simulation and Synthesis Techniques for Asynchronous FIFO Design.
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- Embedding Asynchronous FIFO Memory Blocks in Xilinx Virtex Series FPGAs Targeted for Critical Space System Applications.
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- Asynchronous FIFO Design with Gray code Pointer for High Speed AMBA AHB Compliant Memory controller.
- Crossing clock domains with an Asynchronous FIFO
- system on chip - Why do we use a gray encoded signal by 2 stage flip-flop in asynchronous FIFO to avoid race-condition issue? - Electrical Engineering Stack Exchange
- https://www.chipverify.com/verification/constraint-random-verification
- https://github.com/raysalemi/uvmprimer
- https://www.youtube.com/@theuvmprimer4123/playlists