Chittagong University of Engineering And Technology

Department of Electrical And Electronic Engineering

NAME OF THE EXPERIMENT/REPORT

Project Report

COURSE NO. : EEE-366

COURSE TITLE : Digital Electronics Sessional

REMARKS

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STUDENT ID : 1702009

LEVEL : 3

TERM : 2

SECTION : A

GROUP : A1

Task-1:-Use 4 bit Synchronous Up/Down Counter with Load and Reset.

Simulation Outputs:-

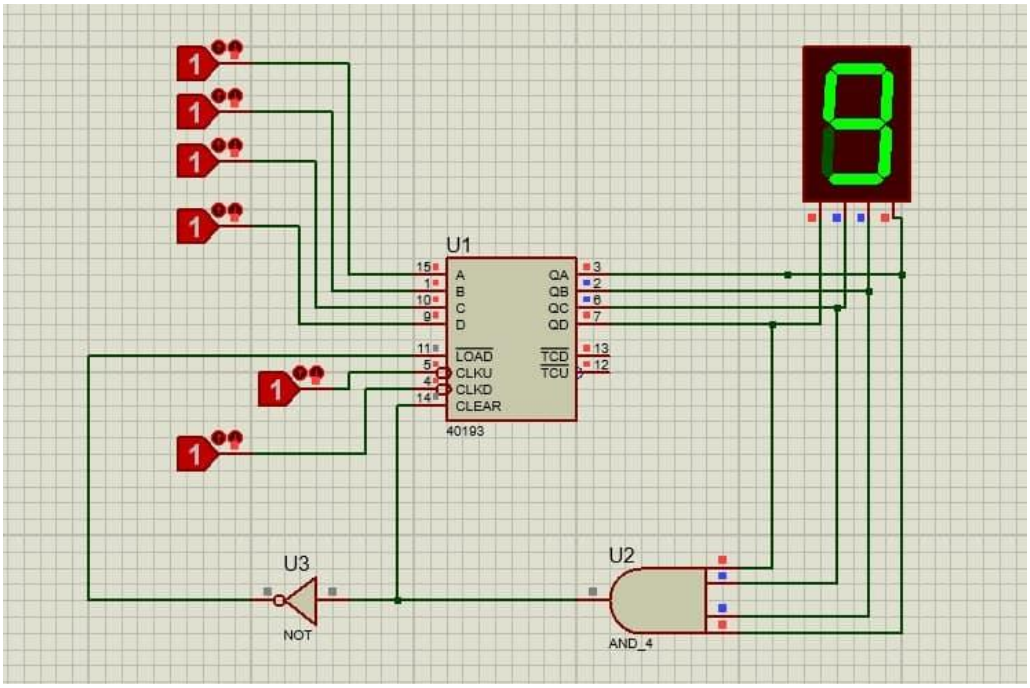

Fig.1(a)

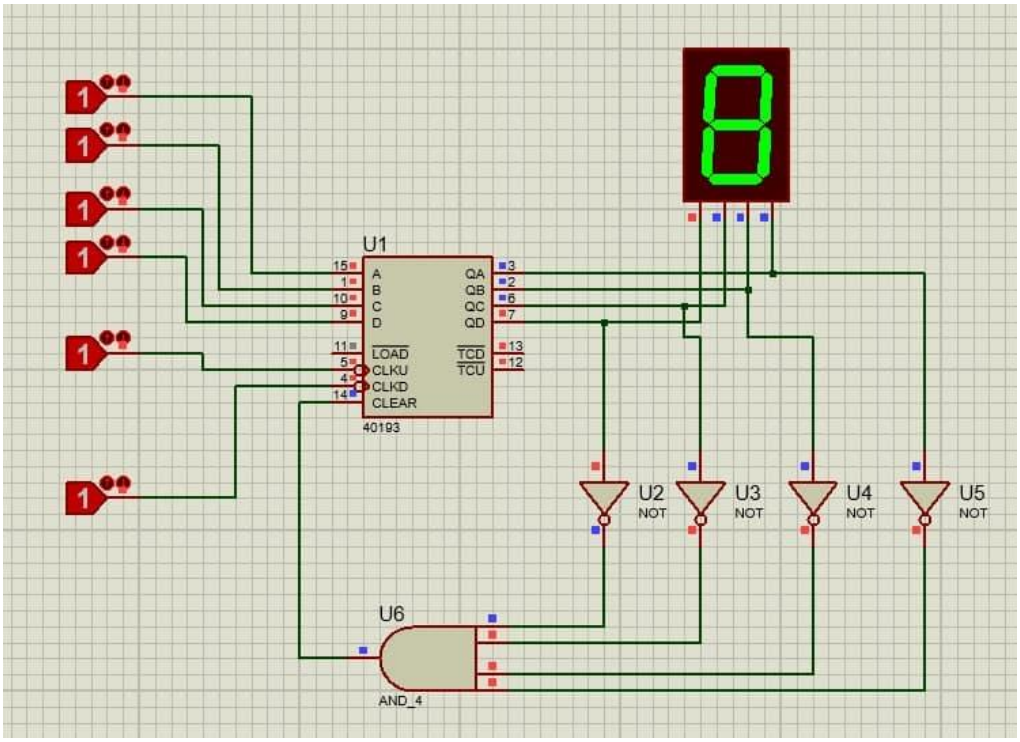

Fig.1(b)

Fig.1. (a and b)Represents synchronous up/down counter(top figure(1(a)) representing up counter and bottom figure(1(b)) representing down counter). As it is a 4 bit counter,

it will show output from 0 to 15.In up counter it will counts 0,1,2,3....15 and in down counter 15,14, 13,....2,1,0. Here 40193 ic counter is used. Here,A,B,C,D is the input and QA,QB,QC,QD is the output.here is a clock up pin and clock down pin and there is a pin for load and clear.if clear pin is 1, LCD display will clear it's screen. The segment display is connected with 3,2,6,7 pins of the IC.At 4 and 5 pins,two clock signal is applied.here, there is some difference between up and down counter.In up counter,there is a input in the load pin of the ic followed by a not gate but in the down counter there is nothing such that.

Task-2

2. You will design 2 counter.
   i. First one will count like the following sequence
   ii. Second one will count in reverse direction

Last Digit of ID	Counting Sequence
0	0,3,4,5,0,3,4,5……..
1	0,1,4,5,6,0,1,4,5,6……..
2	0,1,2,5,6,7,0,1,2,5,6,7……
3	0,1,2,3,6,7,8,0,1,2,3,6,7,8…….
4	……
5	……
6	……
7	……
8	……
9	0,1,2,3,4,5,6,7,8,9,12,13,14, 0,1,2,3,4,5,6,7,8,9,12,13,14,

Simulation Outputs:-

2(I)

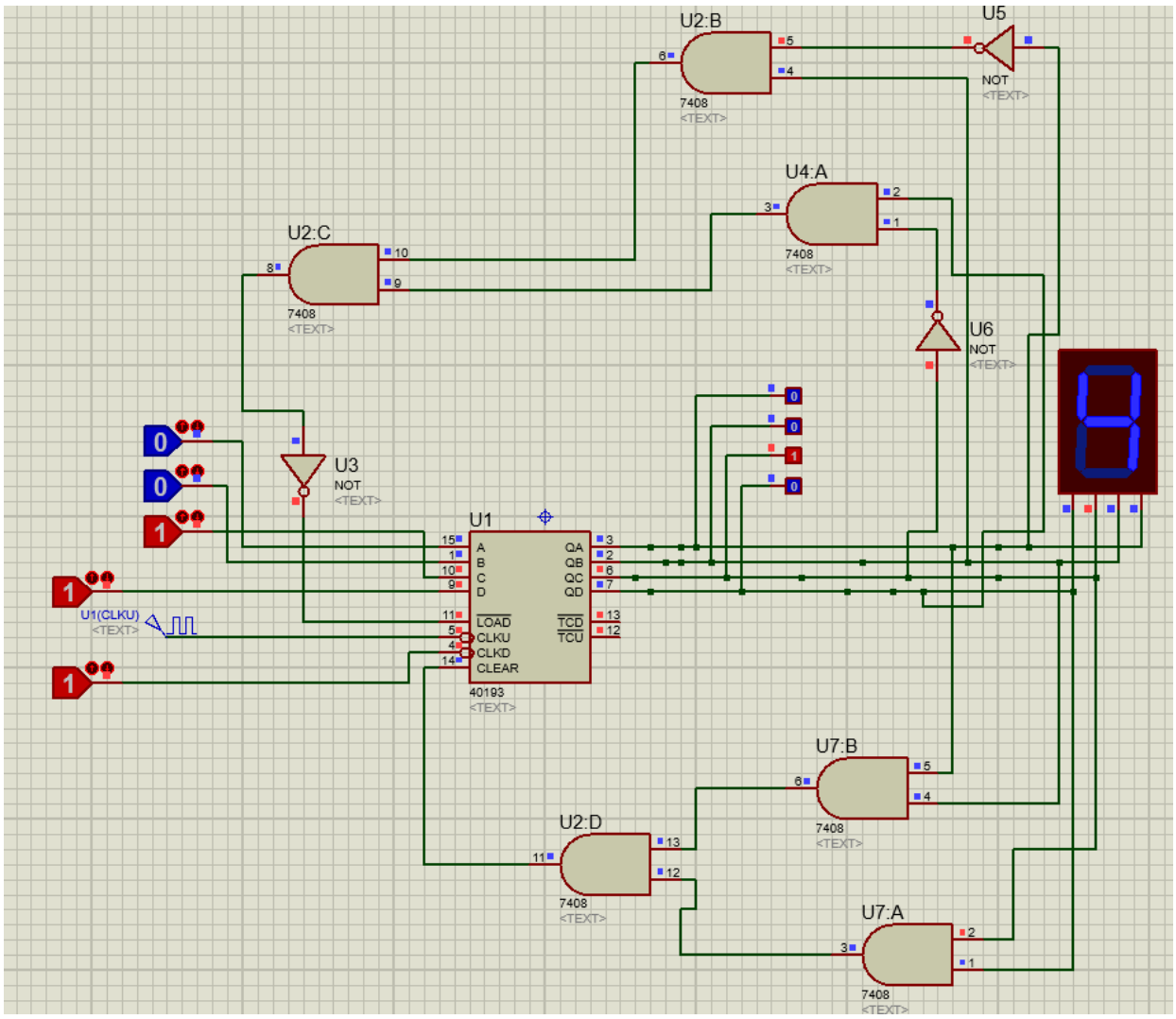

Fig.2 represents the circuit diagram for a counter that counts in the sequence of 0,1,2,3,4,5,6, 7,8, 9,12,13,14,0,1...here,in the counter, 10 is skipped and from 12 it is incremented again.So,for this the binary of 10 or 1010 or A_bar,B,C_bar,D logic function is implemented and its output is appied to the load pin by a nor gate.So,load pin will be activated when it will get the input of 0, then the output of segment display will show that is in the input/1100/12, from this it will be counted again from 12. After 14, the counter will show again 0,it will not show 15. So,for this, the clear pin should be 1, for this the binary of 15 that is ABCD logic function is applied and it is applied to the clear pin.So,after reaching 15, the screen gets clear and count again from 0.

2(II)

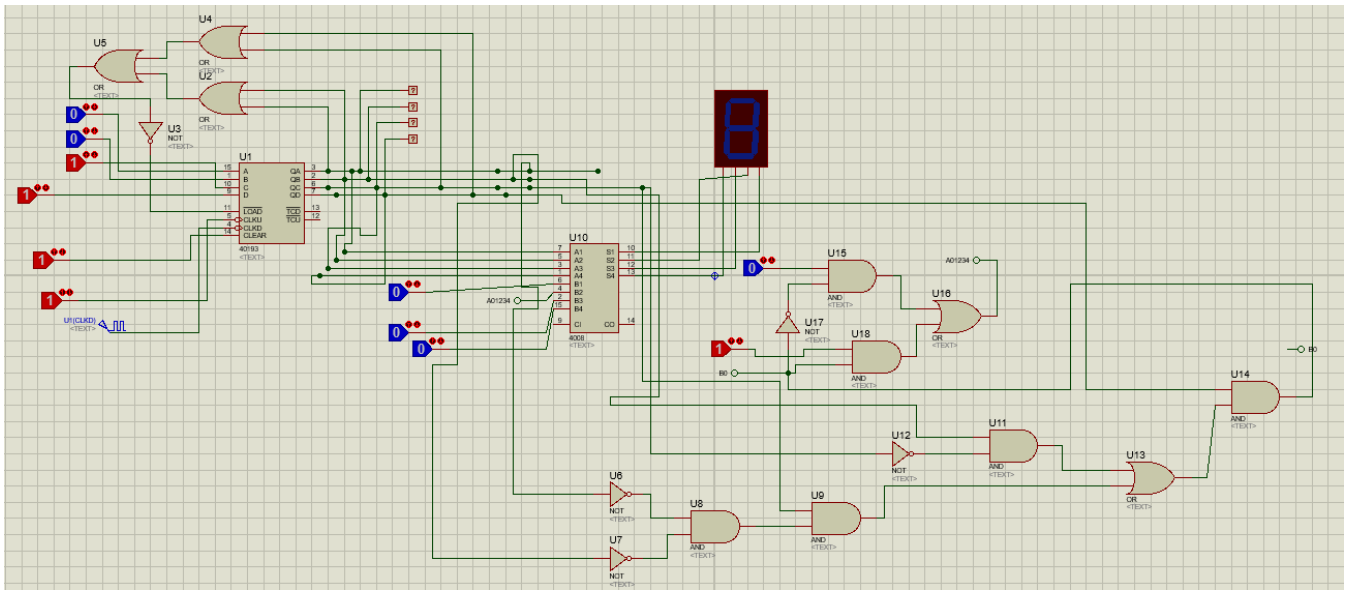

Fig.3 represents the circuit diagram for a counter that counts in the reverse sequence of 0,1,2,3,4,5,6, 7,8, 9,12,13,14,0,1…. Here,in A,B,C,D pins, 4 inputs is applied.Here,4008 IC adder circuit and 40193 IC of counter circuit is used. The seven segment display is connected in the 10, 11,12, 13 pins of 4008 IC.