Chittagong University of Engineering And Technology

Department of Electrical And Electronic Engineering

NAME OF THE EXPERIMENT/REPORT

Study of D and T Flip Flop by NAND and NOR gate,Construction of 4-bit counter with clear and reset option, Study of shift register in all its modes.

COURSE NO. : EEE-366

COURSE TITLE : Digital Electronics Sessional.

EXPERIMENT NO : 11,12,13

DATE OF EXPERIMENT : 27.12.21

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REMARKS

NAME : Amith Deb Nath

STUDENT ID : 1702009

LEVEL : 3

TERM : 2

SECTION : A

GROUP : A1

Experiment No.:-11

Objectives: The objectives of this experiment is to study the different types of Flip-Flops.

Task 1:Study of D and T Flip Flop by NAND and NOR gate.

Simulation Outputs:-

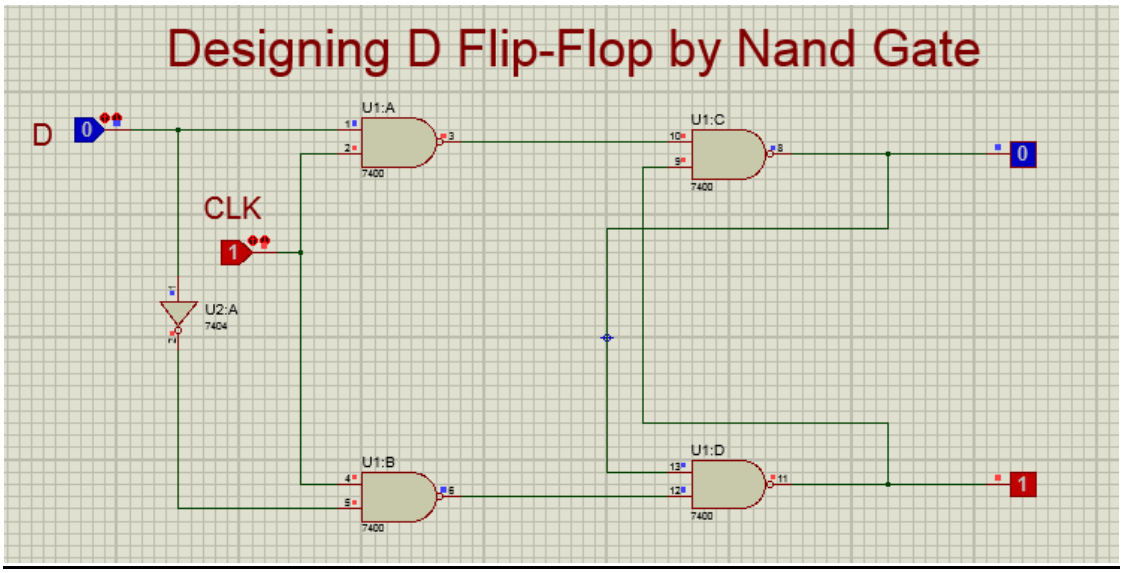

Fig.1. represents a D Flip-flop designing by Nand Gate. When Clock pulses in 1, the outcome is shown in the image above. By changing the value of input D when the clock pulse is 1, the output values change from their previously stored value. In this scenario, changing the value of D causes the Flip-output Flop's to change. When the ClOCK pulse is 0, however, the output does not change regardless of the value of D. It serves as a latch in this scenario.

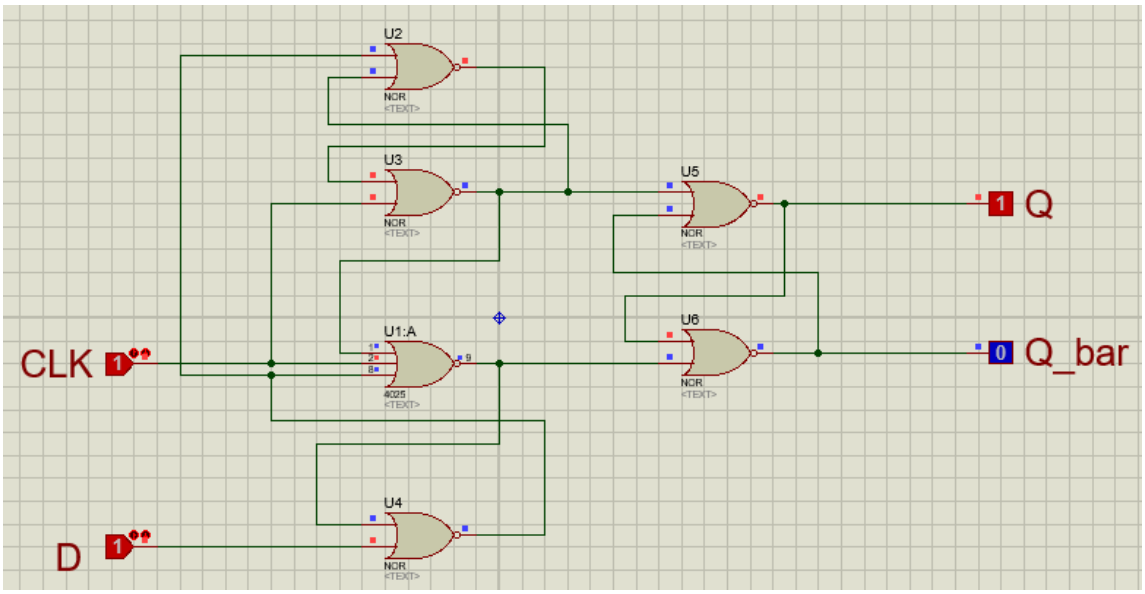

Fig.2. represents the D Flip Flop designing by NOR Gate.In this case,the output is as same as the D Flip Flop designing by NAND Gate. When Clock pulses in 1, the outcome is shown in the

image above. By changing the value of input D when the clock pulse is 1, the output values change from their previously stored value. In this scenario, changing the value of D causes the Flip-output Flop's to change. When the ClOCK pulse is 0, however, the output does not change regardless of the value of D.

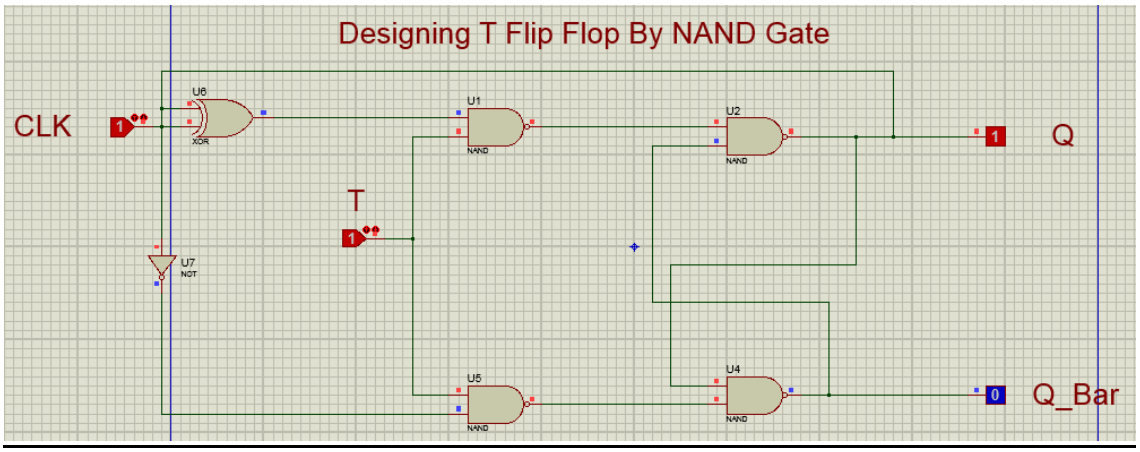

Fig.3. represents T flip-flop designing by NAND Gate. The input Toggle value is indicated by T. When the clock is set to 1, the output Q and Q Bar are pulsed by altering the value of T,then the output value toggles from its previous value. When clock is set to 0, however, adjusting the Toggle input has no effect on the output.

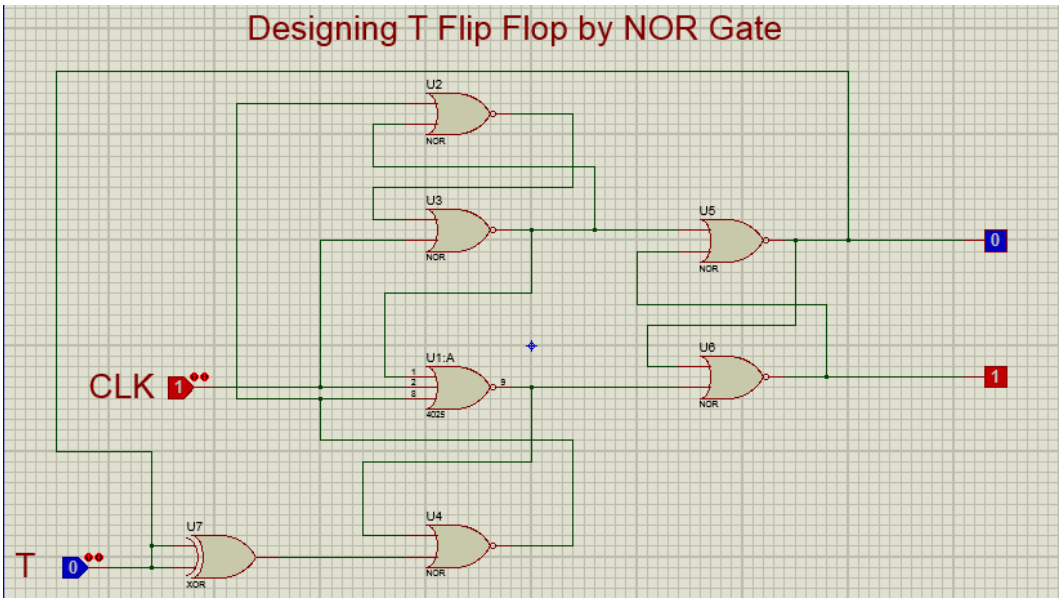

Fig.4. represents the T Flip Flop designing by NOR Gate.here,also the principle is same as T flip flop by NAND gate. The input Toggle value is indicated by T. When the clock is set to 1, the output Q and Q Bar are pulsed by altering the value of T,then the output value toggles from its previous value. When clock is set to 0, however, adjusting the Toggle input has no effect on the output.

Experiment No.:-12

Objectives: The objectives of this experiment is to construction and verification of 4 bit ripple counter.

Task 2. Construction of 4-bit counter with clear and reset option

Simulation Outputs:-

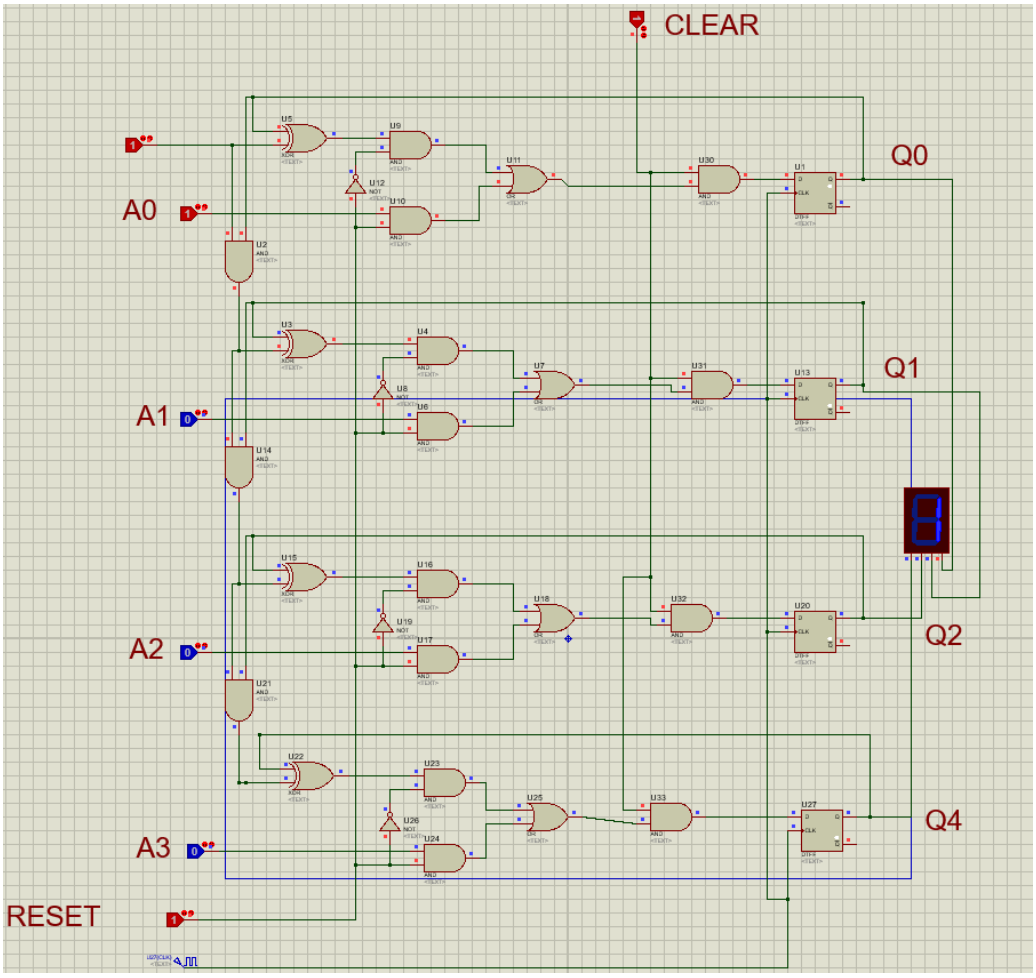

Fig.5. represents a four-bit up-counter and a & segment BCD counter. This circuit counts from 0 to 1 in the following order: 0, 1, 2,..., 0, 1, and so on. The flip-flop outputs Q3, Q2, Q1, Q0, and Q0 represent the count. Counting with an initial count of 0 is sometimes essential. Using the ability to clear the flip-flops, this state can be obtained. However, starting with a different count is occasionally advantageous. A counter circuit must have some inputs that may be used to load the initial count in order for this form of operation to work. It's possible to achieve this by using the Clear and Preset inputs. To enable parallel-load capability, the circuit in Fig. 1 is modified. When the preset pin is enabled, the counts start from 1. Prior to each D input, a two-input multiplexer is used.The standard counting procedure is performed using one input

to the multiplexer. A data bit can be directly placed into the flip-flop as the other input. The mode of operation is selected using a control input called Preset. When reset = 0 the circuit counts. When reset = 1, the counter is reset with a fresh initial value. A and gate is added before each Flip-flip to clean the circuit. The previous multiplexer output is connected to one pin of the and gate, while the other pin is used to supply clear command.

Experiment No.:-13

Objectives: The objectives of this experiment is to construct a)Serial in Serial Out b)Serial in Parallel Out c)Parallel in Parallel Out d)Parallel in serial Out.

Task 3:Study of shift register in all its modes

Simulation Outputs:-

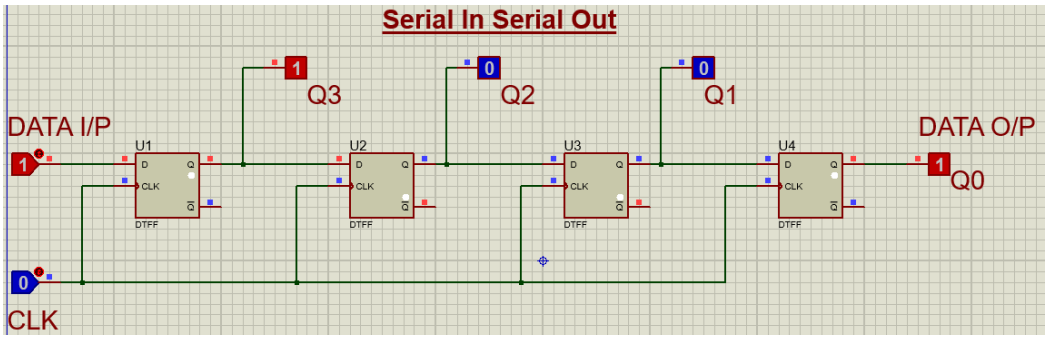

Fig.6. represents Serial In. Serial Out register. The input data is set to 1001 in this case. When the clock is triggered, the first register receives 1 bit. The next bit is a zero. The next bit is then 0. Last but not least, bit 1 was inserted into the register. As a result, the output is 1001.

TABLE I. Truth table of SISO

CLK	Serial In	Q3	Q2	Q1	Q0	Serial Out
1	1	1	0	0	0	1
2	0	0	1	0	0	0
3	0	0	0	1	0	0
4	1	1	0	0	1	1

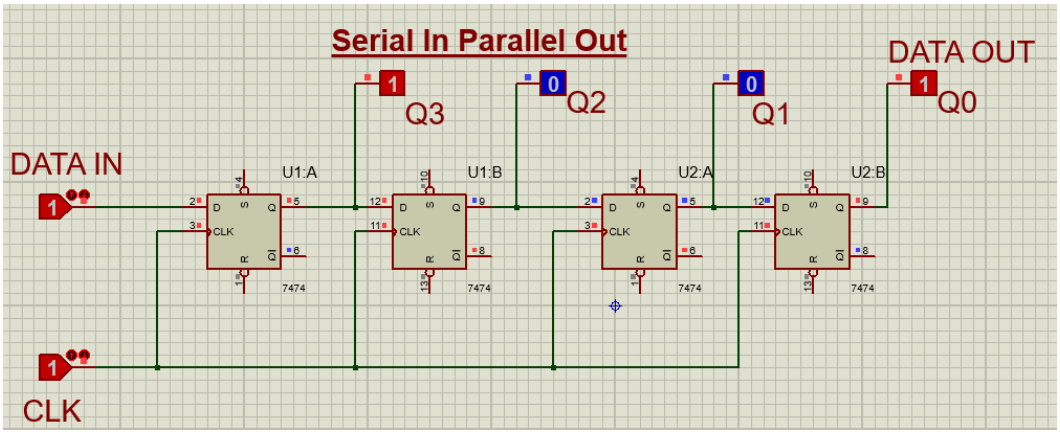

Fig.7. represents Serial In Parallel Out register. Here, the input data is chosen as 1001. When the clock is triggered, at first 1 bit goes to the first register. Next bit is 0. Then the upcoming bit is 0. Finally, last bit 1 entered to the register. So, the output is 1001.

TABLE II. Truth table of SIPO

CLK	Serial In	Q3	Q2	Q1	Q0	Parallel Out
1	1	1	0	0	0	1
2	0	0	1	0	0	0
3	0	0	0	1	0	0
4	1	1	0	0	1	1

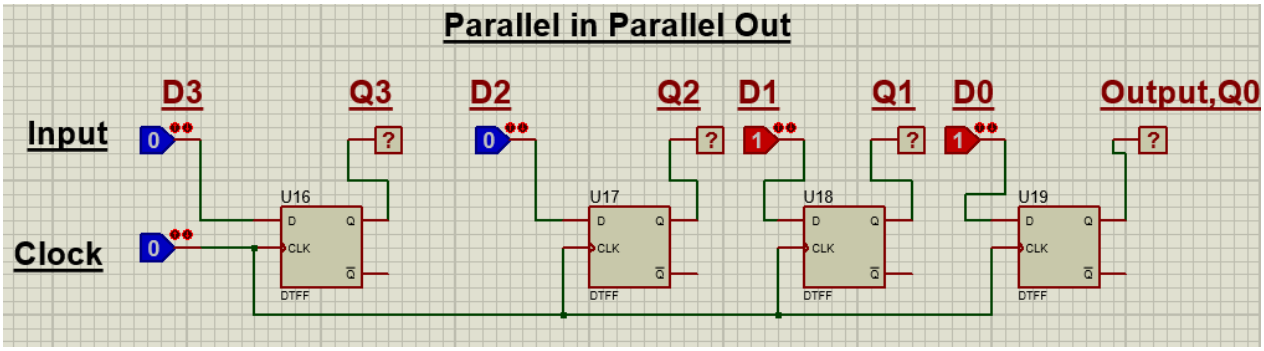

Fig.8. represents Parallel In Parallel Out shift register which are storage devices in which both data loading and data retrieval activities take place at the same time. This diagram depicts a PIPO register that can store an n-bit input data word (Data in). At the point of the first clock pulse, each flip-flop stores an individual bit of the data in appearing as its input (U19 stores B1 appearing at D0; U18 stores B2 appearing at D1... Un stores Bn appearing at Dn). Furthermore, the bit stored in each individual flip flop appears at its appropriate output pins at the same time (Q1 = D1; Q2 = D2... Qn = Bn). This means that in a single clock pulse, both data storage and data recovery occur..

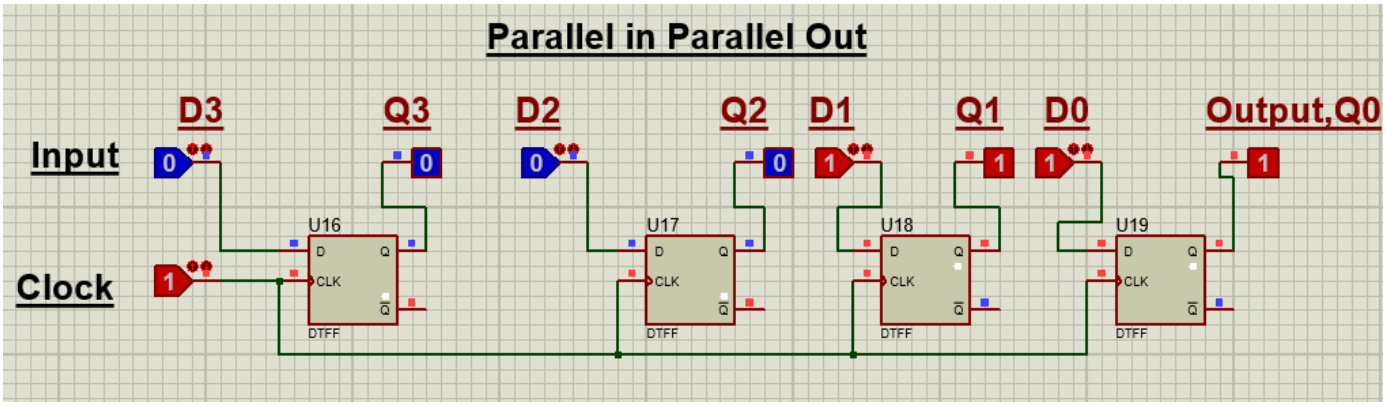

Fig.9. represents the actual working condition of PIPO register. When the clock pulse get positive triggered which means it goes to 1 from 0,then the input data stream parallelly loaded as the output data byte at the same time.

TABLE III. Truth Table for PIPO register

CLK	Data Input				Output			
	D0	D1	D2	D3	Q0	Q1	Q2	Q3
1	1	0	0	1	1	0	0	1
2	1	0	1	0	1	0	1	0

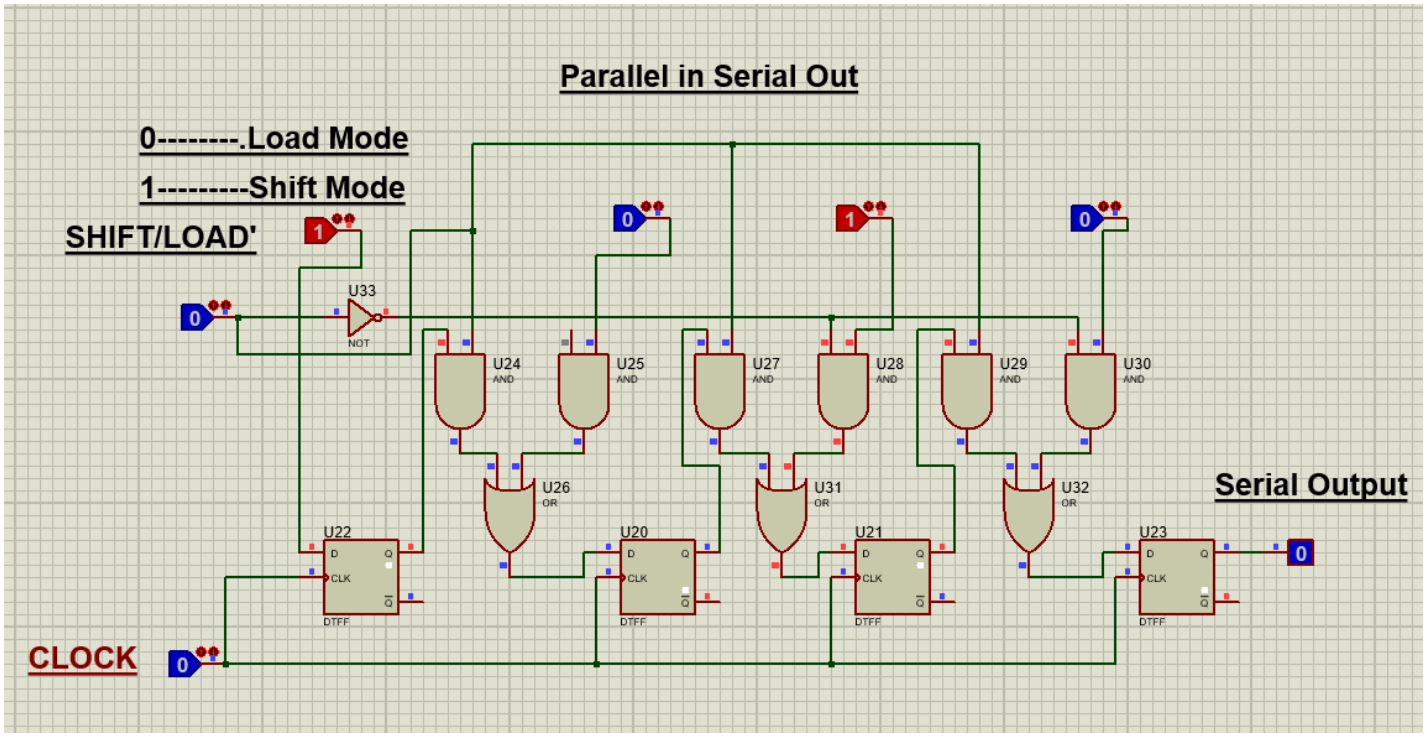

Fig.10. represents the Parallel in Serial out register, The data is entered in concurrently, and the results are sent serially. This is a four-bit Parallel in Serial out register. The previous Flip Flop's output is the flip flop's input. The combinational circuit connects the input and output signals. The binary inputs B0, B1, B2, and B3 are routed through this combinational circuit. The two modes in which the PISO circuit operates are shift mode and load mode. The load mode is represented by this Figure, which indicates the pin is active low when in load mode.

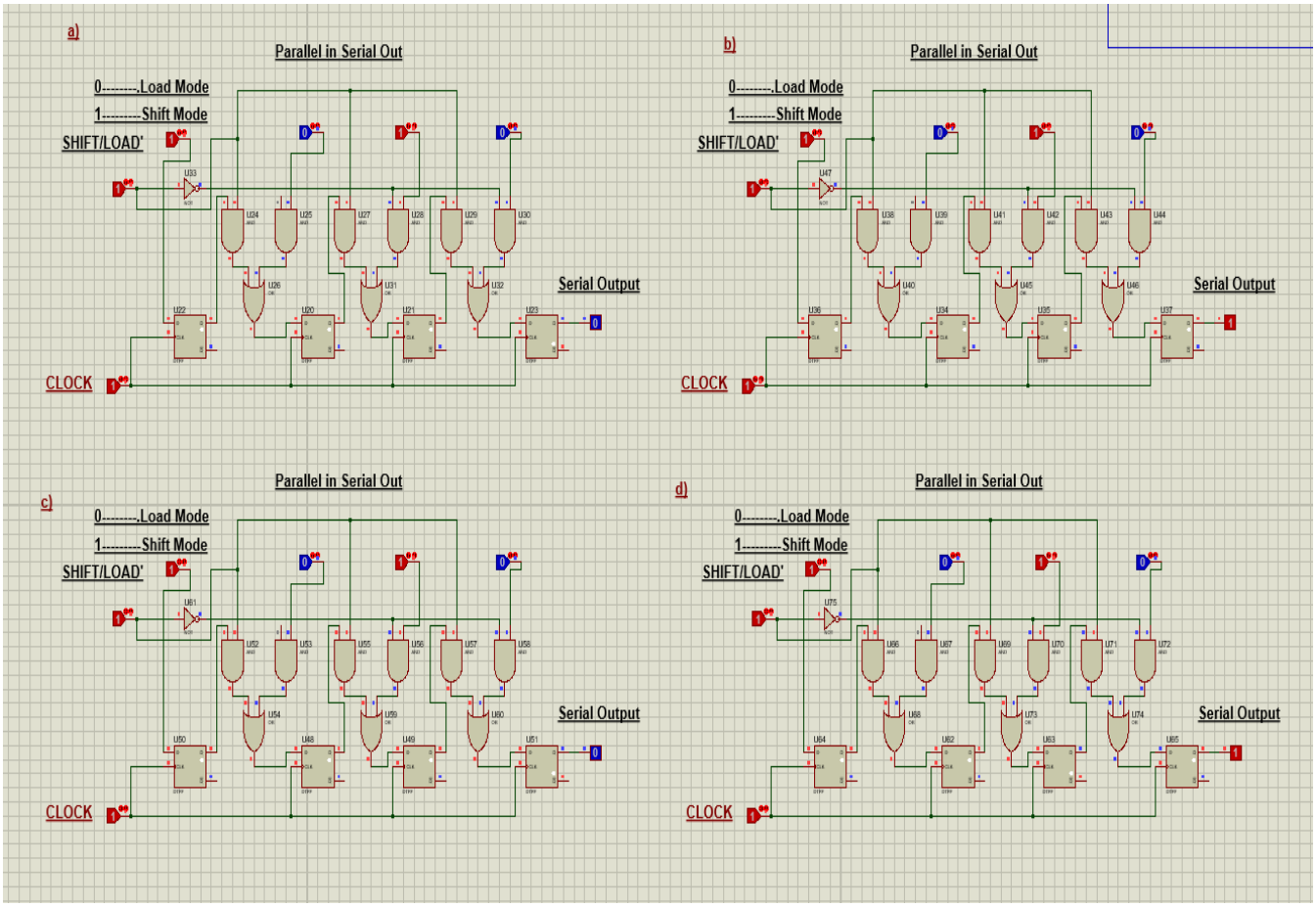

Fig.11. represents parallel to serial data loading from the given data stream with the changing phase of clock pulse. Here, our 4-bit data stream is 1010 which has been given as the input data bits. When the clock pulse changes its phase from 0 to 1 with the shift mode, output is serially loaded in the output terminal which is our desired operation.

TABLE IV. Truth Table for PISO shift register

CLK	Q3	Q2	Q1	Q0	Output
0	1	0	0	1	1
1	0	0	0	0	0
2	0	0	0	0	0
3	0	0	0	0	0

DISCUSSIONS:- In this experiment,a D flip flop is designed by nand gate and also it is designed by only nor gate.Similarly,a T flip flop is designed by nand and nor gate only.Then,a 4 bit counter with clear and reset option is designed. Then,Different types of register, serial in serial out,serial in parallel out,parallel in parallel out,parallel in serial out are designed.