Chittagong University of Engineering And Technology

Department of Electrical And Electronic Engineering

NAME OF THE EXPERIMENT/REPORT

Design and implementation of magnitude comparators using logic gates(4 tasks);Design and implementation of multiplexer(3 tasks)

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REMARKS

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LEVEL : 3

TERM : 2

SECTION : A

GROUP : A1

Experiment No.:-8

Task-1:- Design of four bit magnitude comparator using logic gates

Simulation outputs:-

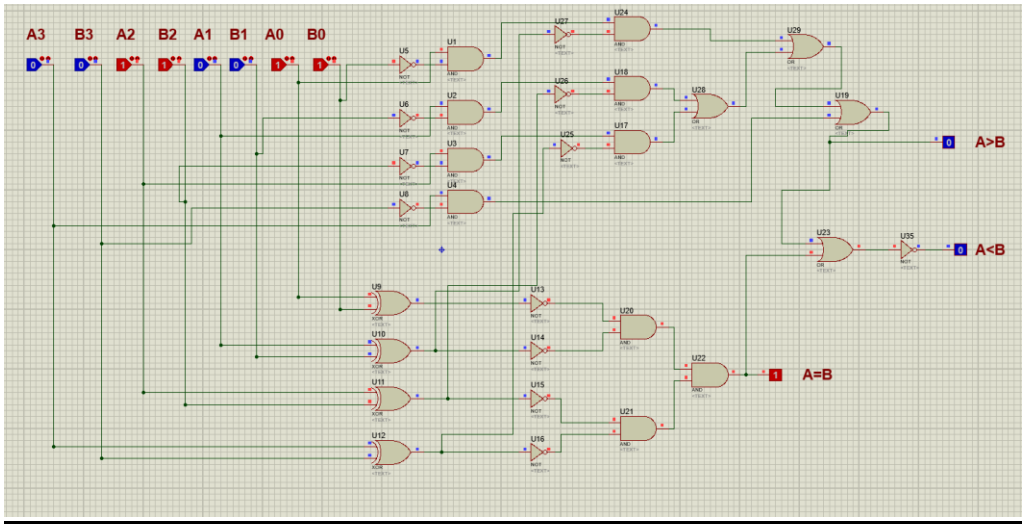

Fig.1. represents a 4 bit magnitude comparator(A=B case). Here , two input A and B is taken. By this circuit, we have to check whether A is equal to B or not. By using a XOR,NOT,AND gates, the comparator for checking A=B is made. For output checking, A is set to 0101 ,B is set to 0101. Then, the output of A=B is observed as 1 that is by this comparator circuit two 4 bit input variable can be checked whether it is equal or not.

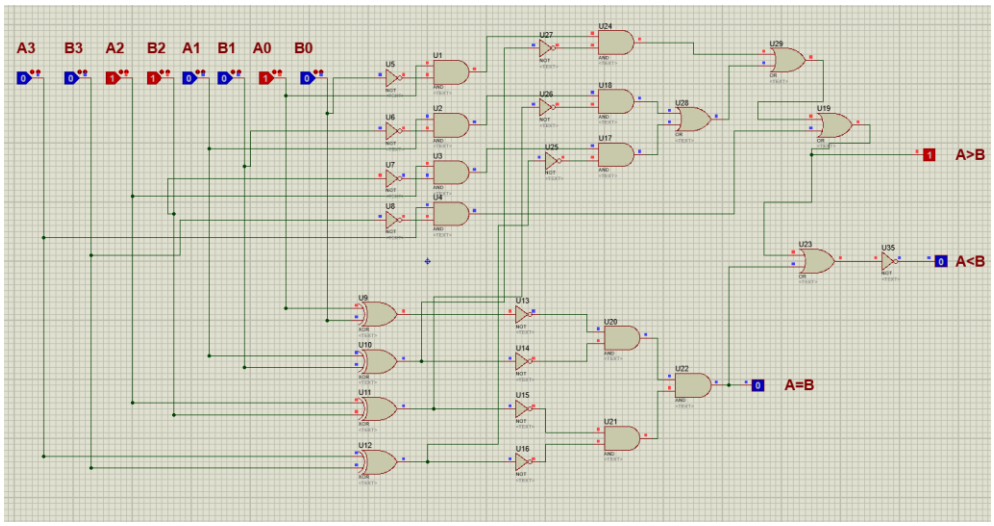

Fig.2. represents a 4 bit magnitude comparator(A>B case). Here , two input A and B is taken. By this circuit, we have to check whether A is greater than B or not. By using OR,NOT,AND gates the comparator for checking A>B is made. For output checking, A is set to 0101 ,B is set to 0100. Then, the output of A>B is observed as 1 that is by this comparator circuit two 4 bit input variable can be checked whether A is greater than B or not.

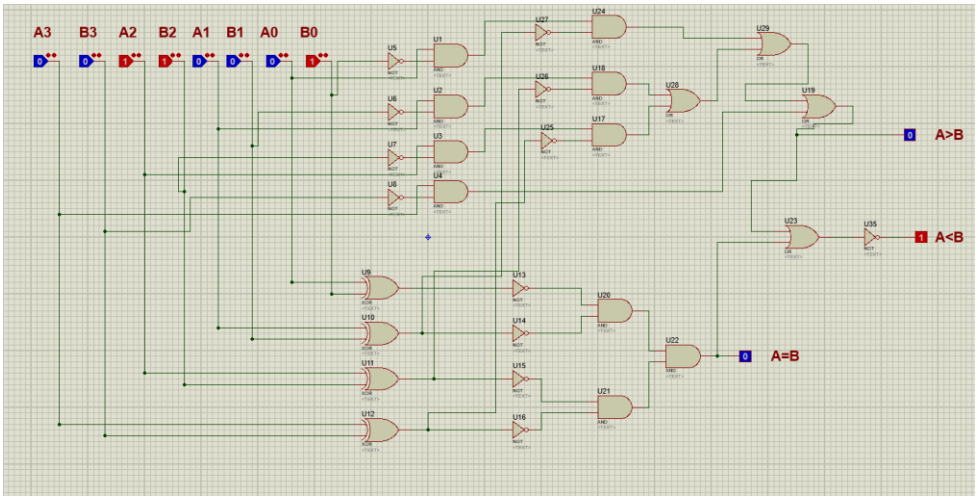

Fig.3. represents a 4 bit magnitude comparator(A<B case). Here , two input A and B is taken. By this circuit, we have to check whether A is smaller than B or not. By combining two circuits of (A=B) and (A>B) the comparator for checking A>B is made. For output checking, A is set to 0100 ,B is set to 0101. Then, the output of A<B is observed as 1 that is by this comparator circuit two 4 bit input variable can be checked whether A is smaller than B or not.

Task-2:- Parity Bit Checker

Simulation outputs:-

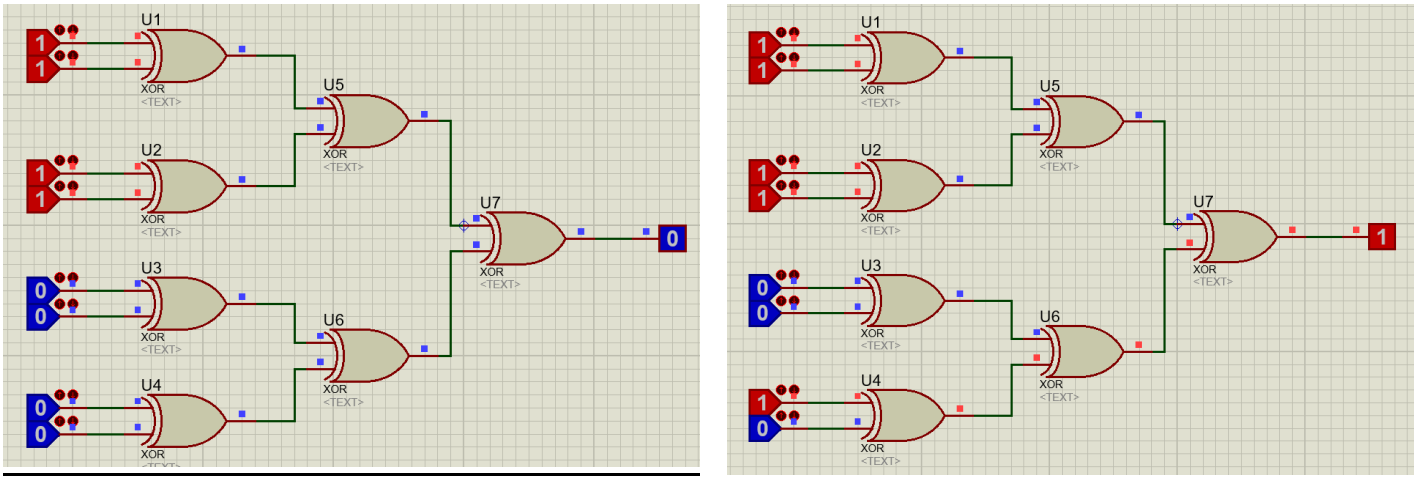

Fig.4. represents a parity bit checker circuit. Here ,the circuit is completely made by X-OR gate only. In the case of X-or gate, if there is even number of input 1, then the output is 0.whether if there is odd number of input 1, then the output is 1.Truth table of Xor is given below:-

A	B	XOR
0	0	0
0	1	1
1	0	1
1	1	0

So,in the figure 4, in the left circuit ,as there is even number(4) of input 1, The output is 0. In the right circuit, as there is odd number(5)of input 1,the output is 1 .

Task-3:-Switch making by X-OR gate

Simulation outputs:-

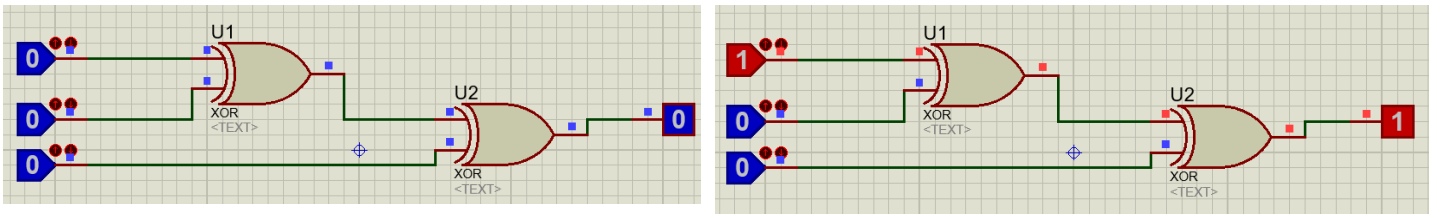

Fig.5. represents a switch maker circuit . Here ,the circuit is completely made by X-OR gate only. In the case of X-or gate, If we change the present state of input(1/0),then the output must change its present state.If the output is 0,by the change of any random input,ouput will be 1. So,in the figure 5, in the left circuit , there all input is 0, The output is also 0. In the right circuit, as we change one input 0 to 1 ,then the output is changed to 1 from 0.similarly, we can select any random input and can change its present states,the output also will change its present state.here, output 0 means switch off and output 1 means switch on. By increasing the number of x-or gates, we can give n number of input.So,the switch can be controlled by n number of users.

Task-4:-light controlling by SPDT and DPDT Switches

Simulation outputs:-

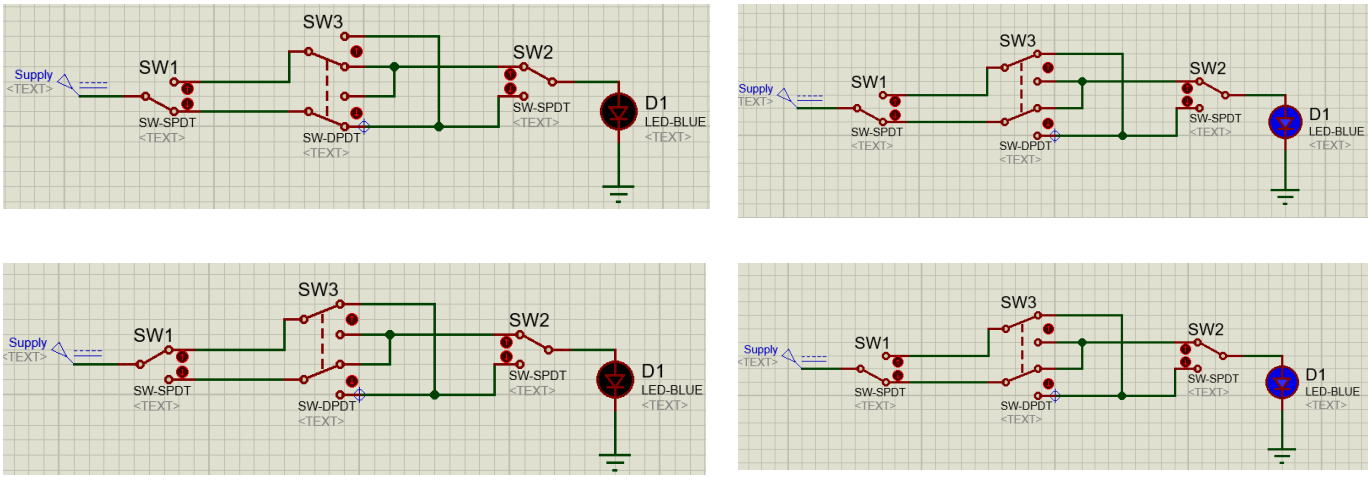

Fig.6. represents a light controlling circuit . Here ,the circuit is made by SPDT and DPDT switches, the DPDT switch will be connected in between two SPDT switches. A power supply of 5V is connected to first SPDT and the output led is connected to the second SPDT switch.So,in the left-top corner Figure , led is off when DPDT switch throw is down.Remaining two SPDT as before,when DPDT switch is made up,led is on that is shown on right top corner. Similarly, in the left-bottom corner Figure , led is off when first SPDT switch throw is up.Remaining DPDT as before,when SPDT swich is made down,led is on that is shown on right bottom corner

figure. So,here in the figure, the light can be controlled from 3 places as there is 1 DPDT switches.Therefore, If there is n number of DPDT switches, the light can be controlled from (n+2) number of places.

Experiment No.:-9

Task-1:- Design of logic gates(And,OR,NOT)by using two to one multiplexer

Simulation outputs:-

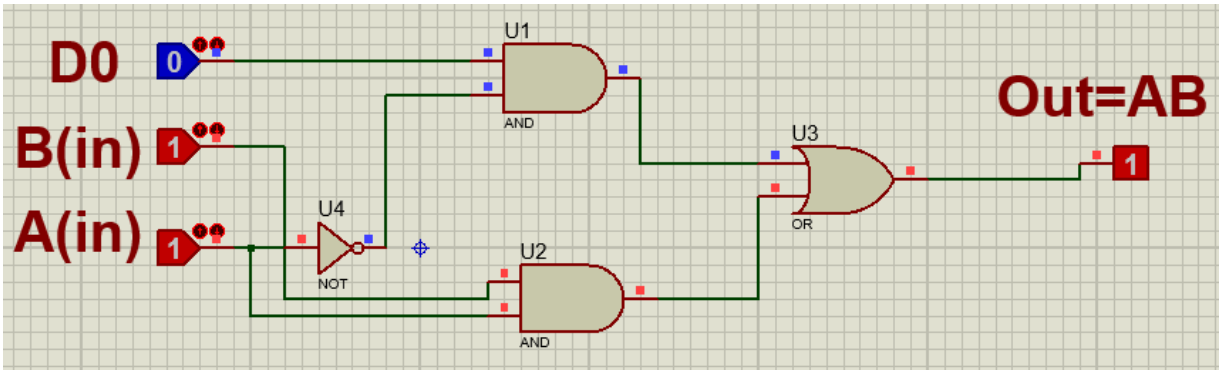

Fig.7 represents an AND gate designing circuit with a two to one multiplexer circuit.To make the circuit, we have to do one input of two to one multiplexer as fixed.Here,D0 (this input will be multiplied with the selection_bar input by AND gate) input should be fixed to 0 always.Then,another input of two to one multiplexer and the selection input will be worked as the variable A and B. As in AND gate if one input is 0,output is zero,so,if selection pin is 0(A input),output will be D0(0).If selection pin (A)is 1,output will be as B input(0/1).Thus,in the final output we will get the output of AND gate.for verifying the output, A=1, B=1 is kept.So,output,AB=1 is observed that verifies the circuit of AND gate.Others combination of AND gate can also be verified by this circuit(00,01,10). The truth table of and gate is given below:-

A	B	AND
0	0	0
0	1	0
1	0	0
1	1	1

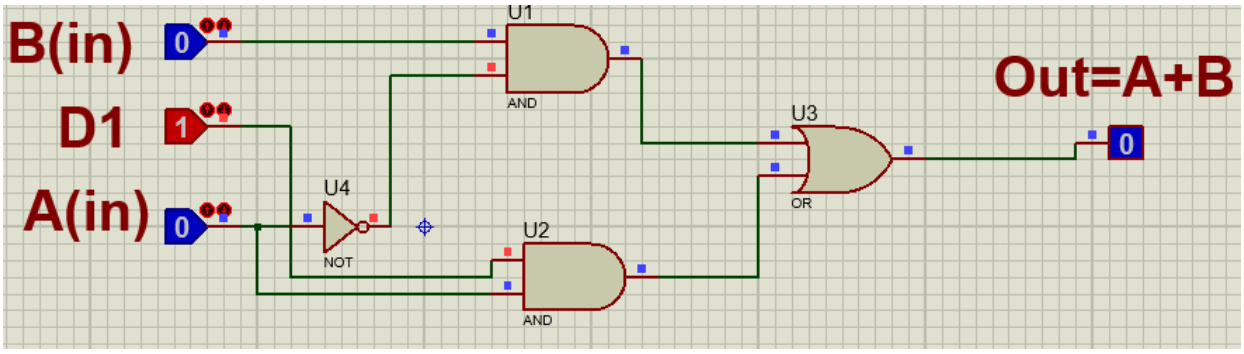

Fig.8 represents an OR gate designing circuit with a two to one multiplexer circuit.To make the circuit, we have to do one input of two to one multiplexer as fixed.Here,D1(this input will be multiplied with the selection input by AND gate) input should be fixed to 1 always.Then,another input of two to one multiplexer and the selection input will be worked as the variable A and B.As in OR gate if one input is 1,output is one,so,if selection pin is 1(A input),output will be D1(1).If selection pin (A)is 0,output will be as B input(0/1).Thus,in the final output we will get the output of OR gate.for verifying the output, A=0, B=0 is kept.So,output,A+B=0 is observed that verifies the circuit of OR gate.others combination of OR gate can also be verified by this circuit(11,01,10).The truth table of OR gate is given below:-

A	B	OR
0	0	0
0	1	1
1	0	1
1	1	1

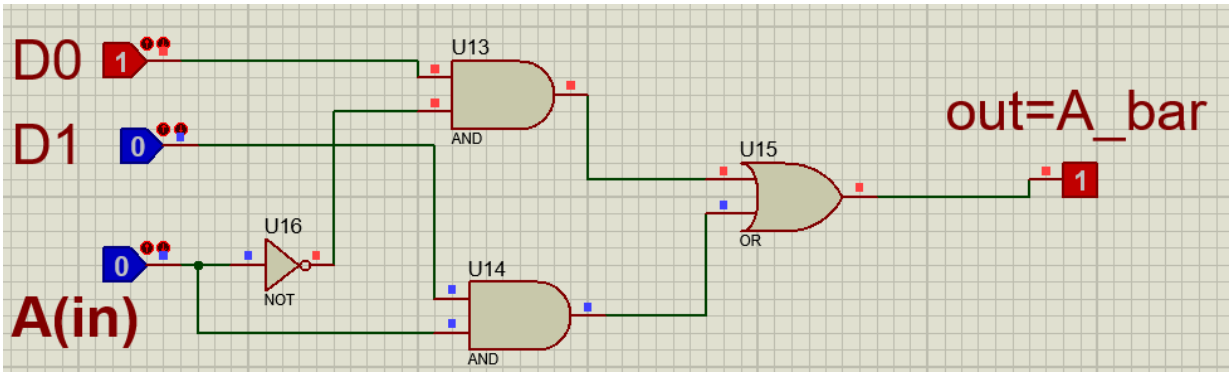

Fig.9. represents an NOT gate designing circuit with a two to one multiplexer circuit.To make the circuit, we have to do two input of two to one multiplexer as fixed.Here,D1(this input will be multiplied with the selection input by and gate) input should be fixed to 0 always. D0 (this

input will be multiplied with the selection_bar input by AND gate) input should be fixed to 1 always.Then, the selection input will be worked as the variable A . If here selection input is 0,in the output it will show the D0 input that is 1 whether if selection input is 1 ,in output it will show the D1 input that is 0.Thus,in the final output we will get the output of NOT gate.for verifying the output, A=0 is kept.So,output,A_Bar=1 is observed that verifies the circuit of NOT gate.others combination of NOT gate can also be verified by this circuit(if A=1,A_Bar=0).The truth table of NOT gate is given below:-

A	A_Bar
1	0
0	1

Task-2:- Design of four to one multiplexer by two to one multiplexer

Simulation outputs:-

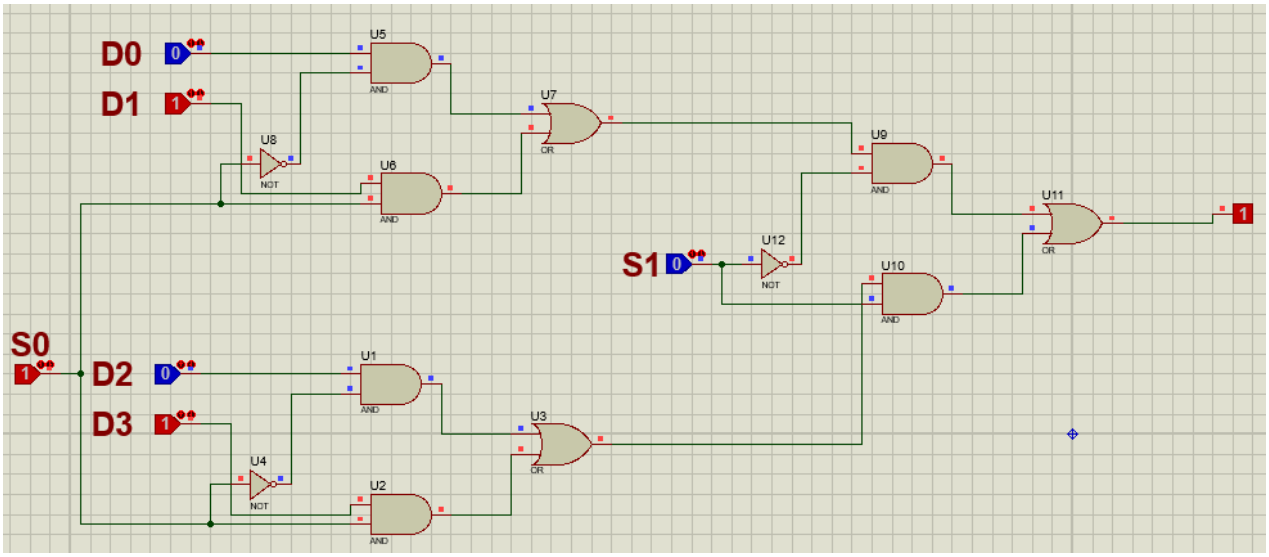

Fig.10. represents a four to one multiplexer using two to one multiplexer.In 2×1multiplexer,there are two input,D0 and D1,and one selection pin S.the output of 2×1 multiplexer is=(S_bar*D0)+(S*D1).In 4×1 multiplexer,there are 4 input(D0,D1,D2,D3),two selection pin(S0,S1) and the output will be =(S1_bar*S0_bar*D0)+(S1_bar*S0*D1)+(S1*S0_bar*D2)+(S0*S1*D3).So,to make a 4×1 multiplexer, three 2×1 multiplexer is needed.the selection pin of first two 2×1 multiplexer will be commoned and worked as S0 and the four input will be applied to this two multiplexer input. whether another selection pin of third 2×1 multiplexer selection pin will be worked as

S1 and the output is taken from this multiplexer.For verifying the output, here S0=1 and S1=0 is kept.So,the output will be as D1 that is kept 1. Other combination that is the truth table of 4×1 multiplexer is given below:-

S1	S0	OUTPUT
0	0	D0
0	1	D1
1	0	D2
1	1	D3

Task-3:- Design of logic gates by using four to one multiplexer

Simulation outputs:-

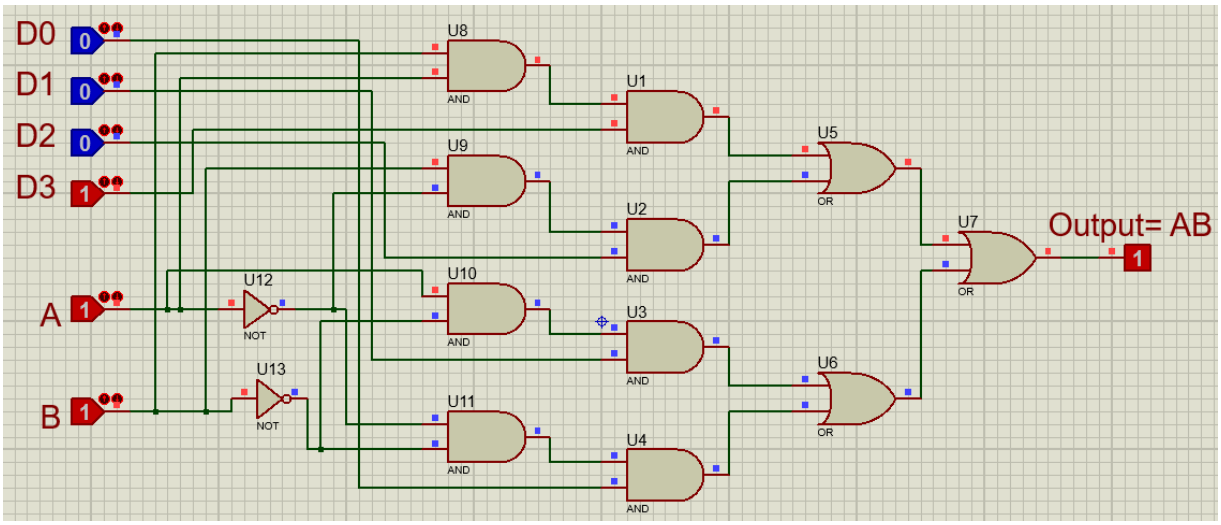

Fig.11 represents an AND gate designing circuit with a four to one multiplexer circuit.To make the circuit, we have to do four input of four to one multiplexer as fixed.Here,D0=0,D1=0,D2=0,D3=1 is kept.Then,the selection input of four to one multiplexer that is S0 and S1 will be worked as the variable A and B. As in and gate if one input is 0,output is zero,so,if selection pin S1=1 and S0=1(A and B input),output will be D3(1) according to the truth table.Thus,in the final output we will get the output of and gate.for verifying the output, A=1, B=1 is kept.So,output,AB=1 is observed that verifies the circuit of and gate.others combination of and gate can also be verified by this circuit(00,01,10).

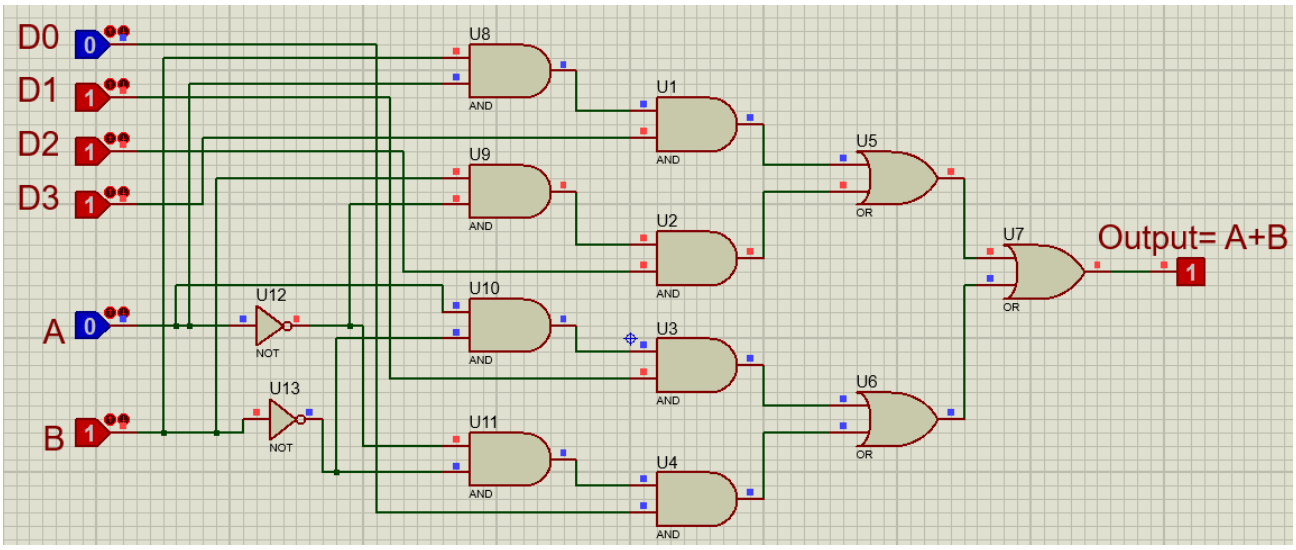

Fig.12 represents an OR gate designing circuit with a four to one multiplexer circuit.To make the circuit, we have to do four input of four to one multiplexer as fixed.Here,D0=0,D1=1,D2=1,D3=1 is kept.Then,the selection input of four to one multiplexer that is S0 and S1 will be worked as the variable A and B. As in OR gate if one input is 1,output is one,so,if selection pin S1=1 and S0=0(A and B input),output will be as D2(1) according to the truth table.Thus,in the final output we will get the output of OR gate.for verifying the output, A=0, B=1 is kept.So,output,A+B=1 is observed that verifies the circuit of OR gate.others combination of OR gate can also be verified by this circuit(00,11,10).

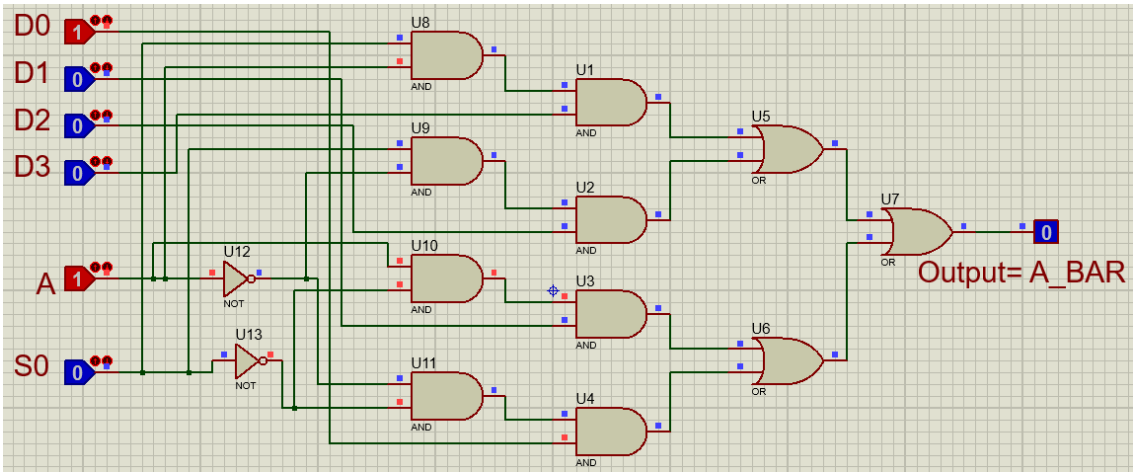

Fig.13. represents an NOT gate designing circuit with a four to one multiplexer circuit.To make the circuit, we have to do four input of four to one multiplexer as fixed. D0=1,D1=0,D2=0,D3=0 is kept.Then,one selection input S0 is kept fixed at 0 and another selection input will be worked as the variable A . If here selection input S1 (A)is 0,in the output it will show the D0 input that is 1 whether if selection input S1(A) is 1 ,in output it will show the D2 input that is 0.Thus,in the final output we will get the output of NOT gate.for verifying the output, A=1 is

kept.So,output,A_Bar=0 is observed that verifies the circuit of NOT gate.others combination of not gate can also be verified by this circuit(if A=1,A_Bar=0).

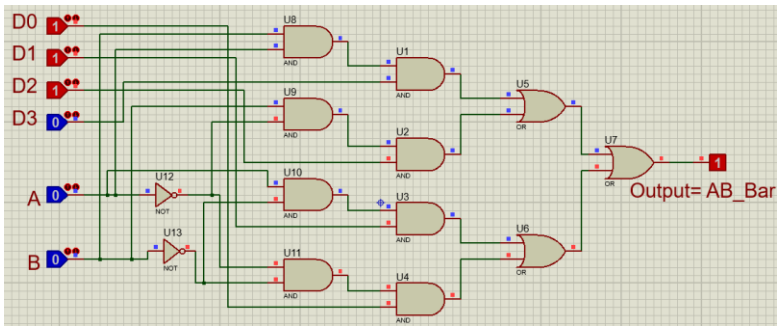

Fig.14 represents an NAND gate designing circuit with a four to one multiplexer circuit.To make the circuit, we have to do four input of four to one multiplexer as fixed.Here,D0=1,D1=1,D2=1,D3=0 is kept.Then,the selection input of four to one multiplexer that is S0 and S1 will be worked as the variable A and B. As in NAND gate if one input is 0,output is one,so,if selection pin S1=0 and S0=0(A and B input),output will be D0(1) according to the truth table.Thus,in the final output we will get the output of NAND gate.for verifying the output, A=0, B=0 is kept.So,output,AB_bar=1 is observed that verifies the circuit of NAND gate.others combination of NAND gate can also be verified by this circuit(11,01,10). The truth table of NAND gate is given below:-

A	B	NAND
0	0	1
0	1	1
1	0	1
1	1	0

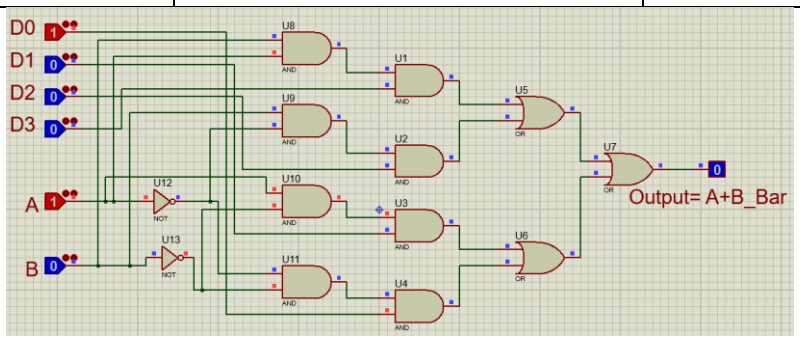

Fig.15 represents an NOR gate designing circuit with a four to one multiplexer circuit.To make the circuit, we have to do four input of four to one multiplexer as fixed.Here,D0=1,D1=0,D2=0,D3=0 is kept.Then,the selection input of four to one multiplexer that is S0 and S1 will be worked as the variable A and B. As in NOR gate if one input is 1,output

is zero,so,if selection pin S1=1 and S0=0(A and B input),output will be as D2(0) according to the truth table.Thus,in the final output we will get the output of NOR gate.for verifying the output, A=1, B=0 is kept.So,output,A+B_bar=0 is observed that verifies the circuit of NOR gate.others combination of NOR gate can also be verified by this circuit(00,11,01). The truth table of NOR gate is given below:-

A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0

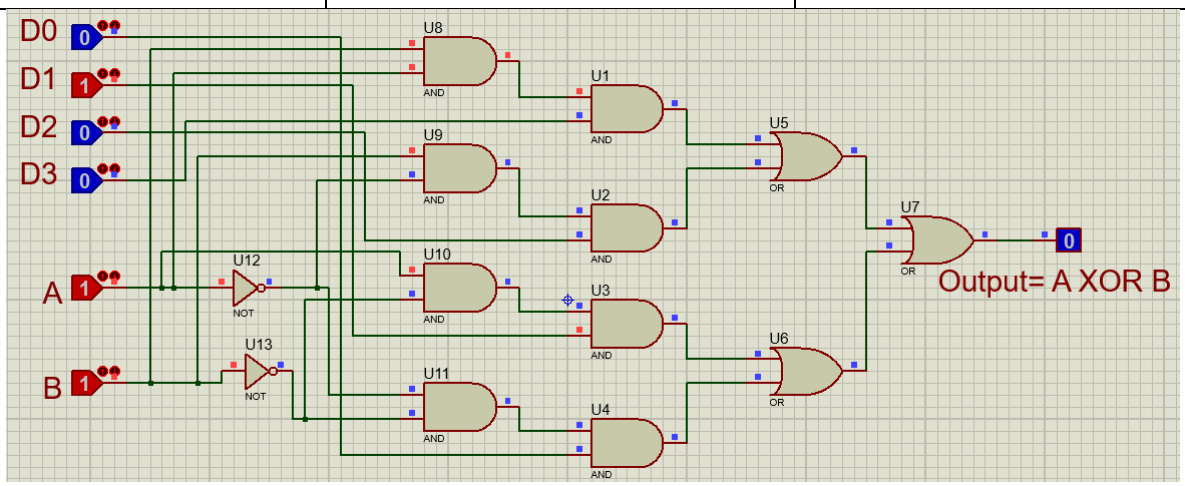

Fig.16 represents an X-OR gate designing circuit with a four to one multiplexer circuit.To make the circuit, we have to do four input of four to one multiplexer as fixed.Here,D0=0,D1=1,D2=0,D3=0 is kept.Then,the selection input of four to one multiplexer that is S0 and S1 will be worked as the variable A and B.If selection pin S1=1 and S0=1(A and B input),output will be as D3(0) according to the truth table.Thus,in the final output we will get the output of XOR gate.for verifying the output, A=1, B=1 is kept.So,output,A XOR B=0 is observed that verifies the circuit of XOR gate.others combination of XOR gate can also be verified by this circuit(00,10,01). The truth table of XOR gate is given below:-

A	B	X-OR(A_bar*B+A*B_bar)
0	0	0
0	1	1
1	0	1
1	1	0

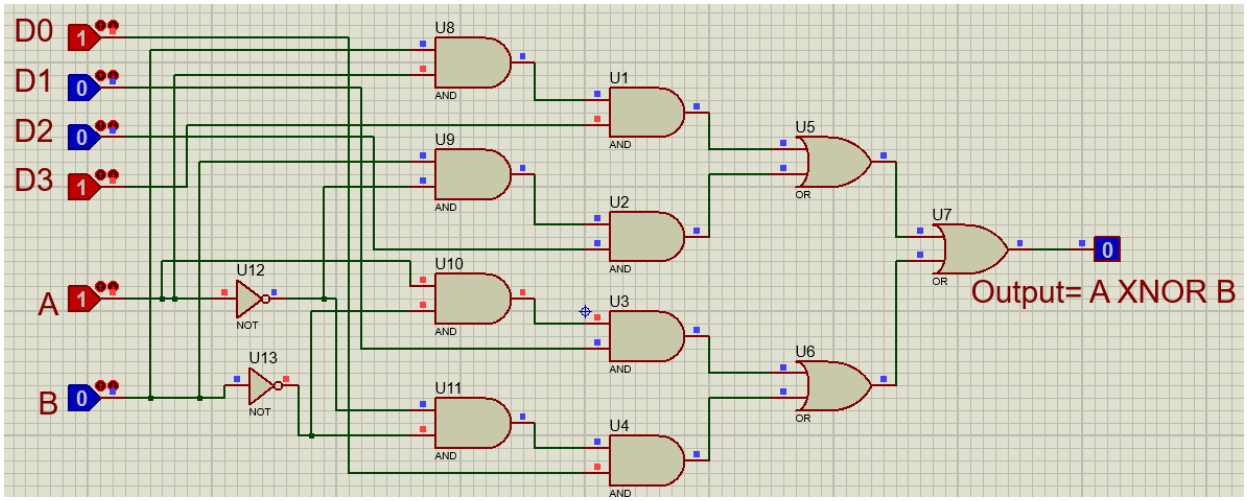

Fig.17 represents an X-NOR gate designing circuit with a four to one multiplexer circuit.To make the circuit, we have to do four input of four to one multiplexer as fixed.Here,D0=1,D1=0,D2=0,D3=1 is kept.Then,the selection input of four to one multiplexer that is S0 and S1 will be worked as the variable A and B.If selection pin S1=1 and S0=0(A and B input),output will be as D2(0) according to the truth table.Thus,in the final output we will get the output of XNOR gate.for verifying the output, A=1, B=0 is kept.So,output,A XNOR B=0 is observed that verifies the circuit of XNOR gate.others combination of XNOR gate can also be verified by this circuit(00,11,01). The truth table of XNOR gate is given below:-

A	B	XNOR(A_bar*B_bar+A*B)
0	0	1
0	1	0
1	0	0
1	1	1

Discussions:- In this experiment,by using logic gates,a 4 bit magnitude comparator is designed. Then,a parity bit checker circuit by using only x-or gate is made, this is important in data communication to Check whether data is lost or not.Then,two circuit, one is by X-OR gate and another is by SPDT and DPDT switches is made. By this two circuit led output can be controlled from n number of places. Then,by a 2×1 multiplexer AND,OR,NOT gates are designed.Then,a 4×1 multiplexer is made by 2×1 multiplexer.then,AND,OR,NOT, NAND,NOR,XOR,XNOR gates are designed by 4×1 multiplexer.