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CSE141L

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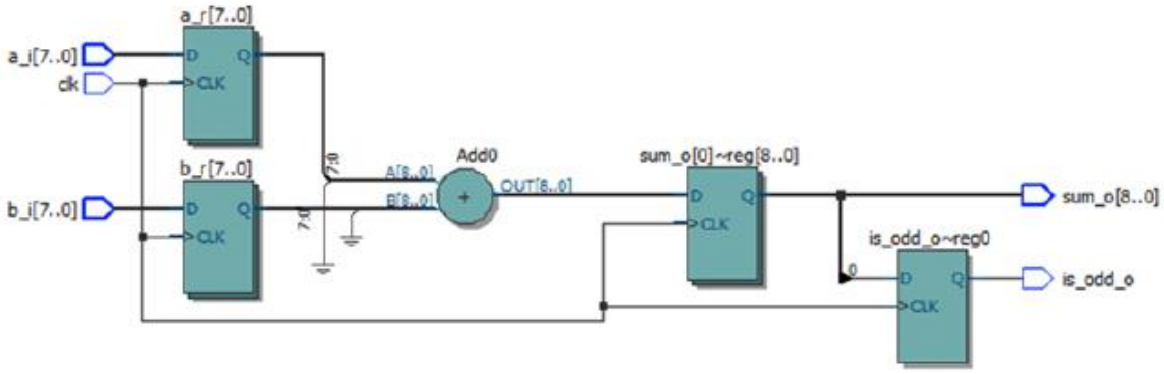
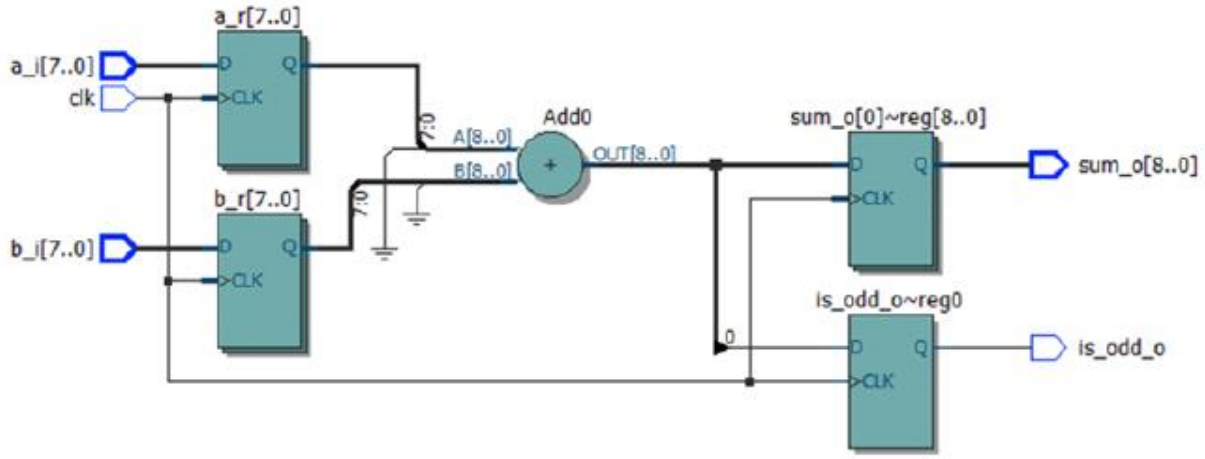
Lab 1

1. Draw a schematic for adder.sv. In your schematic, you should clearly show the function of the design by using flip-flops, various gates, comparators, adders, and/or wires. Try to infer a schematic from the Verilog source, but it is fine to use a generated schematic from Quartus II as long as it is detailed enough.
    a. Schamatic:



2. Modify adder.sv so that is_odd_o is simultaneously updated with sum_o. Perform the same behavioral simulation you did in the previous step again. Note: When updating your adder.sv, both sum_o and is_odd_o should be updated on the **second rising edge after the input(s) change.** Draw a schematic for the modified adder and include it in your report. You should also briefly describe what changes you needed to make in order to get the desired behavior.
    a. Schematic



3. FPGAs like the Altera part are comprised of a set of logic elements, each of which can contain a small portion of combinational logic, or a register, or both. Report the following information from your generated Place and Route reports:
    a. How many flip-flops (a.k.a. registers) are used for the design?
        i. 26
    b. How many flip-flops does the EP4CE40F29C6 have total?
        i. 39600
    c. How many combinational functions does your design use?
        i. 9
    d. How many combinational functions does the EP4CE40F29C6 have total?
        i. 39600
4. Report the following information from your timing reports **(You should always use the worst case (Slow 1200mV 85C Model) when measuring maximum clock frequency):**
    a. What is the reported Fmax of your design?
        i. 548.85 MHz
    b. What is the cycle time (cycle time = 1/Fmax) of your design? Show your work.
        i. 1/548.85 Mhz = 1.82 ns
5. Since your FPGA has limited hardware resources and you are always concerned about your performance, you should try to characterize the cost of different sizes of adders. Fill out the following table with information on adders ranging from 8 bits to 64 bits.

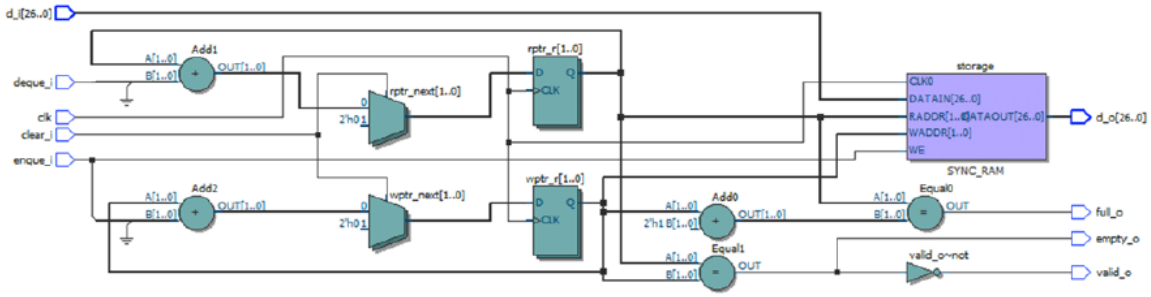
Width	Fmax in MHz	# of combinational functions	# of registers (flip-flops) used
8	548.85	26	26
16	416.32	50	50
32	311.24	98	98
64	196.16	194	194

6. Add the test cases described above to lab1\reg_file\src\tb\reg_file_tb.sv. What behavior do you expect in each of the three scenarios? Be specific.
    a. Reading from two different registers at the same time.
        i. Both registers should return the correct values
    b. Reading from the same register on both read ports.
        i. Both ports should return the correct values
    c. Reading from a register while writing to it.
        i. The port should return the value being written to the register
7. Fill out the following table for register files of different configurations. (Note that some register files might not fit in the FPGA device due to their demands on resources.) In such cases, explain the reason.

Configuration	Fmax in MHz	# of combinational functions	# of registers (flip-flops) used	# of memory bits

8 16-bit regs	325.53	322	186	0
16 16-bit regs	1010.01	29	29	512
32 16-bit regs	985.12	32	32	1024
32 64-bit regs	973.61	80	80	4096
256 32-bit regs	973.71	57	57	16384

8. Desugar the second always_ff block in fifo.sv. Make sure that fifo_tb.sv still passes after you have made your changes. Once you are done, draw a CLEAR, reasonable schematic for your desugared fifo.sv, assuming that default parameters are used. Be sure to label all wires and logic blocks with their names and their widths from the Verilog.
    a. Schematic:



9. It is important to know how to use ModelSim effectively for debugging. This includes knowing how to add relevant signals to the waveform window. Add a command to core\src\tb\core_tb\sim.tcl to add signals from the cl_decode submodule to the waveform window.
    a. Done
10. Measure the following data:
    a. Number of instructions executed.
        i. 160
    b. Number of cycles needed to run the program to completion.
        i. 3327
11. Report the following information from your generated Place and Route reports:
    a. How many flip-flops (a.k.a. registers) are used for the design?
        i. 2096
    b. How many combinational functions does your design use?
        i. 3918
    c. How many embedded RAM bits (memory bits) does you design use?
        i. 16384
    d. What is the reported Fmax?
        i. 55.57 MHz
    e. What is the cycle time of your design? Show your work.
        i. 1/55.57MHz = 1.8x10^-8
    f. If additional cores require no overhead beyond the resources required by a single core. Approximately how many cores could you instantiate and still fit? Show your work.
        i. Total logic elements/logic elements = 39600/5934 = 6.67

g. Execution time (# of cycles x cycle time).
    i. 60 micro seconds