FW version : GPNAAB3Q (CS 9.0)
FW release schedule : November 9th, 2018
Application on MP : 6weeks from release date.

Affected products	PM1725a HHHL	MZPLL1T6HEHP-00003
		MZPLL3T2HMLS-00003
		MZPLL6T4HMLS-00003
	PM1725a 2.5”	MZWLL800HEHP-00003
		MZWLL1T6HEHP-00003
		MZWLL3T2HMJP-00003
		MZWLL6T4HMLS-00003

General PM1725a *FW*
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JIRA ID	ISSUE-TYPE	SUMMARY	SEVERITY	LIKELIHOOD	DEFECT COMPONENT	FAILURE SCENARIO	ROOT CAUSE	FIRMWARE-CHANGES
EPICSW-5154	Enhancement	RAID recovery buffer allocation enhancement	Low	Mid	Performance	N/A	N/A	Allocate RAID recovery buffer from DRAM instead of SRAM.
NTM-11634	Defect	Assert condition when host sends multiple invalid commands	Medium	High	N/A	Host issues commands with wrong NLB	Host issues commands with wrong NLB setting caused one core to send Multiple "Invalid Filed in Cmd" errors to another core. The second core acknowledges the errors synchronously. The rate at acknowledgement sent from core 2 is slower than cores 1 error message send operation. This causes the firmware to ran out of resources and resulted in assert	Improve handling rate of IPC between the two cores to eliminate resource depletion
NTM-11741	Defect	PCIe Link Failure when external PERST# toggles quickly	High	High	N/A	Link failure might occur when PERST happens right after Hot Reset.	When PERST happens right after Hot Reset, there is a timing hole on PMA ready interrupt handling. If Hot Reset and PERST are over-lapped, the device might be put into an abnormal state. Samsung could also verify that the failure timing in NetApp's failure is exactly matched with Samsung's reproduction.	Workaround code in FW has been applied to mask PMA Ready interrupt source during PERST processing (Avoid handling of PMA Ready interrupt during above timing window)
NTM-11744	Defect	HeavyFWDown_Reset test on dual port cause system hang	Medium	High	Error Recovery	Connect dual port to server then run script on both port for 60 hours.	When FSQ is full CMD fetch cannot become idle 2) If we consider CMD fetch state waiting to write to FSQ as idle state then AXI errors occurs because ARb module is not idle.	Change the flow for Delete IO SQ because when multiple Delete SQ commands are outstanding the Command Fetch module cannot be idle. For fetch module to be idle arbitration idle is also required. This change is applied to QCC == 0 and FCC == 0 check
NTM-11805	Defect	Fixed low QD write performance drop issue	Low	High	Performance	Measure low QD write performance	It's a side effect of PMN-2176(buffer allocation issue fix) that was introduced on GPNA8B3Q.	Fixed write buffer allocation scheme
NTM-12101	Defect	NSSR handling times out	Medium	Very Low	Timeout	1 . FW DL 2. FW Activate 3. Interrupt Step#2 with NSSR Expect FW Activate will FAIL due to interruption as expected but NSSR takes longer	Debug Dump triggered by test and NSSR Meta save use the same resource resulting in NSSR timeout	Isolate the resources needed for NSSR meta data saves and debug dump
NTM-12207 / NTM12606	Defect	Port missing in dual port reset when resets are issued while firmware activation is in progress	Low	Low	Command Functionality	Issue reset in 1 port while FW is being activated(CA=3) on other port	A race condition where a reset received during a small window while activation is in progress re-initializes activation state causing the port to be missed Control to fetch commands at device level was not enabled by new firmware.	When Firmware activation begins, notify host interface core to process the reset as standalone. This will prevent handling of reset while activation is in progress by the core handling the activation Controls to fetch commands are enabled at both device and port level
~~NTM-12275~~	~~Defect~~	~~Incorrect command is abort on Abort command~~	~~Low~~	~~Low~~	~~Command Functionality~~	~~Issue commands with same SQ Id and Cmd Id on both ports and issue a command to abort 1 of the command~~	~~Firmware didn't check Port ID and Function ID when searching target command resulting in command from other port being aborted~~	~~Check port ID and function ID in addition to SQ ID and Cmd ID when searching target command for an Abort command.~~
NTM-12275	Defect	Data units read mismatch Failure	High	High	HIL	FW upgrade with same version and a read operation leads to SMART data value (read as) zero.	From the memory dump it was observed that during the shutdown process if the reset happens before shutdown is complete, the command arbitration gate is opened earlier than expected which causes IOs to come in. Because the drive was in process of shutting down, the saving of Meta data is disabled which causes the performance counters to not increment on the drive side as they get incremented on the host side.	Shutdown handling modified to suit Dual port and cover corner cases like this.

NTM-12478	Defect	Identify command timeout during LFU	Low	Low	Timeout	During a mixed Live FW Update and FLR (Functional Level Reset) test, it was observed that an Identify command timed out.	Race condition between LFU update and FLR handling caused drive to enable CC.EN and accept commands before it is ready to process the command after LFU. This caused incoming commands (an identify command in this case) not being processed and led to time out	Use internal flag to manage internal state transitions between LFU and FLR handling to avoid such race condition.
NTM-12295	Defect	Device missing on a port after controller reset	Low	Low	Command Functionality	1. Port 0 is running ping pong test 2. Port 1 is running controller reset When this sequence is repeated, host observes device is missing on port 1	FLR handling from port 0 is delayed because all reset interrupts are masked while firmware is being reloaded. This resulted in host dropping the drive	FLR interrupt is not masked as part of FW update and handled FLR in Host Interface core. This resulted in servicing FLR without any delay preventing host from dropping the drive
NTM-12543	Defect	Timeout of controller enable(CC.EN=1)	Low	Very Low	Command Functionality	FW_DW_DUAL_RESET failed at NVMe_PCIe_RESET	Reset standalone path will unmask CC.EN and CC.EN interrupt can come in during firmware activation. Because we handle CC.EN early, so we won't set RDY bit.	Remove the unmask CC.EN in reset standalone which is not needed.
NTM-12566	Defect	NVMe I/O failed, Device Not ready	High	Low	Other	Device not ready caused NVMe I/O failed to read	1) Fix CPU CYCLE was negative value by converting INT32 type. UINT32 type is applied to calculate the delta CPU cycle between last PERST and current. 2) Discard False PMA ready interrupt only if PERST is observed by bootLoader. PMA ready interrupt is discarded only if PERST ASSERT is followed by PMA ready interrupt within 700us. If PERST ASSERT is not observed by bootloader, PMA ready is handled as valid	1) Fix CPU CYCLE was negative value by converting INT32 type. UINT32 type is applied to calculate the delta CPU cycle between last PERST and current. 2) Discard False PMA ready interrupt only if PERST is observed by bootLoader. PMA ready interrupt is discarded only if PERST ASSERT is followed by PMA ready interrupt within 700us. If PERST ASSERT is not observed by bootloader, PMA ready is handled as valid
NTM-12579	Defect	Memory dump SPO addresses mismatch	High	High	Command Functionality	SPO memory dump region is incorrect.	SPO Memory dump buffer address is incorrect.	Updated correct memory dump address.
NTM-12646	Defect	Preserve current feature values after live firmware update	Low	High	Command Functionality	Change feature values using SetFeature command. After live firmware update, the current feature values are reverted to default values	This was a bug in firmware where it incorrect overwrites current value with default value after live firmware update	Added code to preserve current feature values cross live firmware update
NTM-12657	Defect	Crash Dump generation allocating additional Backup memory without freeing	High	High	N/A	Crash dump stuck	Crash Dump generation allocating additional Backup memory without freeing, leading to overflow	Freeing previous memory before second backup starts.
NTM-12733	Defect	Command Latency observed by host	Low	Low	Command Functionality	When host issues commands on both ports, host may observe additional latency	Firmware was incorrectly checking only port 0 and not port 1 for outstanding commands before triggering background meta save causing additional latency.	Saving of background metdata is performed when there are no outstanding commands on bpth ports
NTM-12767	Defect	Drive link up failure during reset test	high	Low	Command Functionality	Reset + I/O stress test. Drive dropped offline	A corner case handling code didn't enable/disable IRQ correctly and caused IRQ was incorrectly enabled during IRQ handling, and led to nested interrupts and stack overflow.	Fixed the code where IRQ enable/disable was not implemented correctly
NTM-12832	Defect	ID Timeout after FW activation	High	Low	FW Download	After FW activation, RDY bit is set but ID time out	Function level arbitration for FW activation is enabled late	Enable the function level arbitration before user volume open for FW activation with reset case

NTM-12945	Defect	FW Activation Failed When Primary FW Image Copy Is Bad	High	Low	FW Download	Stress dual port I/O + FW download/activation test. FW activation failed after ~25,000 cycles	Drive maintains two copies for each slot. If loading FW image from primary copy fails, the drive should try to load the FW image from mirror copy. However, this part of code was not implemented properly and drive failed to load FW from mirror copy	Correct the code to 1) load from mirror copy when primary copy fails to load, 2) repair primary copy after successful loading from mirror copy
NTM-13009	Defect	Window'7 will not boot	High	High	Command Functionality	Windows fails to boot in some systems	If host issues FLR or PERST before drive finishes initialization, it is possible that the CC.EN enabling interrupt will not be processed in time because this interrupt was temporarily masked during initialization. This can cause some Windows systems failed to boot.	Unmask the CC.EN interrupt handling as soon as possible during initialization
NTM-13053	Defect	Reset handling issue when Controller Reset occurs while port reset is being processed	High	High	N/A	If there is any higher pending interrupt, this interrupt will be discarded. but the current check code has omitted peding port reset in case of controller reset	Since we clear the cc.en and ctrl reset mask in reset standalone mode, therefore port level reset can happen with ctrl reset at same time. We don't need to handle the ctrl reset in this case.	When ctrl reset happens, if there is port level reset going, we ignore the ctrl reset.
NVME-1148	Feature	Make sure all the Error Notifiers register to Error manager after Error manager initialization	N/A	N/A	N/A	N/A	N/A	Make all error notifiers register to Error manager after Error manager has initialized.
NVME-1423	Feature	Enable GET_SET_FEATURE_PERSIST_OVER_LFU	N/A	N/A	N/A	N/A	N/A	set GET_SET_FEATURE_PERSIST_OVER_LFU
PM1723B-1631	Defect	Crash dump might not be completed	Low	Mid	Crash dump	Crash dump is not completed, when it is triggered.	A race condition might occur among cores during a crash dump process, which causes the case that a crash dump might not be completed.	Added sync state among cores to avoid a race condition.
PMN-2204	Defect	Incorrect SMART Media Error Count After SPO	Low	Mid	SMART	Issue Write Uncorrectable to create UECC errors, then issue read command to get UECC errors. Randomely power cycle the drive and check SMART media error count after power on	During firmware bring-up process, SMART data from SPO buffer gets uploaded to FW run-time memory in normal case. When CC.EN gets enabled before the SMART initialization process, there is a defect in firmware that the timestamp in HIL meta gets updated. And, since the timestamp in HIL meta is more recent than the timestamp in SPO buffer, the SMART data in SPO buffer gets overwritten by the old data in HIL meta.	Fixed to use the newest SMART data from SPO buffer in the failure case.
PMN-2208	Defect	A device open might take more than a normal open case if a device shutdown happens whilist a deallocate operation is in progress.	Low	Mid	Performance	During "POR/Reset + IO/DSM" regression, FTL user volume open might take more than 10sec	If a device shutdown happens whilst deallocate operation is in process, FTL user volume open might take more that 10sec occur since FTL map information from previous deallocate process was not updated and resumed before FTL user volume open process.	enhanced deallocate operation code to update FTL map information before shutdown.
	Defect	Write command timeout	Low	Low	N/A	Random Read/Write (OK) Get Log page (OK) Seq. Write (Fail)	In failed case, there is write request from host following Cache flush request happens almost same time. Then, write buffer state is changed to Prevention state for Cache flush, but missed to transit to active state for Write request So, it makes false Write buffer full state because of Prevention state, and causes Assert because write request from host cannot be handled due to no active buffer.	Its simple fix to handle hole for write request from host in case of entering Cache flush operation. Write request will be reserved instead of missing on the operation in starting Cache flush.