ENGR. ALAN MANUEL K. GLORIA

January 1, 1983
Filipino

#7, 3rd Flr., Sto. Tomas St.,
Bgy. Don Manuel, Quezon City, M.M., 1113
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Work Experience

Senior R&D Engineer 2017-02-20 — Present
Nokia Technology Center Philippines, Inc., Metro Manila, Philippines

- Senior R&D Engineer (1 year, 2017-Present)

Since 2017, implementing and debugging software for cellular base stations.

Senior Digital Systems Architect 2004-07-07 — 2017-01-20 (12 Years)
Rohm LSI Design Philippines, Inc., Metro Manila, Philippines

- Middle-Level Management (7 Years, 2009-2017)
- LSI digital design (8 Years, 2007-Present)
- LSI functional verification (2 Years, 2006-2007)
- LSI reverse-engineering (3 Years, 2004-2006)

Since 2007, designing LCD and OLED Active Matrix Display Drivers, initially for cellphones (2007-2009) and later for automotive (2009-Present), including management responsibilities and verification. Pioneered in 2009 the use of software Object-Oriented Programming techniques (SystemVerilog classes and industry standard Universal Verification Methodology) to create IC verification environments at this company.

Programming Skills

Expert in C, C++, Posix. Intermediate in Scheme, Haskell, Javascript, IA32 / AMD64 Assembly, and shell scripting. Expert in object-oriented design. Intermediate in functional programming. Recently learning Vala. Can write a little Perl, Ruby, and Python.

Co-author (with David A. Wheeler) of two Scheme Requests for Implementation, SRFI-105 (Curly-infix-expressions, 2012) and SRFI-110 (Sweet-expressions, 2013).

Some understanding of Bitcoin technology including but not limited to: Bitcoin SCRIPT, 1 RETURN, payment channel implementations, softfork vs hardforks, atomic swaps, funding transactions as an offchain pattern, HTLC, adaptor signatures in Scriptless Script, MimbleWimble, sidechains, Lightning Network. Contributes pseudonymously to c-lightning development.

Digital LSI Design Skills

Expert in Verilog (IEEE 1364-1995, IEEE 1364-2001) and SystemVerilog (IEEE 1800-2005, IEEE 1800-2009). Expert in digital architectures for display drivers. Extensive experience in writing synthesizable RTL and digital design verification environments, particularly constrained randomized stimulus and automated output checking. Expert in multi-clock design and multi-lane logic pipelines.

Education

University of Santo Tomas, *B.S., Electronics and Communications Engineering*,
Graduated *cum laude*, March 2004

Seminars
JG Nera Training Consultants, *Foundations of Leadership Excellence: Planning, Organizing, Leading, & Controlling (POLC)*, July 2014

Interests
Bitcoin
Lightning Network
Computer programming
Game programming
Science fiction